

BLS6G3135-20; BLS6G3135S-20

LDMOS S-Band radar power transistor

Rev. 4 — 11 March 2013

Product data sheet

1. Product profile

1.1 General description

20 W LDMOS power transistor intended for radar applications in the 3.1 GHz to 3.5 GHz range.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ }^{\circ}\text{C}$; $t_p = 300\text{ }\mu\text{s}$; $\delta = 10\text{ }\%$; $I_{DQ} = 50\text{ mA}$; in a class-AB production test circuit.

Mode of operation	f (GHz)	V _{DS} (V)	P _L (W)	G _p (dB)	η_D (%)	t _r (ns)	t _f (ns)
Pulsed RF	3.1 to 3.5	32	20	15.5	45	20	10

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

- Typical pulsed RF performance at a frequency of 3.1 GHz to 3.5 GHz, a supply voltage of 32 V, an I_{DQ} of 50 mA, a t_p of 300 μs and a δ of 10 %:
 - ◆ Output power = 20 W
 - ◆ Power gain = 15.5 dB
 - ◆ Efficiency = 45 %
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (3.1 GHz to 3.5 GHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

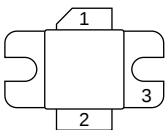
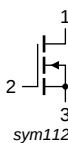
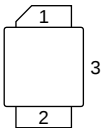


1.3 Applications

- S-Band power amplifiers for radar applications in the 3.1 GHz to 3.5 GHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLS6G3135-20 (SOT608A)			
1	drain		
2	gate		
3	source		
BLS6G3135S-20 (SOT608B)			
1	drain		
2	gate		
3	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLS6G3135-20	-	flanged ceramic package; 2 mounting holes; 2 leads	SOT608A
BLS6G3135S-20	-	ceramic earless flanged package; 2 leads	SOT608B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	60	V
V_{GS}	gate-source voltage		-0.5	+13	V
I_D	drain current		-	2.1	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Max	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 20\text{ W}$			
		$t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$	0.76	0.92	K/W
		$t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$	0.79	0.95	K/W

6. Characteristics

Table 6. Characteristics

$T_j = 25\text{ °C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.5\text{ mA}$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 40\text{ mA}$	1.4	2	2.4	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	1.5	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	6	8.2	-	A
I_{GSS}	gate leakage current	$V_{GS} = 8.3\text{ V}; V_{DS} = 0\text{ V}$	-	-	150	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 1.4\text{ A}$	-	2.8	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 1.4\text{ A}$	-	0.37	0.58	Ω

7. Application information

Table 7. Application information

Mode of operation: pulsed RF; $t_p = 300\text{ }\mu\text{s}; \delta = 10\text{ }\%$; RF performance at $V_{DS} = 32\text{ V}; I_{DQ} = 50\text{ mA}; T_{case} = 25\text{ °C}$; unless otherwise specified; in a class-AB production circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
P_L	output power		-	20	-	W
V_{CC}	supply voltage	$P_L = 20\text{ W}$	-	-	32	V
G_p	power gain	$P_L = 20\text{ W}$	12	15.5	-	dB
η_D	drain efficiency	$P_L = 20\text{ W}$	40	45	-	%
t_r	rise time	$P_L = 20\text{ W}$	-	20	50	ns
t_f	fall time	$P_L = 20\text{ W}$	-	10	50	ns

7.1 Impedance information

Table 8. Typical impedance

f	Z_S	Z_L (optimized for η_D)	Z_L (optimized for G_p)	$G_{p(opt)}$	η_D [1]
GHz	Ω	Ω	Ω	dB	%
3.1	$31.24 - j31.07$	$6.99 + j12.9$	$13.01 + j14.75$	18.08	48.34
3.2	$50.56 - j12.48$	$5.82 + j8.77$	$11.47 + j11.17$	17.97	45.60
3.3	$43.66 + j17.27$	$2.32 + j6.17$	$10.05 + j10.55$	17.75	47.01
3.4	$24.13 + j28.47$	$5.52 + j6.10$	$9.93 + j8.48$	17.91	47.03
3.5	$10.56 + j22.21$	$5.79 + j3.19$	$9.37 + j5.73$	17.68	46.54

[1] Measured with Z_L optimized for G_p .

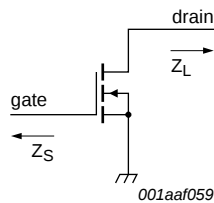


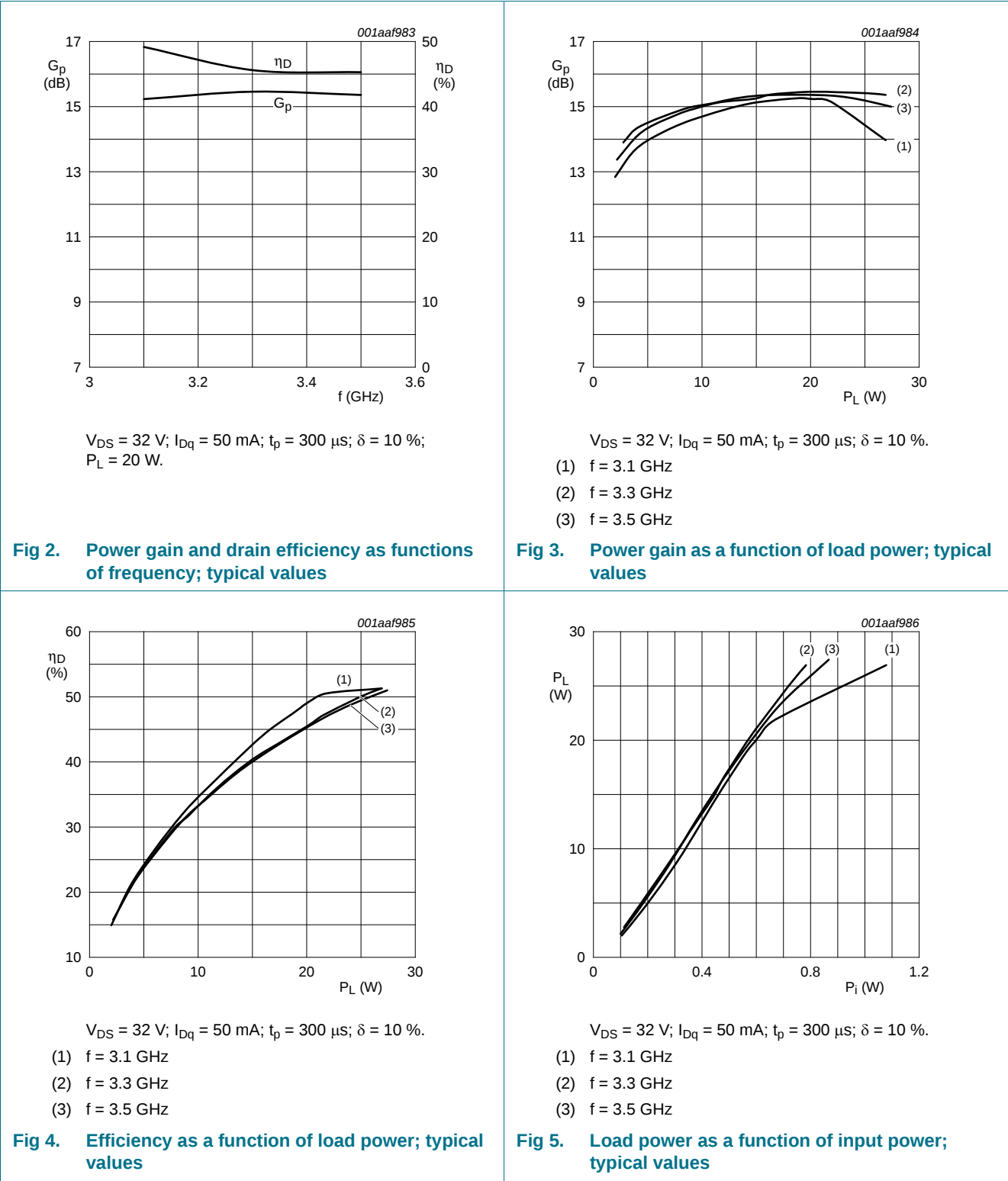
Fig 1. Definition of transistor impedance

7.2 Ruggedness in class-AB operation

The BLS6G3135-20 and BLS6G3135S-20 are capable of withstanding a load mismatch corresponding to VSWR = 5 : 1 through all phases under the following conditions:

$V_{DS} = 32$ V; $I_{Dq} = 50$ mA; $P_L = 20$ W; $t_p = 300$ μ s; $\delta = 10$ %.

7.3 Graphs



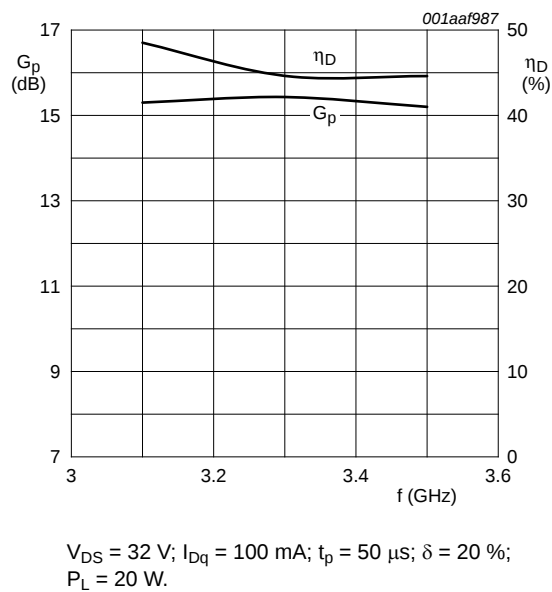


Fig 6. Power gain and drain efficiency as functions of frequency; typical values

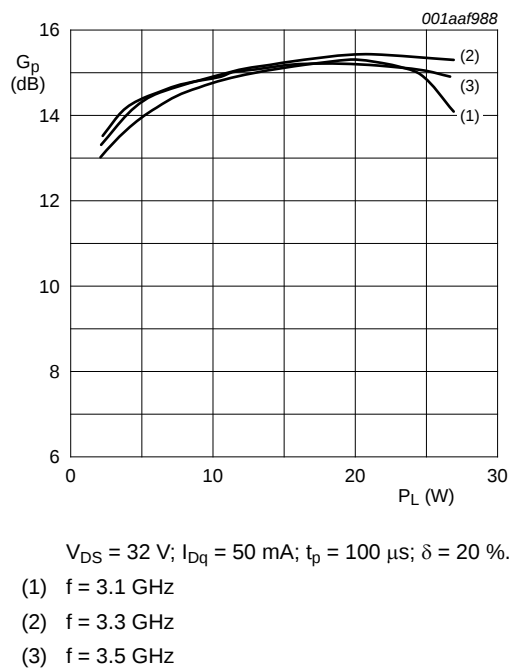


Fig 7. Power gain as a function of load power; typical values

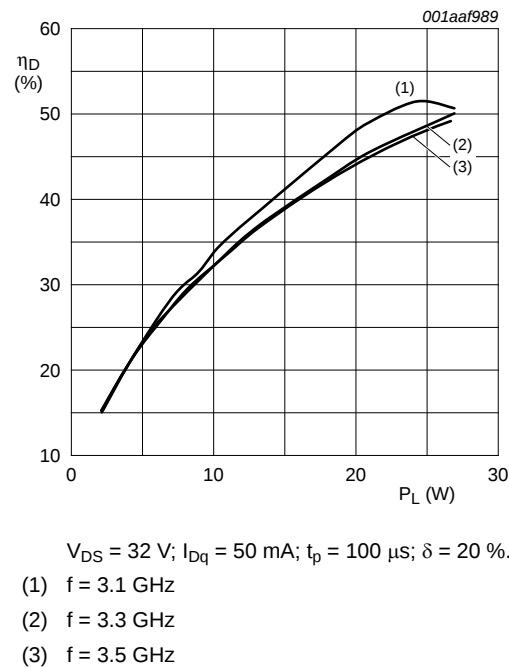


Fig 8. Efficiency as a function of load power; typical values

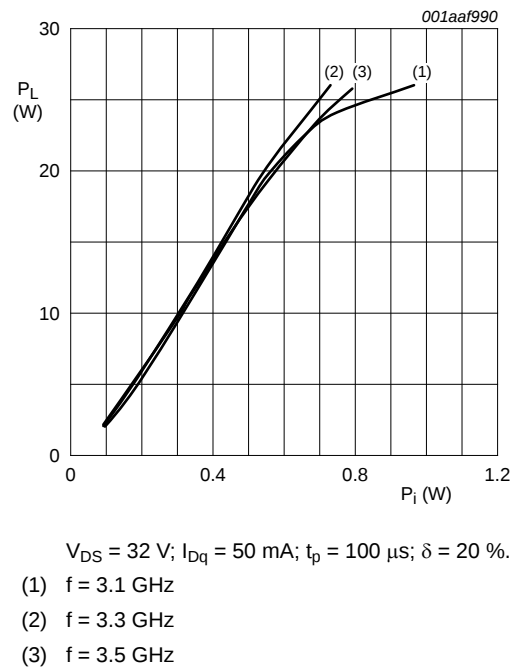


Fig 9. Load power as a function of input power; typical values

8. Test information

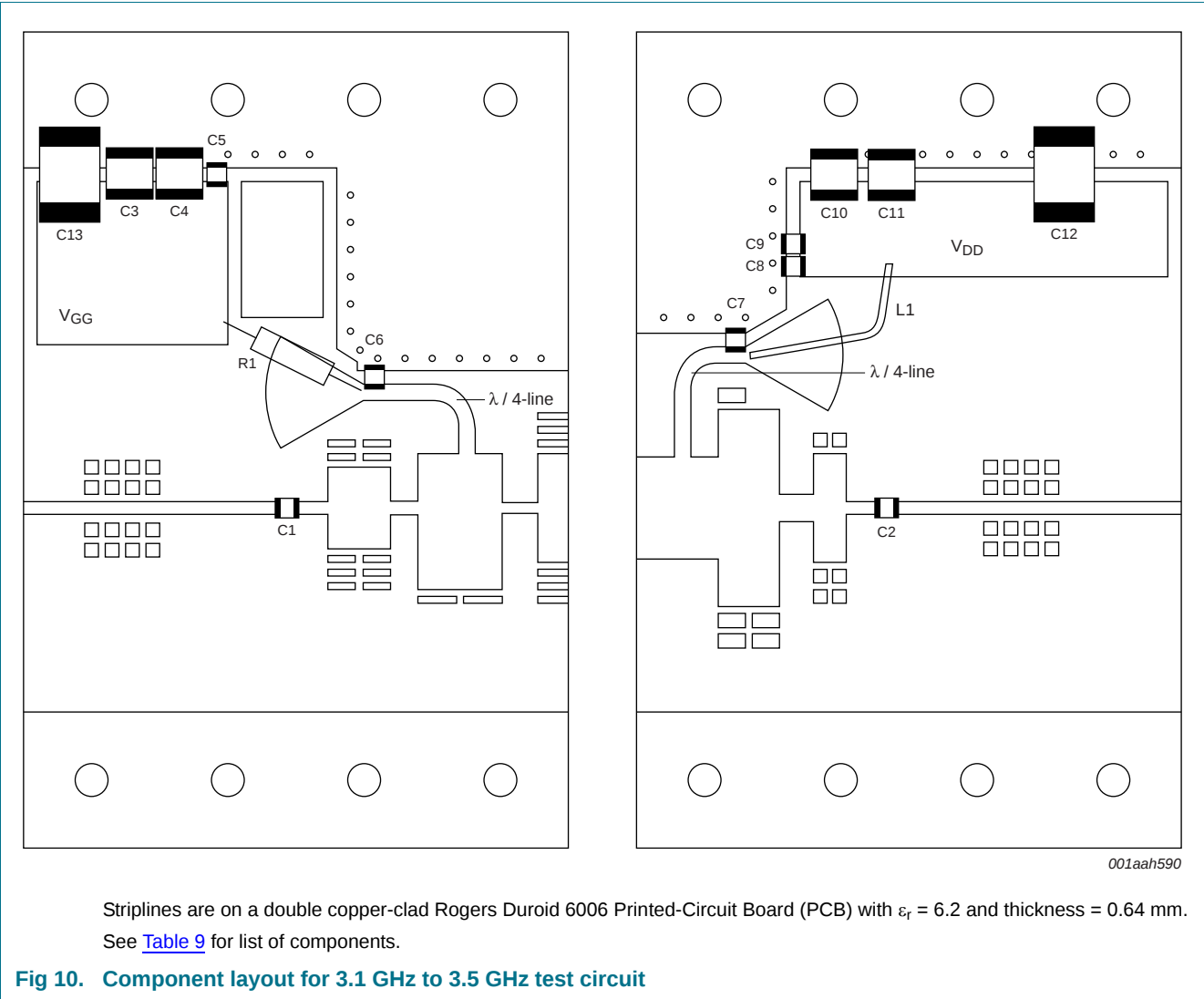


Table 9. List of components
See [Figure 10](#).

Component	Description	Value	Remarks
C1, C2, C5, C6, C7, C8, C9	multilayer ceramic chip capacitor	33 pF	[1]
C3, C4, C10, C11	multilayer ceramic chip capacitor	470 pF	[2]
C12	electrolytic capacitor	47 μF; 63 V	
C13	electrolytic capacitor	10 μF; 35 V	
L1	copper wire	-	
R1	resistor	49.9 Ω	

[1] American Technical Ceramics type 100A or capacitor of same quality.
[2] American Technical Ceramics type 100B or capacitor of same quality.

9. Package outline

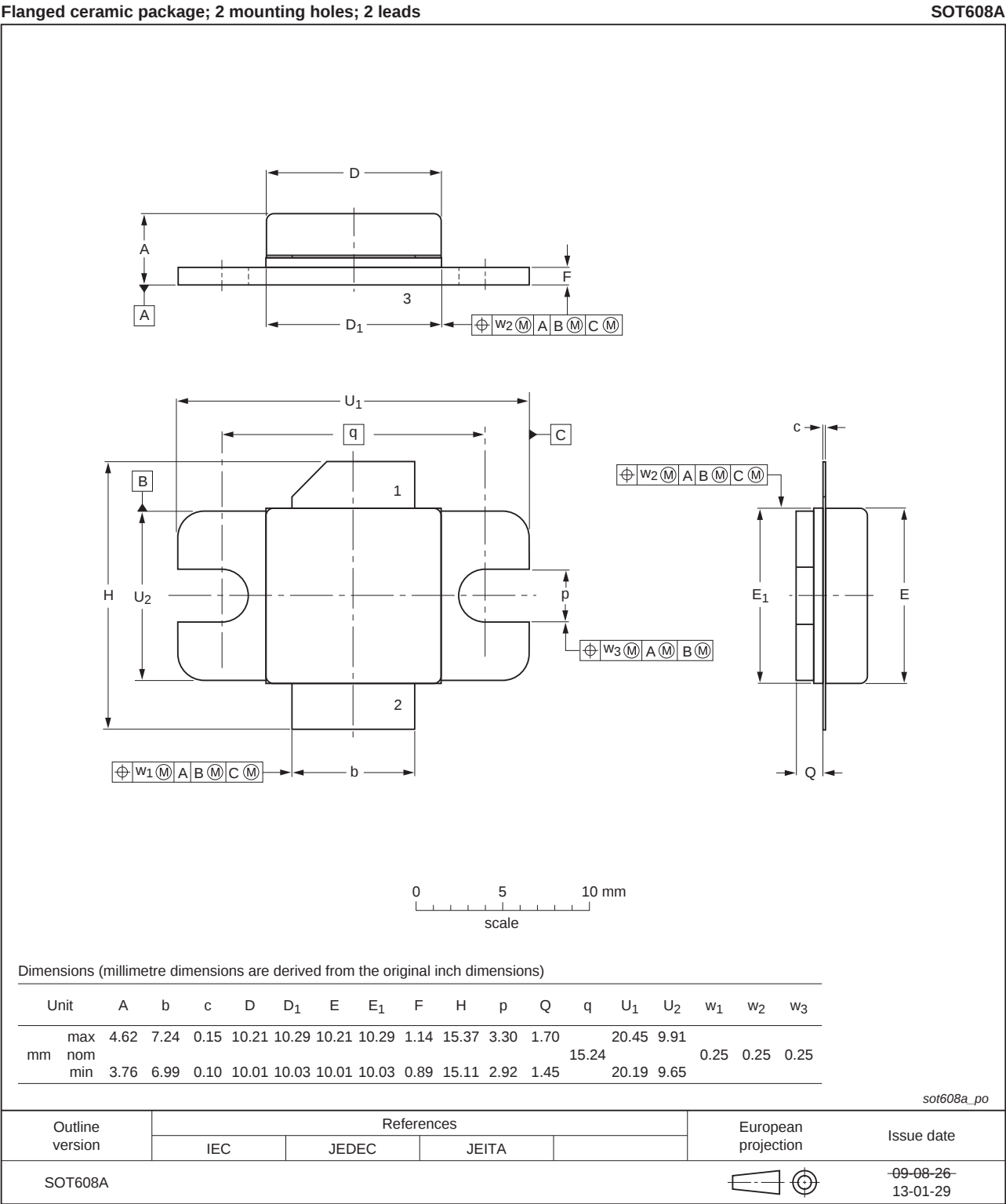
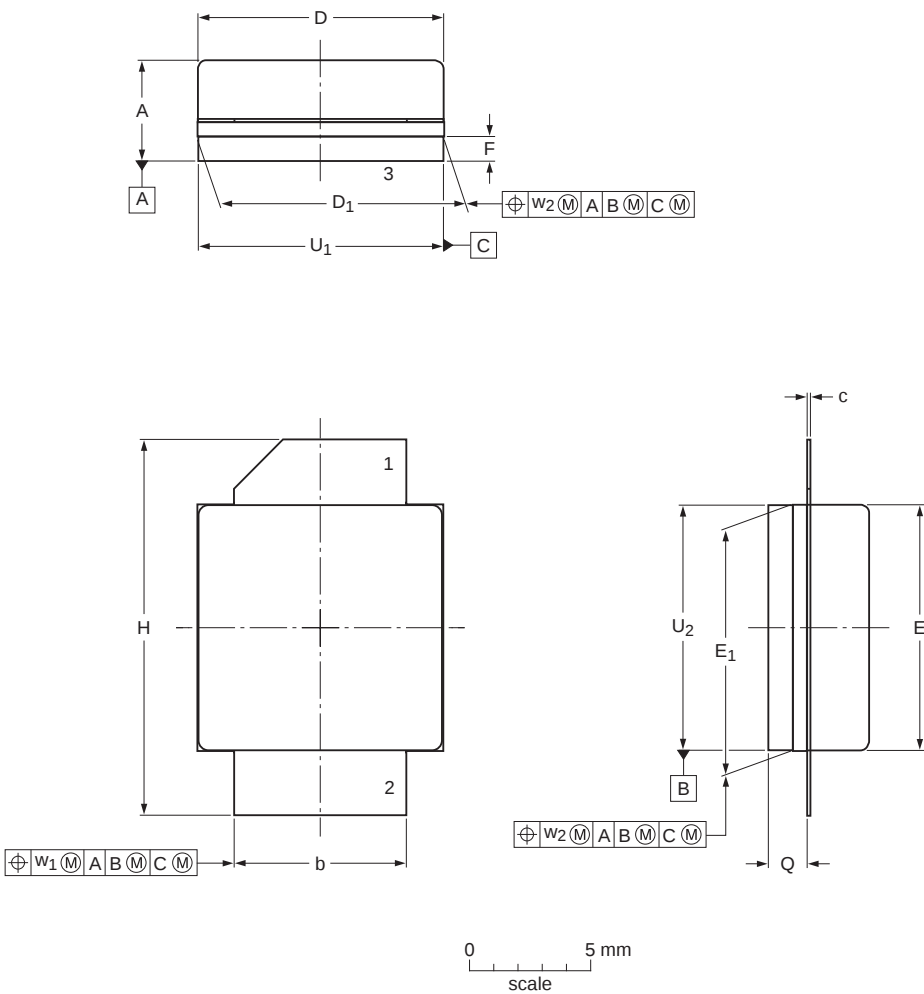


Fig 11. Package outline SOT608A

Ceramic earless flanged package; 2 leads

SOT608B



Dimensions (millimetre dimensions are derived from the original inch dimensions)

Unit	A	b	c	D	D ₁	E	E ₁	F	H	Q	U ₁	U ₂	w ₁	w ₂
max	4.62	7.24	0.15	10.21	10.29	10.21	10.29	1.14	15.37	1.70	10.24	10.24		
mm													0.25	0.25
nom														
min	3.76	6.99	0.10	10.01	10.03	10.01	10.03	0.89	15.11	1.45	9.98	9.98		

sot608b_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT608B						09-08-26 13-01-29

Fig 12. Package outline SOT608B

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
LDMOS	Laterally Diffused Metal Oxide Semiconductor
RF	Radio Frequency
S-Band	Short wave Band
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLS6G3135-20_6G3135S-20 v.4	20130311	Product data sheet	-	BLS6G3135-20_6G3135S-20_3
Modifications:	• Update of Package Outline drawing.			
BLS6G3135-20_6G3135S-20_3	20090303	Product data sheet	-	BLS6G3135-20_6G3135S-20_2
BLS6G3135-20_6G3135S-20_2	20081217	Product data sheet	-	BLS6G3135-20_6G3135S-20_1
BLS6G3135-20_6G3135S-20_1	20070307	Objective data sheet	-	-

12. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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