REJ03B0071-0040Z
Rev.0.40
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1. Overview

The M16C/26A group (M16C/26A, M16C/26T) of single-chip microcomputers is built using the high-performance silicon gate CMOS process using a M16C/60 Series CPU core and is packaged in a 42-pin and 48-pin plastic molded QFP. These single-chip microcomputers operate using sophisticated instructions featuring a high level of instruction efficiency. With 1M bytes of address space, they are capable of executing instructions at high speed. In addition, this microcomputer contains a multiplier and a DMAC which combined with fast instruction processing capability, makes it suitable for control of various OA, communication, and industrial equipment which requires high-speed arithmetic/logic operations.
There is a Normal-ver. for M16C/26A and T-ver. and v-ver. for M16C/26T.

1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment,

Specifications written in this manual are believed to be accurate, but are not guaranteed to be entirely free of error. Specifications in this manual may be changed for functional or performance improvements. Please make sure your manual is the latest edition.

1.2 Performance Outline

Table 1.1 lists performance outline of M16C/26A group (M16C/26A, M16C/26T) 48-pin device.

Table 1.2 lists performance outline of M16C/26A 42-pin device.

Table 1.1. Performance outline of M16C/26A group (48-pin device)(M16C/26A, M16C/26T)

Item		Performance
CPU	Number of basic instructions	91 instructions
	Shortest instruction	50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) (M16C/26A, M16C/26T(T-ver.)) 100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V) (M16C/26A) 50 ns (f(BCLK)= 20MHz, Vcc= 4.2V to 5.5V -40 to 105°C) (M16C/26T(V-ver.)) 62.5 ns (f(BCLK)= 16MHz, Vcc= 4.2V to 5.5V -40 to 125°C) (M16C/26T(V-ver.))
	Operation mode	Single chip mode
	Address space	1M byte
	Memory capacity	ROM/RAM : See the product list
Peripheral function	Port	Input/Output : 39 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer
	Serial I/O	2 channels (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous, I2C bus[1] , or IEBus[2])
	A/D converter	10 bit A/D Converter : 1 circuit, 12 channels
	DMAC	2 channels
	CRC calcuration circuit	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	20 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits Main clock(*), Sub-clock(*) On-chip oscillator, PLL frequency synthesizer (*)These circuit contain a built-in feedback resister.
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function
	Low voltage detection circuit	Available (M16C/26A) Not available (M16C/26T)
Electrical Characteristics	Power supply voltage	Vcc=3.0V to 5.5V (f(BCLK)=20MHz) (M16C/26A) Vcc=2.7V to 5.5V (f(BCLK)=10MHz)
		Vcc=3.0V to 5.5V (M16C/26T(T-ver.))
		Vcc=4.2V to 5.5V (M16C/26T(V-ver.))
	Power consumption	16mA (Vcc=5V, f(BCLK)=20MHz) 25 µA (Vcc=3V, f(BCLK)=f(XCIN)=32KHz on RAM) 1.8 µA (Vcc=3V, f(BCLK)=f(XCIN)=32KHz, in wait mode) 0.7 µA (Vcc=3V, when stop mode)
Flash memory	Program/erase voltage	2.7V to 5.5V (M16C/26A) 3.0V to 5.5V (M16C/26T(T-ver.)) 4.2V to 5.5V (M16C/26T(V-ver.))
	Number of program/erase	100 times (Block A ,Block B : 10,000 times (option[3]))
Operating ambient temperature		-20 to 85°C / -40 to 85°C [4] (M16C/26A)
		-40 to 85°C (M16C/26T(T-ver.))
		-40 to 105°C / -40 to 125°C (M16C/26T(V-ver.))
Package		48-pin plastic molded QFP

Notes:
1. I2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. If you desire this option, please so specify.
4. See Table 1.6 for the operating ambient temperature.

Table 1.2. Performance outline of M16C/26A group (42-pin device) (M16C/26A)

Item		Performance
CPU	Number of basic instructions	91 instructions
	Shortest instruction	50 ns (f(BCLK)= 20MHz, Vcc= 3.0V to 5.5V) 100 ns (f(BCLK)= 10MHz, Vcc= 2.7V to 5.5V)
	Operation mode	Single chip mode
	Address space	1M byte
	Memory capacity	ROM/RAM : See the product list
Peripheral function	Port	Input/Output : 33 lines
	Multifunction timer	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase Motor Control Timer
	Serial I/O	1 channel (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous, I^2C bus[1] , or IEBus[2])
	A/D converter	10 bit A/D Converter : 1 circuit, 10 channels
	DMAC	2 channels
	CRC calcuration circuit	2 polynomial (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	18 internal and 8 external sources, 4 software sources, 7 levels
	Clock generation circuit	4 circuits Main clock(*), Sub-clock(*) On-chip oscillator, PLL frequency synthesizer (*)These circuit contain a built-in feedback resister.
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function
	Low voltage detection circuit	Available
Electrical Characteristics	Power supply voltage	Vcc=3.0V to 5.5V (f(BCLK)=20MHz) Vcc=2.7V to 5.5V (f(BCLK)=10MHz)
	Power consumption	16mA (Vcc=5V, f(BCLK)=20MHz) 25 µA (Vcc=3V, f(BCLK)=f(X_{CIN})=32KHz on RAM) 1.8 µA (Vcc=3V, f(BCLK)=f(X_{CIN})=32KHz, in wait mode) 0.7 µA (Vcc=3V, when stop mode)
Flash memory	Program/erase voltage	2.7V to 5.5V
	Number of program/erase	100 times(all area) or 1,000 times(program ara)/10,000 times(data area)[3]
Operating ambient temperature		-20 to 85°C / -40 to 85°C [3]
Package		42-pin plastic molded SSOP

Notes:
1. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. See Table 1.6 for the number of program/erase and the operating ambient temperature.

1.3 Block Diagram

Figure 1.1 is a block diagram of the M16C/26A group, 48-pin device.

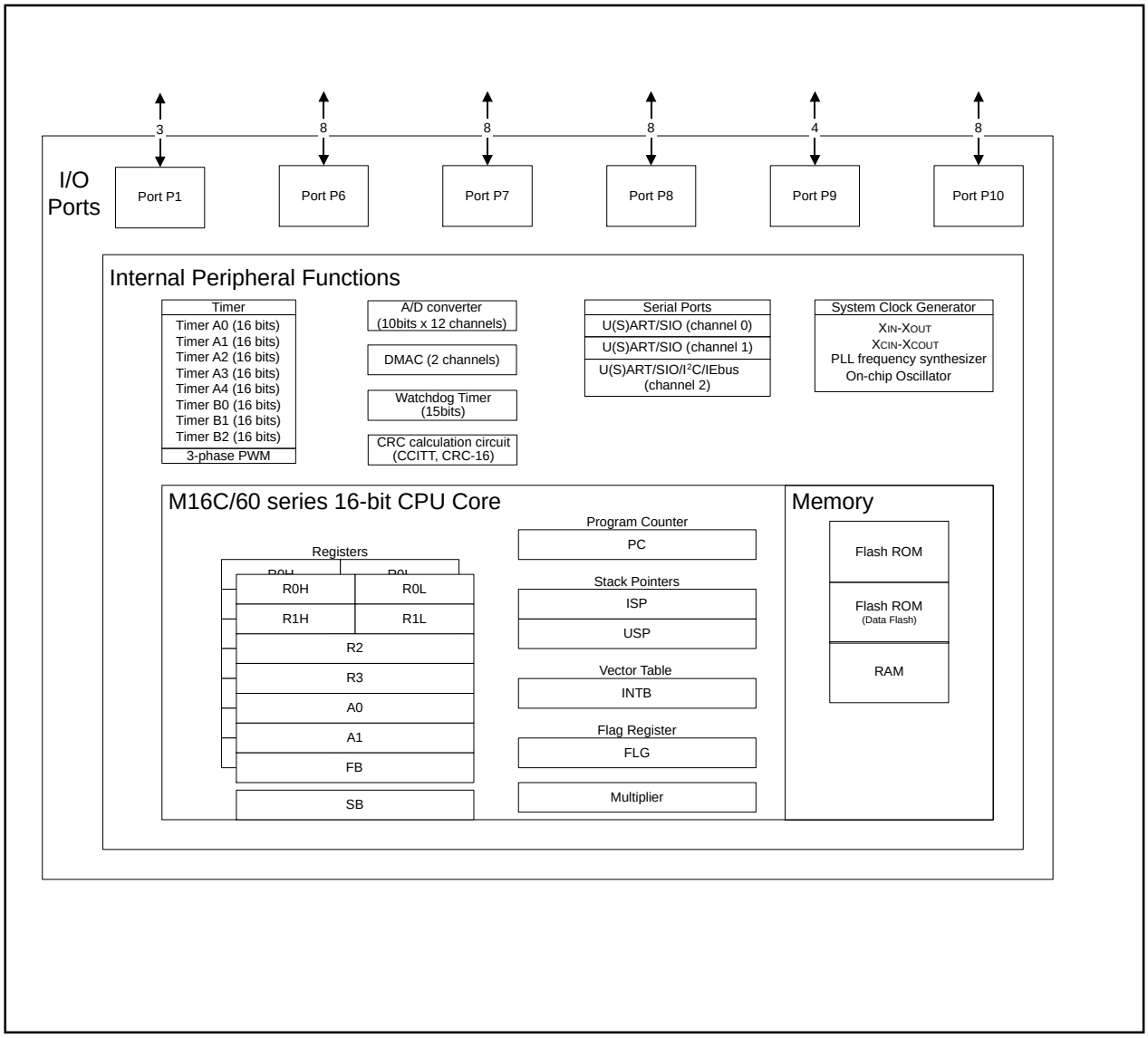


Figure 1.1. M16C/26A Group, 48-pin Block Diagram

Figure 1.2 is a block diagram of the M16C/26A group, 42-pin device.

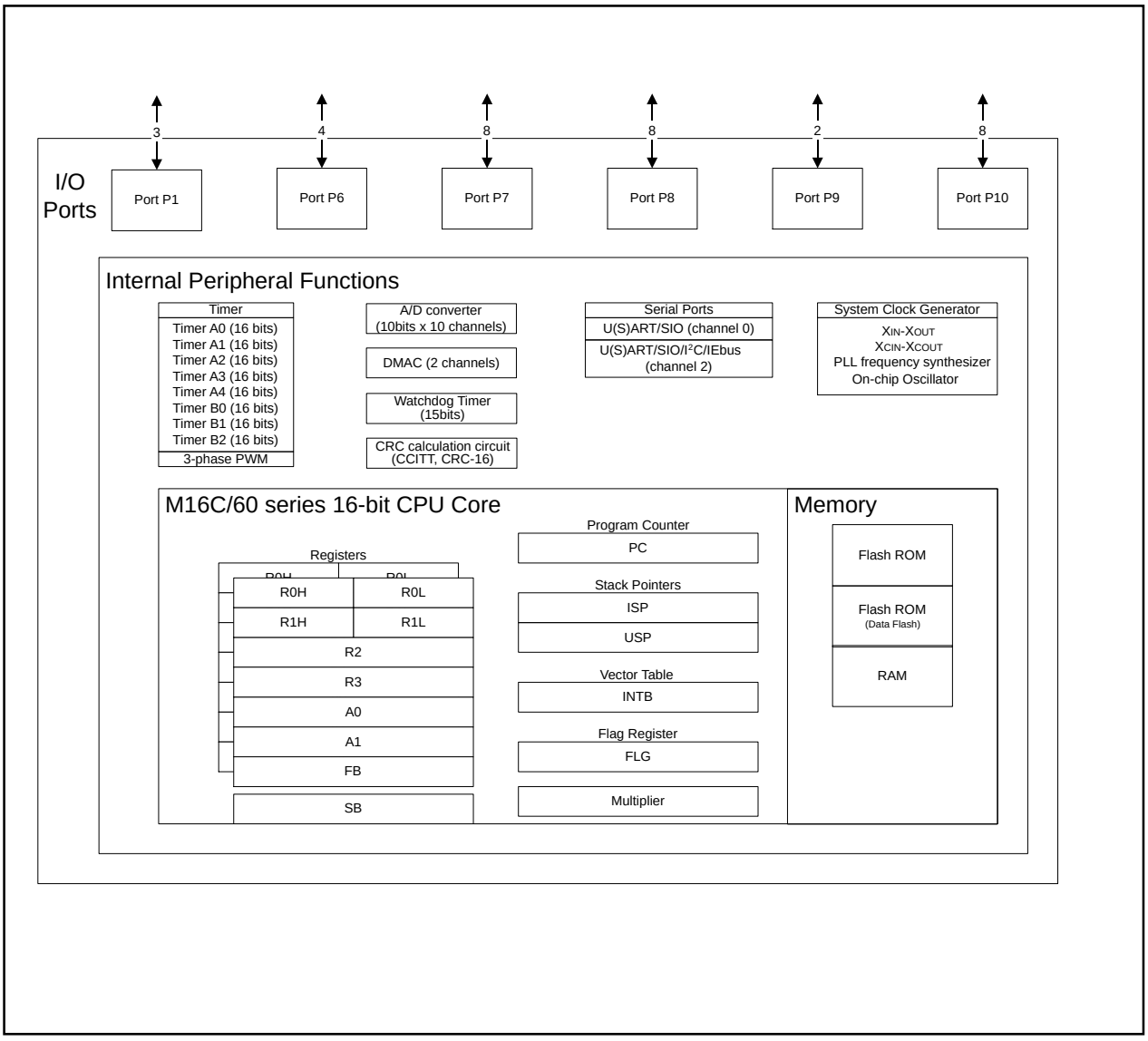


Figure 1.2. M16C/26A Group, 42-pin Block Diagram

1.4 Product List

Tables 1.3 to 1.5 list the M16C/28 group products and Figure 1.3 shows the type numbers, memory sizes and packages.

Table 1.3. Product List (1) -M16C/26A **As of Jun 2004**

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30260M3A-XXXGP (D)	24K byte	1K byte	48P6Q	Mask ROM Version
M30260M4A-XXXGP (D)	32K byte	1K byte		
M30260M6A-XXXGP (D)	48K byte	2K byte		
M30260M8A-XXXGP (D)	64K byte	2K byte		
M30263M3A-XXXFP (D)	24K byte	1K byte	42P2R	
M30263M4A-XXXFP (D)	32K byte	1K byte		
M30263M6A-XXXFP (D)	48K byte	2K byte		
M30263M8A-XXXFP (D)	64K byte	2K byte		
M30260F3AGP (D)	24K + 4K byte	1K byte	48P6Q	Flash ROM Version
M30260F4AGP (D)	32K + 4K byte	1K byte		
M30260F6AGP (D)	48K + 4K byte	2K byte		
M30260F8AGP (D)	64K + 4K byte	2K byte		
M30263F3AFP (D)	24K + 4K byte	1K byte	42P2R	
M30263F4AFP (D)	32K + 4K byte	1K byte		
M30263F6AFP (D)	48K + 4K byte	2K byte		
M30263F8AFP (D)	64K + 4K byte	2K byte		

(P) : under planning (D) : under development

Table 1.4. Product List (2) -M16C/26T T-ver. **As of Jun 2004**

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30260M3T-XXXGP (P)	24K byte	1K byte	48P6Q	Mask ROM Version
M30260M4T-XXXGP (P)	32K byte	1K byte		
M30260M6T-XXXGP (P)	48K byte	2K byte		
M30260M8T-XXXGP (P)	64K byte	2K byte		
M30260F3TGP (D)	24K + 4K byte	1K byte	48P6Q	Flash ROM Version
M30260F4TGP (D)	32K + 4K byte	1K byte		
M30260F6TGP (D)	48K + 4K byte	2K byte		
M30260F8TGP (D)	64K + 4K byte	2K byte		

(P) : under planning (D) : under development

NOTES: Specification of M16C/26T partly varies from the one of M16C/26A

Table 1.5. Product List (3) -M16C/26T V-ver. **As of Jun 2004**

Type No.	ROM capacity	RAM capacity	Package type	Remarks
M30260M3V-XXXGP (P)	24K byte	1K byte	48P6Q	Mask ROM Version
M30260M4V-XXXGP (P)	32K byte	1K byte		
M30260M6V-XXXGP (P)	48K byte	2K byte		
M30260M8V-XXXGP (P)	64K byte	2K byte		
M30260F3VGP (D)	24K + 4K byte	1K byte	48P6Q	Flash ROM Version
M30260F4VGP (D)	32K + 4K byte	1K byte		
M30260F6VGP (D)	48K + 4K byte	2K byte		
M30260F8VGP (D)	64K + 4K byte	2K byte		

(P) : under planning (D) : under development

NOTES: Specification of M16C/26T partly varies from the one of M16C/26A

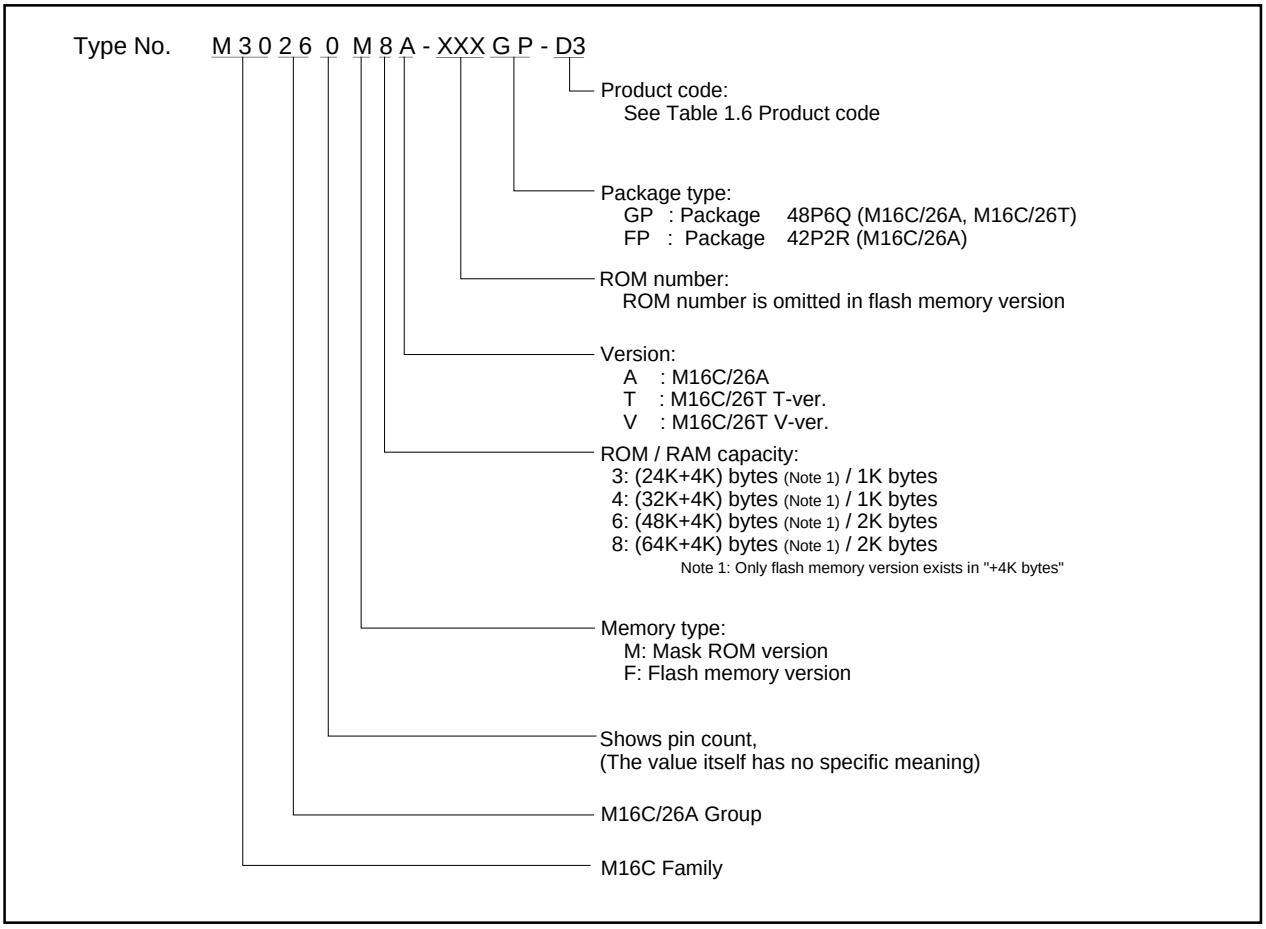


Figure 1.3. Type No., Memory Size, and Package

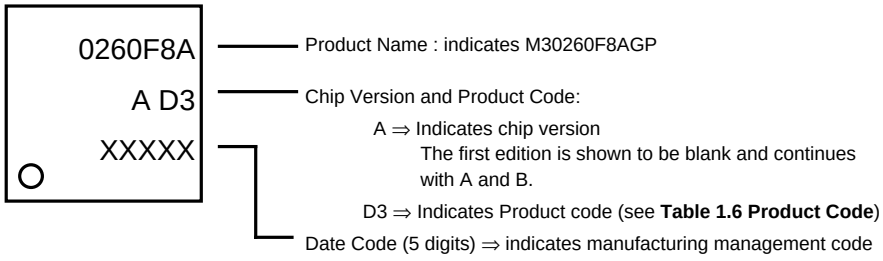
Table 1.6. Product code (Flash memory version, M16C/26A)

Product Code	Package	Internal ROM (Program area)		Internal ROM (Data area)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
D3	Lead-included	100	0°C to 60°C	100	0°C to 60°C	-40°C to 85°C
D5						-20°C to 85°C
D7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
D9					-20°C to 85°C	-20°C to 85°C
U3	Lead-free	100		100	0°C to 60°C	-40°C to 85°C
U5						-20°C to 85°C
U7		1,000		10,000	-40°C to 85°C	-40°C to 85°C
U9					-20°C to 85°C	-20°C to 85°C

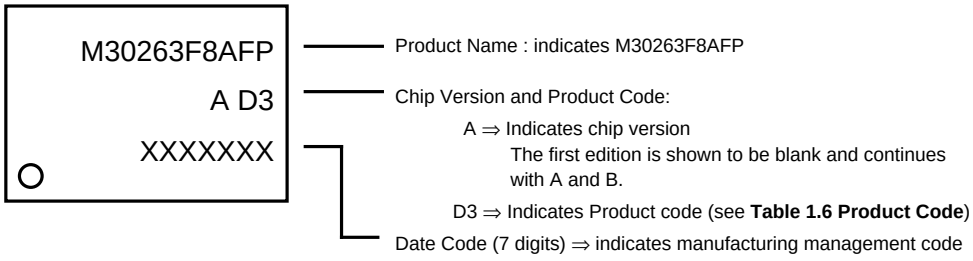
(MASK ROM version, M16C/26A)

Product Code	Package	Operating Ambient Temperature
D3	Lead-included	-40°C to 85°C
D5		-20°C to 85°C
U3	Lead-free	-40°C to 85°C
U5		-20°C to 85°C

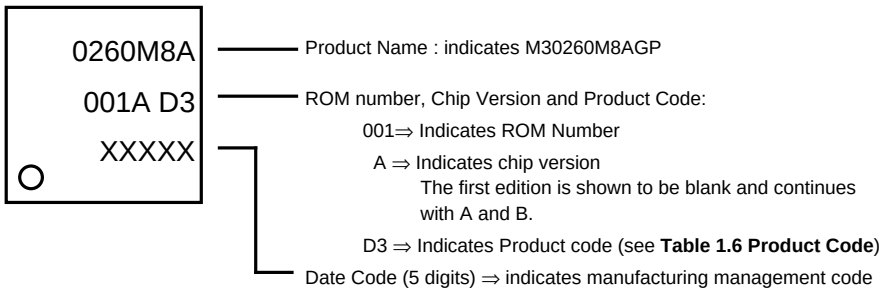
(1) Flash memory version, 48P6Q, M16C/26A



(2) Flash memory version, 42P2R, M16C/26A



(3) MASK ROM version, 48P6Q, M16C/26A



(4) MASK ROM version, 42P2R, M16C/26A

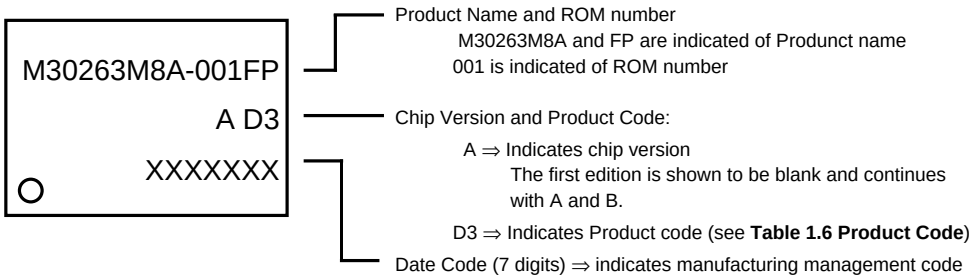


Figure 1.4. Marking Diagram of Flash Memory versionfor M16C/26A (Top View)

1.5 Pin Configuration

Figures 1.5 and 1.6 show the pin configurations (top view).

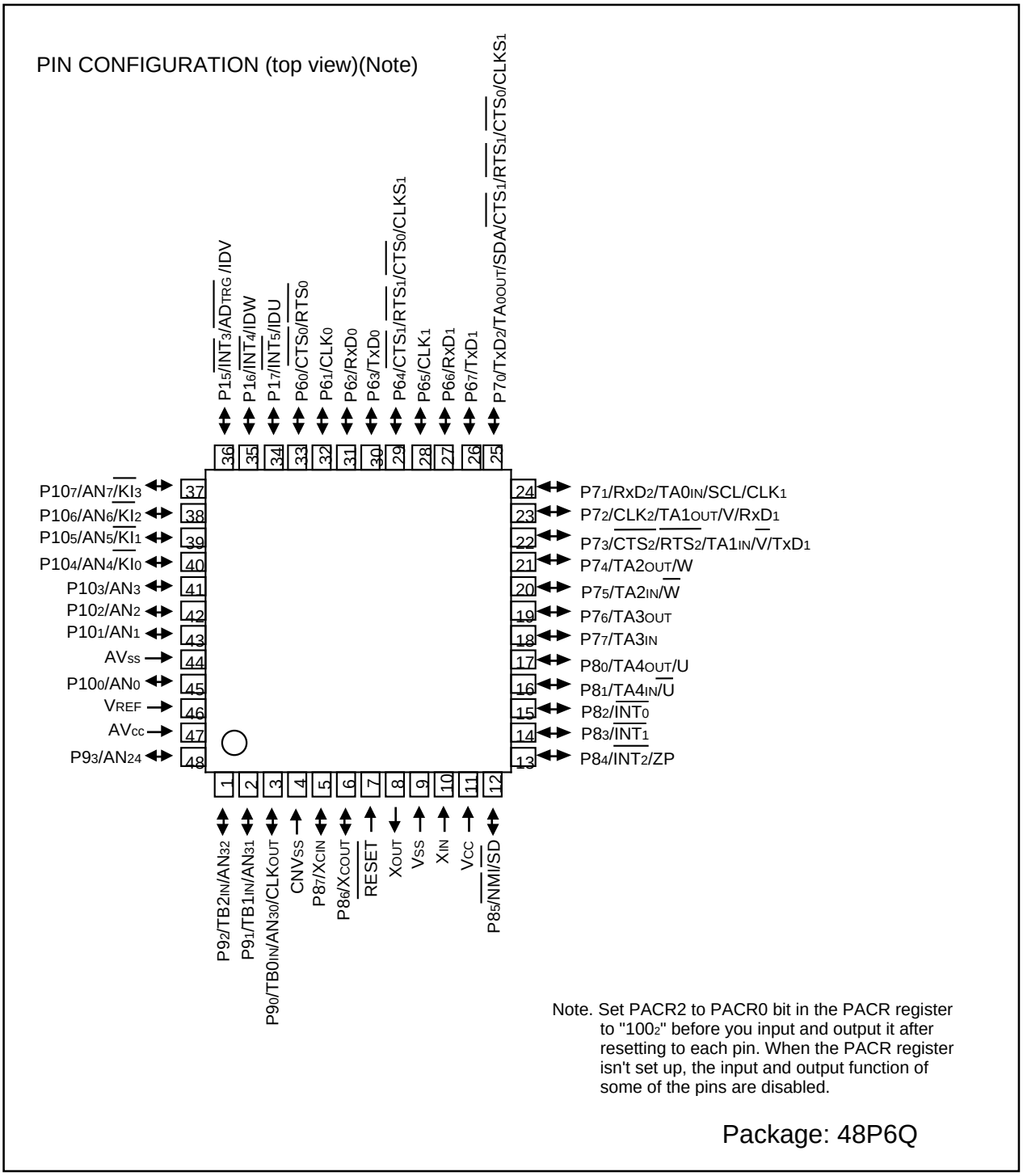
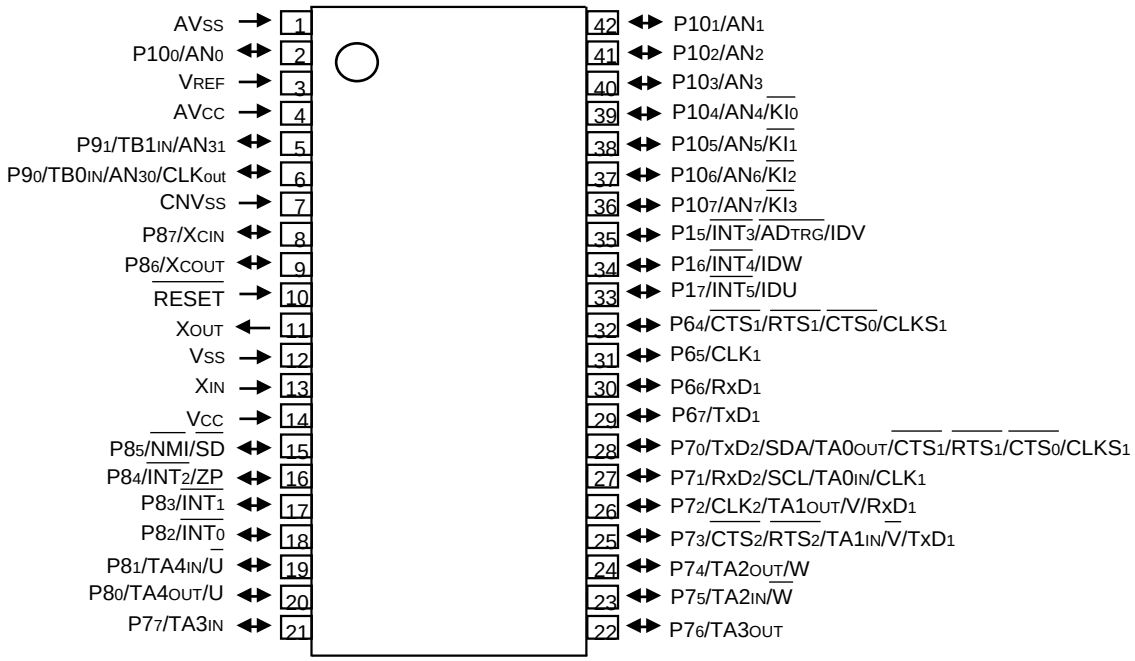


Figure 1.5. Pin Configuration (Top View) of M16C/26A Group, 48-pin Package

PIN CONFIGURATION (top view)(Note)



Note. Set PACR2 to PACR0 bit in the PACR register to "001$_2$" before you input and output it after resetting to each pin. When the PACR register isn't set up, the input and output function of some of the pins are disabled.

Package: 42P2R

Figure 1.6. Pin Configuration (Top View) of M16C/26A Group, 42-pin Package

1.6 Pin Description

Table 1.6 and 1.7 describes the available pins.

Table 1.6. Pin Description(1)

Pin name	Signal name	I/O type	Function
V_{CC},V_{SS}	Power supply input		Apply 0V to the Vss pin, and the following voltage to the Vcc pin. 2.7 to 5.5V (M16C/26A) 3.0 to 5.5V (M16C/26T T-ver.) 4.2 to 5.5V (M16C/26T V-ver.)
CNV_{SS}	CNV_{SS}	Input	Connect this pin to Vss.
$\overline{RESET}$	Reset input	Input	"L" on this input resets the microcomputer.
X_{IN} X_{OUT}	Clock input Clock output	Input Output	These pins are provided for the main clock generating circuit input/output. Connect a ceramic resonator or crystal between the X_{IN} and the X_{OUT} pins. To use an externally derived clock, input it to the X_{IN} pin and leave the X_{OUT} pin open. If X_{IN} is not used (for external oscillator or external clock) connect X_{IN} pin to V_{CC} and leave X_{OUT} pin open.
AV_{CC}	Analog power supply input		This pin is a power supply input for the A/D converter. Connect this pin to V_{CC}.
AV_{SS}	Analog power supply input		This pin is a power supply input for the A/D converter. Connect this pin to V_{SS}.
V_{REF}	Reference Voltage input	Input	This pin is a reference voltage input for the A/D converter.
$P1_5$~$P1_7$	I/O port P1	Input/ output	This is an 3-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input, a pull-up resister option can be selected for the entire group of three pins. Additional software selectable secondary functions are: 1) $P1_5$ to $P1_7$ can be configured as external $\overline{INT}$ interrupt pins; 2) $P1_5$ to $P1_7$ can be configured as position-data-retain function input pins,and; 3) $P1_5$ can input a trigger for the A/D converter.
$P6_0$~$P6_7$	I/O port P6	Input/ output	This is an 8-bit CMOS I/O port. It has an input/output port direction register that allows the user to set each pin for input or output individually. When used for input, a pull-up resister option can be selected for the entire group of four pins. Pins in this port also function as UART0 and UART1 I/O, as selected by software.$P6_0$ to $P6_3$ are not available in the 42 pin version.
$P7_0$~$P7_7$	I/O port P7	Input/ output	This is an 8-bit I/O port equivalent to P6. P7 can also function as I/O for timer A0 to A3, as selected by software. Additional programming options are: $P7_0$ to $P7_3$ can assume UART1 I/O or UART2 I/O capabilities, and $P7_2$ to $P7_5$ can function as output pins for the three-phase motor control timer.

Table 1.7. Pin Description(2)

Pin name	Signal name	I/O type	Function
$P8_0$~$P8_7$	I/O port P8	Input/ output	This is an 8-bit I/O port equivalent to P6. Additional software-selectable secondary functions are: 1) $P8_0$ and $P8_1$ can act as either I/O for Timer A4, or as output pins for the three-phase motor control timer; 2) $P8_2$ to $P8_4$ can be configured as external $\overline{INT}$ interrupt pins. $P8_4$ can be used for Timer A Zphase function; 3) $P8_5$ can be used as $\overline{NMI}/\overline{SD}$. $P8_5$ can not be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $P8_5$ after setting the direction register for $P8_5$ to "0" when the three-phase motor control is enabled, and; 4) $P8_6$ and $P8_7$ can serve as I/O pins for the sub-clock generation circuit. In this latter case, a quartz oscillator must be connented between $P8_6$ (X_{COUT} pin) and $P8_7$ (X_{CIN} pin).
$P9_0$~$P9_3$	I/O port P9	Input/ output	This is an 4-bit I/O port equivalent to P6. Additional software-selectable secondary functions are: 1) $P9_0$ to $P9_2$ can act as Timer B0~B2 input pins, and; 2) $P9_0$ to $P9_3$ can act as A/D converter input pins. $P9_0$ outputs a no-divide, divide-by-8 or divide-by-32 clock of X_{IN} or a clock of the same frequency as X_{CIN} as selected by program. $P9_2$ to $P9_3$ are not available in the 42 pin version.
$P10_0$~$P10_7$	I/O port P10	Input/ output	This is an 8-bit I/O port equivalent to P6. This port can also function as A/D converter input pins, as selected by software. Furthermore, $P10_4$ to $P10_7$ can also function as input pins for the key input interrupt function.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The CPU has 13 registers. Of these, R0, R1, R2, R3, A0, A1 and FB comprise a register bank. There are two register banks.

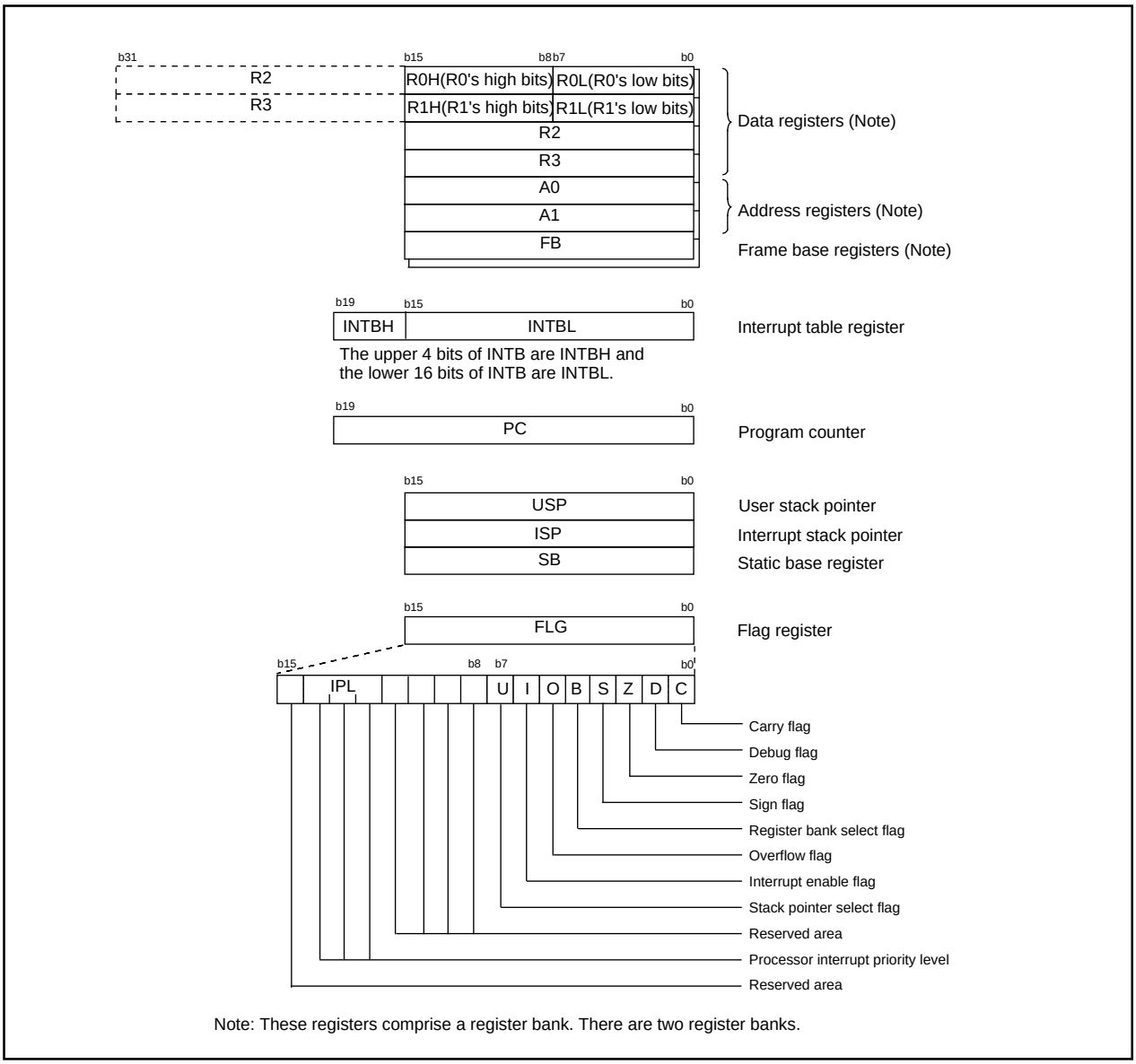


Figure 2.1. Central Processing Unit Register

2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to “0”.

2.8.3 Zero Flag (Z Flag)

This flag is set to “1” when an arithmetic operation resulted in 0; otherwise, it is “0”.

2.8.4 Sign Flag (S Flag)

This flag is set to “1” when an arithmetic operation resulted in a negative value; otherwise, it is “0”.

2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is “0” ; register bank 1 is selected when this flag is “1”.

2.8.6 Overflow Flag (O Flag)

This flag is set to “1” when the operation resulted in an overflow; otherwise, it is “0”.

2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is “0”, and are enabled when the I flag is “1”. The I flag is cleared to “0” when the interrupt request is accepted.

2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is “0”; USP is selected when the U flag is “1”.

The U flag is cleared to “0” when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

2.8.10 Reserved Area

When write to this bit, write "0". When read, its content is indeterminate.

3. Memory

Figure 3.1 is a memory map. The linear address space of 1M bytes extends from address 00000_{16} to $FFFFF_{16}$. The internal ROM is allocated in a lower address directiom beginning with address $FFFFF_{16}$. For example, a 64-Kbyte internal ROM is allocated to the address from $F0000_{16}$ to $FFFFF_{16}$.

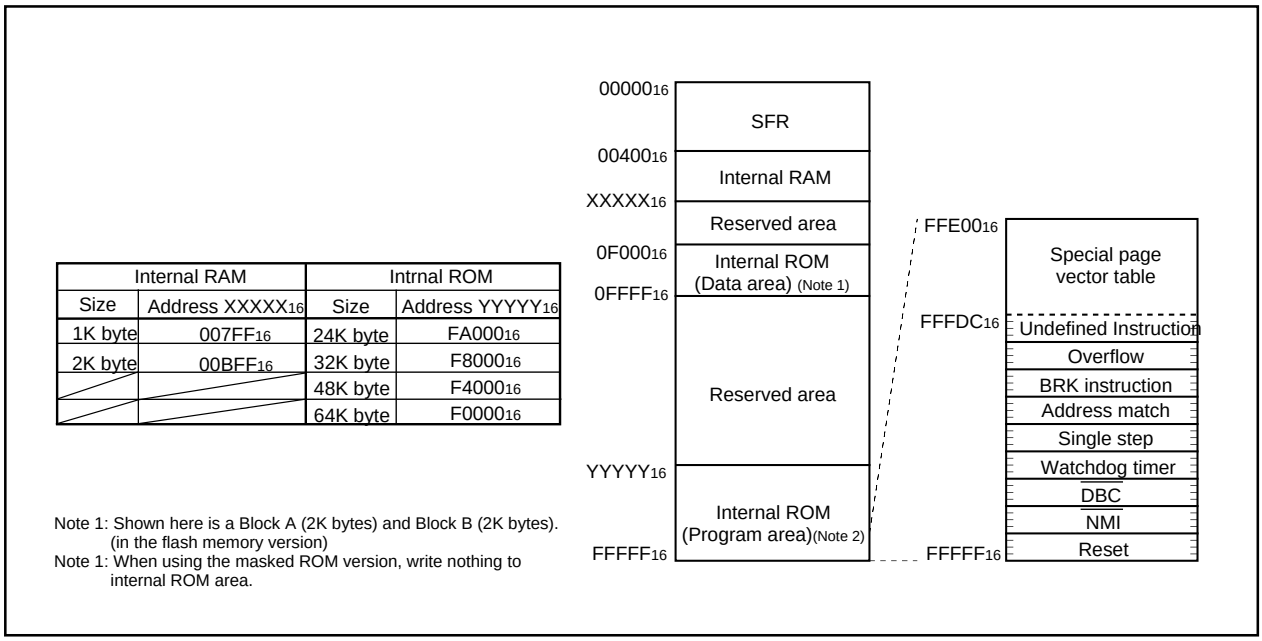
The fixed interrupt vector table is allocated to the address from $FFFDC_{16}$ to $FFFFF_{16}$. Therefore store the start address of each interrupt routine here. For details, refer to the "Interrupt".

These devices also contain two blocks of Flash ROM as Data Flash memory to store data. These two blocks of 2K bytes are located from $0F000_{16}$ to $0FFFF_{16}$ on all versions.

The internal RAM is allocated in an upper address direction beginning with address 00400_{16}. For example, a 1-Kbyte internal RAM is allocated to the address from 00400_{16} to $007FF_{16}$. In addition to storing data, the internal RAM also stores the stack used when calling subroutines and when interrupts are generated.

The SFR is allocated to the address from 00000_{16} to $003FF_{16}$. Peripheral function control registers are located here. Of the SFR, any area which has no functions allocated is reserved for future use and cannot be used by users.

The special page vector table is allocated to the addresses from $FFE00_{16}$ to $FFFDB_{16}$. This vector is used by the JMPS or JSRS instruction. For details, refer to the "M16C/60 and M16C/20 Series Software Manual".



Internal RAM		Intrnal ROM	
Size	Address XXXXX$_{16}$	Size	Address YYYYY$_{16}$
1K byte	007FF$_{16}$	24K byte	FA000$_{16}$
2K byte	00BFF$_{16}$	32K byte	F8000$_{16}$
		48K byte	F4000$_{16}$
		64K byte	F0000$_{16}$

Note 1: Shown here is a Block A (2K bytes) and Block B (2K bytes). (in the flash memory version)
Note 1: When using the masked ROM version, write nothing to internal ROM area.

Figure 3.1. Memory Map

4. Special Function Register (SFR) Map

Address	Register	Symbol	After reset
0000₁₆			
0001₁₆			
0002₁₆			
0003₁₆			
0004₁₆	Processor mode register 0	PM0	00₁₆
0005₁₆	Processor mode register 1	PM1	00001000₂
0006₁₆	System clock control register 0	CM0	01001000₂
0007₁₆	System clock control register 1	CM1	00100000₂
0008₁₆			
0009₁₆	Address match interrupt enable register	AIER	XXXXXX00₂
000A₁₆	Protect register	PBCR	XX000000₂
000B₁₆			
000C₁₆	Oscillation stop detection register (Note 2)	CM2	0X000010₂
000D₁₆			
000E₁₆	Watchdog timer start register	WDTS	??₁₆
000F₁₆	Watchdog timer control register	WDC	00??????₂(Note3)
0010₁₆	Address match interrupt register 0	RMAD0	00₁₆
0011₁₆			00₁₆
0012₁₆			X0₁₆
0013₁₆			
0014₁₆	Address match interrupt register 1	RMAD1	00₁₆
0015₁₆			00₁₆
0016₁₆			X0₁₆
0017₁₆			
0018₁₆			
0019₁₆	Voltage detection register 1 (Note 4,5)	VCR1	00001000₂
001A₁₆	Voltage detection register 2 (Note 4,5)	VCR2	00₁₆
001B₁₆			
001C₁₆	PLL control register 0	PLC0	0001X010₂
001D₁₆			
001E₁₆	Processor mode register 2	PM2	XXX00000₂
001F₁₆	Power supply down detection interrupt register (Note 5)	D4INT	00₁₆
0020₁₆	DMA0 source pointer	SAR0	??₁₆
0021₁₆			??₁₆
0022₁₆			X?₁₆
0023₁₆			
0024₁₆	DMA0 destination pointer	DAR0	??₁₆
0025₁₆			??₁₆
0026₁₆			X?₁₆
0027₁₆			
0028₁₆	DMA0 transfer counter	TCR0	??₁₆
0029₁₆			??₁₆
002A₁₆			
002B₁₆			
002C₁₆	DMA0 control register	DM0CON	00000?00₂
002D₁₆			
002E₁₆			
002F₁₆			
0030₁₆	DMA1 source pointer	SAR1	??₁₆
0031₁₆			??₁₆
0032₁₆			X?₁₆
0033₁₆			
0034₁₆	DMA1 destination pointer	DAR1	??₁₆
0035₁₆			??₁₆
0036₁₆			X?₁₆
0037₁₆			
0038₁₆	DMA1 transfer counter	TCR1	??₁₆
0039₁₆			??₁₆
003A₁₆			
003B₁₆			
003C₁₆	DMA1 control register	DM1CON	00000?00₂
003D₁₆			
003E₁₆			
003F₁₆			

Note 1: The blank areas are reserved and cannot be used by users.
Note 2: The CM20, CM21 and CM27 bits do not change at oscillation stop detection reset..
Note 3: The WDC5 bit is "0" (cold start) immediately after power-on. It can only be set to "1" in a program.
It is set to "0" when the input voltage at the VCC pin drops to Vdet2 or less while the VC25 bit in the VCR2 register is set to "1" (2V detection circuit enable).
Note 4: This register does not change at software reset, watchdog timer reset and oscillation stop detection reset.
Note 5: This register can not use for M16C/26T
X : Nothing is mapped to this bit
? : Undefined

Address	Register	Symbol	After reset
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆	INT3 interrupt control register	INT3IC	XX00?000₂
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆	INT5 interrupt control register	INT5IC	XX00?000₂
0049₁₆	INT4 interrupt control register	INT4IC	XX00?000₂
004A₁₆	UART2 Bus collision detection interrupt control register	BCNIC	XXXX?000₂
004B₁₆	DMA0 interrupt control register	DM0IC	XXXX?000₂
004C₁₆	DMA1 interrupt control register	DM1IC	XXXX?000₂
004D₁₆	Key input interrupt control register	KUPIC	XXXX?000₂
004E₁₆	A/D conversion interrupt control register	ADIC	XXXX?000₂
004F₁₆	UART2 transmit interrupt control register	S2TIC	XXXX?000₂
0050₁₆	UART2 receive interrupt control register	S2RIC	XXXX?000₂
0051₁₆	UART0 transmit interrupt control register	S0TIC	XXXX?000₂
0052₁₆	UART0 receive interrupt control register	S0RIC	XXXX?000₂
0053₁₆	UART1 transmit interrupt control register	S1TIC	XXXX?000₂
0054₁₆	UART1 receive interrupt control register	S1RIC	XXXX?000₂
0055₁₆	TimerA0 interrupt control register	TA0IC	XXXX?000₂
0056₁₆	TimerA1 interrupt control register	TA1IC	XXXX?000₂
0057₁₆	TimerA2 interrupt control register	TA2IC	XXXX?000₂
0058₁₆	TimerA3 interrupt control register	TA3IC	XXXX?000₂
0059₁₆	TimerA4 interrupt control register	TA4IC	XXXX?000₂
005A₁₆	TimerB0 interrupt control register	TB0IC	XXXX?000₂
005B₁₆	TimerB1 interrupt control register	TB1IC	XXXX?000₂
005C₁₆	TimerB2 interrupt control register	TB2IC	XXXX?000₂
005D₁₆	INT0 interrupt control register	INT0IC	XX00?000₂
005E₁₆	INT1 interrupt control register	INT1IC	XX00?000₂
005F₁₆	INT2 interrupt control register	INT2IC	XX00?000₂
0060₁₆			
0061₁₆			
0062₁₆			
0063₁₆			
0064₁₆			
0065₁₆			
0066₁₆			
0067₁₆			
0068₁₆			
0069₁₆			
006A₁₆			
006B₁₆			
006C₁₆			
006D₁₆			
006E₁₆			
006F₁₆			
0070₁₆			
0071₁₆			
0072₁₆			
0073₁₆			
0074₁₆			
0075₁₆			
0076₁₆			
0077₁₆			
0078₁₆			
0079₁₆			
007A₁₆			
007B₁₆			
007C₁₆			
007D₁₆			
007E₁₆			
007F₁₆			

Note 1: The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Address	Register	Symbol	After reset
0080₁₆			
0081₁₆			
0082₁₆			
0083₁₆			
0084₁₆			
0085₁₆			
0086₁₆			
≈			
01B0₁₆			
01B1₁₆			
01B2₁₆			
01B3₁₆	Flash memory control register 4 (Note 2)	FMR4	01000000₂
01B4₁₆			
01B5₁₆	Flash memory control register 1 (Note 2)	FMR1	000???0?₂
01B6₁₆			
01B7₁₆	Flash memory control register 0 (Note 2)	FMR0	01₁₆
01B8₁₆			
01B9₁₆			
01BA₁₆			
01BB₁₆			
01BC₁₆			
01BD₁₆			
01BE₁₆			
01BF₁₆			
≈			
0250₁₆			
0251₁₆			
0252₁₆			
0253₁₆			
0254₁₆			
0255₁₆			
0256₁₆			
0257₁₆			
0258₁₆			
0259₁₆			
025A₁₆	Three phase protect control register	TPRC	00₁₆
025B₁₆			
025C₁₆	On-chip oscillator control register	ROCR	00000101₂
025D₁₆	Pin assignment control register	PACR	00₁₆
025E₁₆	Peripheral clock select register	PCLKR	00000011₂
025F₁₆			
≈			
0330₁₆			
0331₁₆			
0332₁₆			
0333₁₆			
0334₁₆			
0335₁₆			
0336₁₆			
0337₁₆			
0338₁₆			
0339₁₆			
033A₁₆			
033B₁₆			
033C₁₆			
033D₁₆			
033E₁₆	NMI digital debounce register	NDDR	FF₁₆
033F₁₆	Port1₇ digital debounce register	P17DDR	FF₁₆

Note 1: The blank areas are reserved and cannot be used by users.
Note 2: This register is included in the flash memory version.

X :Nothing is mapped to this bit
? : Undefined

Address	Register	Symbol	After reset
0340$_{16}$			
0341$_{16}$			
0342$_{16}$	Timer A1-1 register	TA11	??$_{16}$
0343$_{16}$			??$_{16}$
0344$_{16}$	Timer A2-1 register	TA21	??$_{16}$
0345$_{16}$			??$_{16}$
0346$_{16}$	Timer A4-1 register	TA41	??$_{16}$
0347$_{16}$			??$_{16}$
0348$_{16}$	Three phase PWM control register 0	INVC0	00$_{16}$
0349$_{16}$	Three phase PWM control register 1	INVC1	00$_{16}$
034A$_{16}$	Three phase output buffer register 0	IDB0	00$_{16}$
034B$_{16}$	Three phase output buffer register 1	IDB1	00$_{16}$
034C$_{16}$	Dead time timer	DTT	??$_{16}$
034D$_{16}$	Timer B2 Interrupt occurrence frequency set counter	ICTB2	X?$_{16}$
034E$_{16}$	Position-data-retain function control register	PDRF	XXXX0000$_2$
034F$_{16}$			
0350$_{16}$			
0351$_{16}$			
0352$_{16}$			
0353$_{16}$			
0354$_{16}$			
0355$_{16}$			
0356$_{16}$			
0357$_{16}$			
0358$_{16}$	Port function control register	PFCR	00111111$_2$
0359$_{16}$			
035A$_{16}$			
035B$_{16}$			
035C$_{16}$			
035D$_{16}$			
035E$_{16}$	Interrupt request cause select register 2	IFSR2A	XXXXXXX0$_2$
035F$_{16}$	Interrupt request cause select register	IFSR	00$_{16}$
0360$_{16}$			
0361$_{16}$			
0362$_{16}$			
0363$_{16}$			
0364$_{16}$			
0365$_{16}$			
0366$_{16}$			
0367$_{16}$			
0368$_{16}$			
0369$_{16}$			
036A$_{16}$			
036B$_{16}$			
036C$_{16}$			
036D$_{16}$			
036E$_{16}$			
036F$_{16}$			
0370$_{16}$			
0371$_{16}$			
0372$_{16}$			
0373$_{16}$			
0374$_{16}$	UART2 special mode register 4	U2SMR4	00$_{16}$
0375$_{16}$	UART2 special mode register 3	U2SMR3	000X0X0X$_2$
0376$_{16}$	UART2 special mode register 2	U2SMR2	X0000000$_2$
0377$_{16}$	UART2 special mode register	U2SMR	X0000000$_2$
0378$_{16}$	UART2 transmit/receive mode register	U2MR	00$_{16}$
0379$_{16}$	UART2 bit rate register	U2BRG	??$_{16}$
037A$_{16}$	UART2 transmit buffer register	U2TB	????????$_2$
037B$_{16}$			XXXXXXX?$_2$
037C$_{16}$	UART2 transmit/receive control register 0	U2C0	00001000$_2$
037D$_{16}$	UART2 transmit/receive control register 1	U2C1	00000010$_2$
037E$_{16}$	UART2 receive buffer register	U2RB	????????$_2$
037F$_{16}$			?????XX?$_2$

Note 1 :The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Address	Register	Symbol	After reset
0380$_{16}$	Count start flag	TABSR	00$_{16}$
0381$_{16}$	Clock prescaler reset flag	CPSRF	0XXXXXXX$_2$
0382$_{16}$	One-shot start flag	ONSF	00$_{16}$
0383$_{16}$	Trigger select register	TRGSR	00$_{16}$
0384$_{16}$	Up-dowm flag	UDF	00$_{16}$
0385$_{16}$			
0386$_{16}$ 0387$_{16}$	Timer A0 register	TA0	??$_{16}$??$_{16}$
0388$_{16}$ 0389$_{16}$	Timer A1 register	TA1	??$_{16}$??$_{16}$
038A$_{16}$ 038B$_{16}$	Timer A2 register	TA2	??$_{16}$??$_{16}$
038C$_{16}$ 038D$_{16}$	Timer A3 register	TA3	??$_{16}$??$_{16}$
038E$_{16}$ 038F$_{16}$	Timer A4 register	TA4	??$_{16}$??$_{16}$
0390$_{16}$ 0391$_{16}$	Timer B0 register	TB0	??$_{16}$??$_{16}$
0392$_{16}$ 0393$_{16}$	Timer B1 register	TB1	??$_{16}$??$_{16}$
0394$_{16}$ 0395$_{16}$	Timer B2 register	TB2	??$_{16}$??$_{16}$
0396$_{16}$	Timer A0 mode register	TA0MR	00$_{16}$
0397$_{16}$	Timer A1 mode register	TA1MR	00$_{16}$
0398$_{16}$	Timer A2 mode register	TA2MR	00$_{16}$
0399$_{16}$	Timer A3 mode register	TA3MR	00$_{16}$
039A$_{16}$	Timer A4 mode register	TA4MR	00$_{16}$
039B$_{16}$	Timer B0 mode register	TB0MR	00??0000$_2$
039C$_{16}$	Timer B1 mode register	TB1MR	00?X0000$_2$
039D$_{16}$	Timer B2 mode register	TB2MR	00?X0000$_2$
039E$_{16}$	Timer B2 special mode register	TB2SC	X0000000$_2$
039F$_{16}$			
03A0$_{16}$	UART0 transmit/receive mode register	U0MR	00$_{16}$
03A1$_{16}$	UART0 bit rate register	U0BRG	??$_{16}$
03A2$_{16}$ 03A3$_{16}$	UART0 transmit buffer register	U0TB	????????$_2$ XXXXXXX?$_2$
03A4$_{16}$	UART0 transmit/receive control register 0	U0C0	00001000$_2$
03A5$_{16}$	UART0 transmit/receive control register 1	U0C1	00000010$_2$
03A6$_{16}$ 03A7$_{16}$	UART0 receive buffer register	U0RB	????????$_2$?????XX?$_2$
03A8$_{16}$	UART1 transmit/receive mode register	U1MR	00$_{16}$
03A9$_{16}$	UART1 bit rate register	U1BRG	??$_{16}$
03AA$_{16}$ 03AB$_{16}$	UART1 transmit buffer register	U1TB	????????$_2$ XXXXXXX?$_2$
03AC$_{16}$	UART1 transmit/receive control register 0	U1C0	00001000$_2$
03AD$_{16}$	UART1 transmit/receive control register 1	U1C1	00000010$_2$
03AE$_{16}$ 03AF$_{16}$	UART1 receive buffer register	U1RB	????????$_2$?????XX?$_2$
03B0$_{16}$	UART transmit/receive control register 2	UCON	X0000000$_2$
03B1$_{16}$			
03B2$_{16}$			
03B3$_{16}$			
03B4$_{16}$ 03B5$_{16}$	CRC snoop address register	CRCSAR	??$_{16}$ 00XXXX??$_2$
03B6$_{16}$	CRC mode register	CRCMR	0XXXXXX0$_2$
03B7$_{16}$			
03B8$_{16}$	DMA0 request cause select register	DM0SL	00$_{16}$
03B9$_{16}$			
03BA$_{16}$	DMA1 request cause select register	DM1SL	00$_{16}$
03BB$_{16}$			
03BC$_{16}$ 03BD$_{16}$	CRC data register	CRCD	??$_{16}$??$_{16}$
03BE$_{16}$	CRC input register	CRCIN	??$_{16}$
03BF$_{16}$			

Note 1 :The blank areas are reserved and cannot be used by users.

X : Nothing is mapped to this bit
? : Undefined

Address	Register	Symbol	After reset
03C0₁₆	A/D register 0	AD0	????????₂
03C1₁₆			XXXXXX??₂
03C2₁₆	A/D register 1	AD1	????????2
03C3₁₆			XXXXXX??₂
03C4₁₆	A/D register 2	AD2	????????₂
03C5₁₆			XXXXXX??₂
03C6₁₆	A/D register 3	AD3	????????₂
03C7₁₆			XXXXXX??₂
03C8₁₆	A/D register 4	AD4	????????₂
03C9₁₆			XXXXXX??₂
03CA₁₆	A/D register 5	AD5	????????₂
03CB₁₆			XXXXXX??₂
03CC₁₆	A/D register 6	AD6	????????₂
03CD₁₆			XXXXXX??₂
03CE₁₆	A/D register 7	AD7	????????₂
03CF₁₆			XXXXXX??₂
03D0₁₆			
03D1₁₆			
03D2₁₆	A/D trigger control register	ADTRGCON	XXXX0000₂
03D3₁₆	A/D status register 0	ADSTAT0	00000X00₂
03D4₁₆	A/D control register 2	ADCON2	00₁₆
03D5₁₆			
03D6₁₆	A/D control register 0	ADCON0	00000???₂
03D7₁₆	A/D control register 1	ADCON1	00₁₆
03D8₁₆			
03D9₁₆			
03DA₁₆			
03DB₁₆			
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆			
03E1₁₆	Port P1 register	P1	??₁₆
03E2₁₆			
03E3₁₆	Port P1 direction register	PD1	00₁₆
03E4₁₆			
03E5₁₆			
03E6₁₆			
03E7₁₆			
03E8₁₆			
03E9₁₆			
03EA₁₆			
03EB₁₆			
03EC₁₆	Port P6 register	P6	??₁₆
03ED₁₆	Port P7 register	P7	??₁₆
03EE₁₆	Port P6 direction register	PD6	00₁₆
03EF₁₆	Port P7 direction register	PD7	00₁₆
03F0₁₆	Port P8 register	P8	??₁₆
03F1₁₆	Port P9 register	P9	???X????₂
03F2₁₆	Port P8 direction register	PD8	00₁₆
03F3₁₆	Port P9 direction register	PD9	000X0000₂
03F4₁₆	Port P10 register	P10	??₁₆
03F5₁₆			
03F6₁₆	Port P10 direction register	PD10	00₁₆
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆	Pull-up control register 0	PUR0	00₁₆
03FD₁₆	Pull-up control register 1	PUR1	00₁₆
03FE₁₆	Pull-up control register 2	PUR2	00₁₆
03FF₁₆	Port control register	PCR	00₁₆

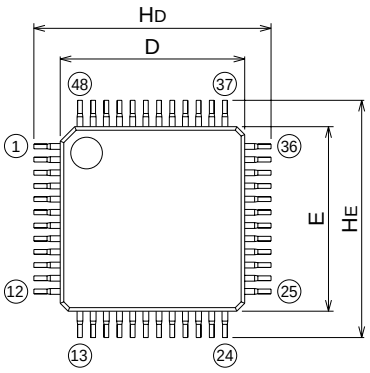
Note 1 :The blank areas are reserved and cannot be used by users.
X : Nothing is mapped to this bit
? : Undefined

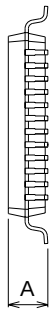
5. Package

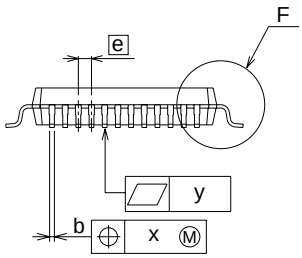
48P6Q-A Recommended

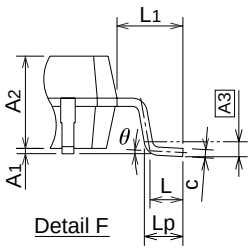
Plastic 48pin 7×7mm body LQFP

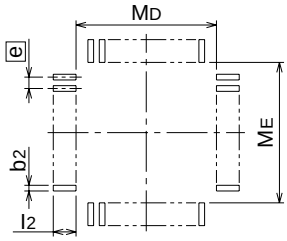
EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
LQFP48-P-77-0.50	–	–	Cu Alloy











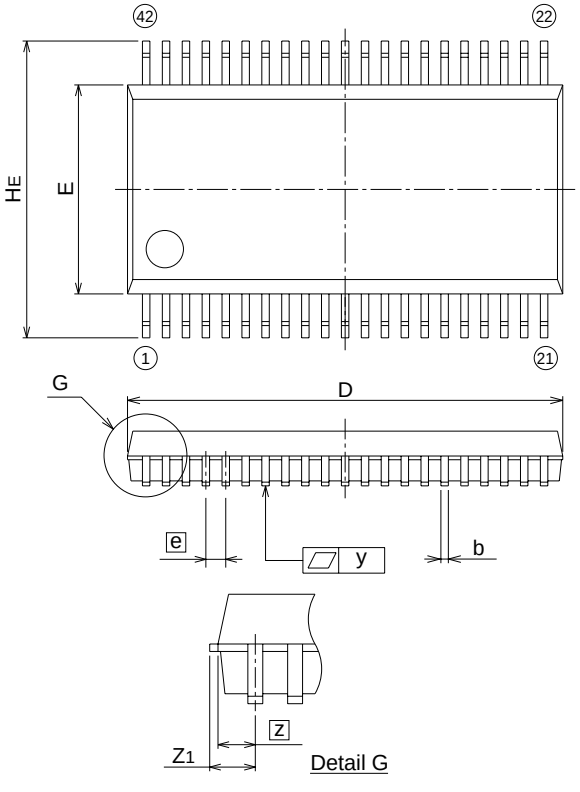
Recommended Mount Pad

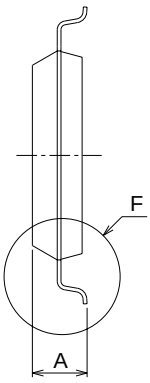
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	1.7
A1	0	0.1	0.2
A2	–	1.4	–
b	0.17	0.22	0.27
c	0.105	0.125	0.175
D	6.9	7.0	7.1
E	6.9	7.0	7.1
e	–	0.5	–
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
L	0.35	0.5	0.65
L1	–	1.0	–
Lp	0.45	0.6	0.75
A3	–	0.25	–
x	–	–	0.08
y	–	–	0.1
θ	0°	–	8°
b2	–	0.225	–
I2	1.0	–	–
MD	–	7.4	–
ME	–	7.4	–

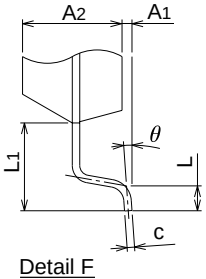
42P2R-E Recommended

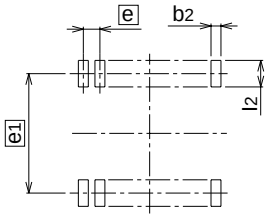
Plastic 42pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP42-P-450-0.80	–	–	Cu Alloy+42 Alloy









Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A1	0.05	–	–
A2	–	2.0	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	–	0.8	–
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	–	1.765	–
z	–	0.75	–
Z1	–	–	0.9
y	–	–	0.15
θ	0°	–	10°
b2	–	0.5	–
e1	–	11.43	–
I2	1.27	–	–

6. Functional differences

6.1 Functional differences between M16C/26A and M16C/26T

Item	M16C/26A	M16C/26T
Main Clock During and After Reset	Oscillating (Initial value of CM05 bit is set to “0” during and after reset)	Not oscillating (Initial value of CM05 bit is set to “1” during and after reset)
Voltage Detection Circuit (Function of 0019_{16}, $001A_{16}$, $001F_{16}$)	Available (Power supply detection register 1, Power supply detection register 2, Power supply down detection interrupt register)	Not available (Reserved register)
Package	48P6Q, 42P2R	48P6Q

Note. Since the emulator between the M16C/26A and M16C/29 group are same, all functions of M16C/29 are built in the emulator. When evaluating M16C/26A group, do not access to the SFR which is not built in M16C/26A group.
Refer to Hardware Manual about detail and electrical characteristics.

6.2 Functional differences between M16C/26A and M16C/26

Item	M16C/26A	M16C/26
Clock Generation Circuit	4 circuits (Main clock oscillation circuit, Sub clock oscillation circuit, On-chip oscillator, PLL frequency synthesizer)	3 circuits (Main clock oscillation circuit, Sub clock oscillation circuit, On-chip oscillator)
System Clock Source After Reset (Initial value of the CM21 bit in the CM2 register)	On-chip oscillator (Initial value "1" of CM21 bit)	Main clock (Initial value "0" of CM21 bit)
Internal RAM Retention limit Detection Circuit (The b5 bit in the VCR2 register)	Available (VC25 bit)	Not available (Reserved bit)
On-chip Oscillator Clock	Selectable (8MHz/1MHz/500KHz)	Fixed (1MHz)
PACR2 to PACR0 in the PACR Register	Necessary to set after reset 48pin:"100$_2$", 42pin:"001$_2$"	No PACR register
IFSR20 Bit in the IFSR2A Register	Necessary to set to "1" after reset	No IFSR2A register
External Interrupt	8 causes (INT2 added)	7 causes
13 pin (48-pin version) Function	$\overline{INT2}$/$\overline{ZP}$	IVCC
P7$_0$, P7$_1$	N-ch open drain output and CMOS output are selectable by S/W	N-ch open drain output
A/D Input Pin (48-pin version)	12 channels	8 channels
A/D Operation Mode	8 modes (single, repeat, single sweep, repeat sweep mode 0, repeat sweep mode 1, simultaneous sampling, delayed trigger mode 0, delayed trigger mode 1) 1 shunt current measurement function is available	5 modes (single, repeat, single sweep, repeat sweep mode 0, repeat sweep mode 1)
Timer B Operation Mode	5 modes (timer, event counter, pulse periods measurement, pulse width measurment, A/D trigger) 1 shunt current measurement function is available	4 modes (timer, event counter, pulse periods measurement, pulse width measurment)
CRC Calculation	Available (compatible to CRC-CCITT and CRC-16 methods)	Not available
Three-Phase Motor Control	•Waveform output/Switching port output by software is enabled •Position-data-retain function	•Waveform output/Switching port output by software is disabled •No position-data-retain function
Digital Debounce Function	This function is in the $\overline{NMI}$/$\overline{SD}$ pin and $\overline{INT5}$ pin	Not available
3 pin (48-pin version) Function	P9$_0$/CLKOUT/TB0IN/AN3$_0$ (CLKOUT: f1, f8, f32, and fC output)	P9$_0$/TB0IN
UART1 Compatible Pin	Switching to P6$_4$ to P6$_7$ or P7$_0$ to P7$_3$ is enabled	P6$_4$ to P6$_7$
Flash Memory Protect Function	Protection to blocks 0, 1 by FMR02 bit Protection to the blocks 0 to 3 by FMR16 bit	Protection to blocks 0,1 by FMR02 bit
Package	48P6Q, 42P2R	48P6Q

Note. Since the emulator between the M16C/26A and M16C/29 group are same, all functions of M16C/29 are built in the emulator. When evaluating M16C/26A group, do not access to the SFR which is not built in M16C/26A group.
Refer to Hardware Manual about detail and electrical characteristics.

REVISION HISTORY	M16C/26A Group (M16C/26A, M16C/26T) Short Sheet

Rev.	Date	Description	
		Page	Summary
0.20	Dec/ 01/ 03		First edition
0.30	Jun/15/04	All	Descriptions about M16C/26A and M16C/26AT are added.
		1	The section “1. Overview” is partly revised.
		2,3	Table 1.1 and 1.2 are partly revised. Note 2 in Table 1.1 and 1.2 are revised.
		4,5	Figure 1.1 and 1.2 integrate descriptions.
		6	The section “1.4 Product List” is partly revised.
		7	Table 1.6 “Porduct code” is added.
		8	Figure 1.4 “Marking Diagram of Flash Memory versionfor M16C/26A (Top View) ” is added
		9,10	Figure 1.5 to 1.6 are partly revised.
		11	Table 1.6 is revised.
		12	Table 1.7 is partly revised.
		15	The Chapter ”3. Memory” is partly revised. Note 2 in Figure 3.1 is added.
		16	The Chapter “4. Special Function Register” is partly revised.
		23, 24	The Chaplte “6. Functional differences” is added.
0.40	Sep/30/04	All	M16C/26AT is changed to M16C/26T.

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