

# MOS FIELD EFFECT TRANSISTORS

## 2SK2499, 2SK2499-Z

### SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### DESCRIPTION

The 2SK2499 is N-Channel MOS Field Effect Transistor designed for high current switching applications.

#### FEATURES

- Low On-Resistance  
 $R_{DS(on)1} = 9 \text{ m}\Omega$  ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 25 \text{ A}$ )  
 $R_{DS(on)2} = 14 \text{ m}\Omega$  ( $V_{GS} = 4 \text{ V}$ ,  $I_D = 25 \text{ A}$ )
- Low  $C_{iss}$   $C_{iss} = 3400 \text{ pF TYP.}$
- High Avalanche Capability.
- Built-in G-S Protection Diode

#### ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ )

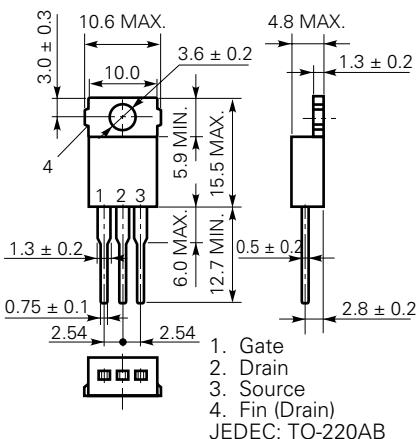
Drain to Source Voltage	$V_{DSS}$	60	V
Gate to Source Voltage	$V_{GSS}$	$\pm 20$	V
Drain Current (DC)	$I_{D(DC)}$	$\pm 50$	A
Drain Current (pulse)*	$I_{D(\text{pulse})}$	$\pm 200$	A
Total Power Dissipation ( $T_c = 25^\circ\text{C}$ )	$P_{T1}$	75	W
Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )	$P_{T2}$	1.5	W
Channel Temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$
Single Avalanche Current**	$I_{AS}$	50	A
Single Avalanche Energy**	$E_{AS}$	250	mJ

\* PW  $\leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$

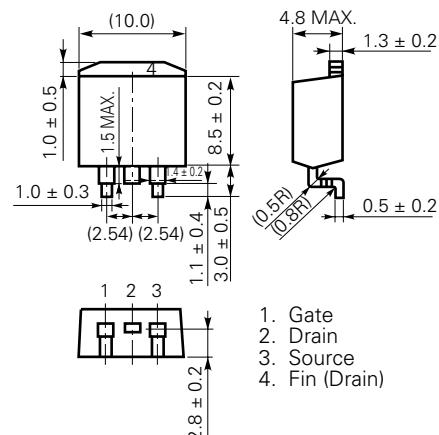
\*\* Starting  $T_{ch} = 25^\circ\text{C}$ ,  $R_G = 25 \Omega$ ,  $V_{GS} = 20 \text{ V} \rightarrow 0$

#### PACKAGE DIMENSIONS

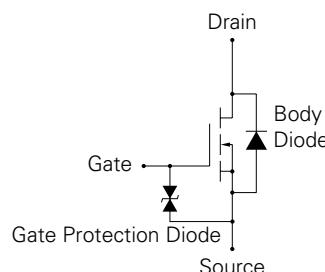
(in millimeters)



#### MP-25 (TO-220)



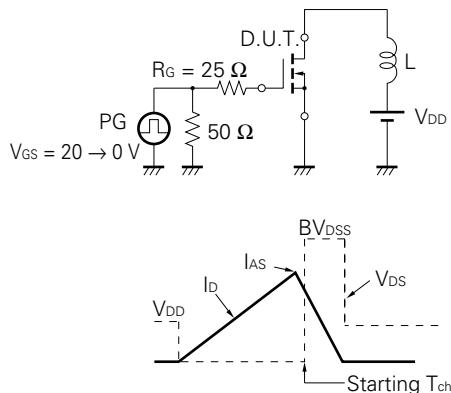
#### MP-25Z (SURFACE MOUNT TYPE)



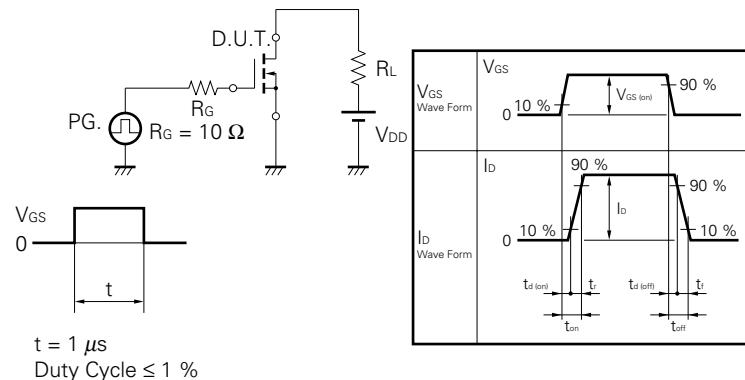
ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-State Resistance	$R_{DS(on)1}$		7.3	9.0	$\text{m}\Omega$	$V_{GS} = 10 \text{ V}, I_D = 25 \text{ A}$
	$R_{DS(on)2}$		11	14	$\text{m}\Omega$	$V_{GS} = 4 \text{ V}, I_D = 25 \text{ A}$
Gate to Source Cutoff Voltage	$V_{GS(\text{off})}$	1.0	1.5	2.0	$\text{V}$	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Forward Transfer Admittance	$ y_{fs} $	20	58		$\text{S}$	$V_{DS} = 10 \text{ V}, I_D = 25 \text{ A}$
Drain Leakage Current	$I_{DSS}$			10	$\mu\text{A}$	$V_{DS} = 60 \text{ V}, V_{GS} = 0$
Gate to Source Leakage Current	$I_{GS}$			$\pm 10$	$\mu\text{A}$	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Input Capacitance	$C_{iss}$		3 400		$\text{pF}$	$V_{DS} = 10 \text{ V}$
Output Capacitance	$C_{oss}$		1 600		$\text{pF}$	$V_{GS} = 0$
Reverse Transfer Capacitance	$C_{rss}$		770		$\text{pF}$	$f = 1 \text{ MHz}$
Turn-On Delay Time	$t_{d(on)}$		55		$\text{ns}$	$I_D = 25 \text{ A}$
Rise Time	$t_r$		360		$\text{ns}$	$V_{GS(on)} = 10 \text{ V}$
Turn-Off Delay Time	$t_{d(off)}$		480		$\text{ns}$	$V_{DD} = 30 \text{ V}$
Fall Time	$t_f$		360		$\text{ns}$	$R_G = 10 \Omega$
Total Gate Charge	$Q_G$		152		$\text{nC}$	$I_D = 50 \text{ A}$
Gate to Source Charge	$Q_{GS}$		11		$\text{nC}$	$V_{DD} = 48 \text{ V}$
Gate to Drain Charge	$Q_{GD}$		60		$\text{nC}$	$V_{GS} = 10 \text{ V}$
Body Diode Forward Voltage	$V_{F(S-D)}$		0.92		$\text{V}$	$I_F = 50 \text{ A}, V_{GS} = 0$
Reverse Recovery Time	$t_{rr}$		105		$\text{ns}$	$I_F = 50 \text{ A}, V_{GS} = 0$
Reverse Recovery Charge	$Q_{rr}$		265		$\text{nC}$	$di/dt = 100 \text{ A}/\mu\text{s}$

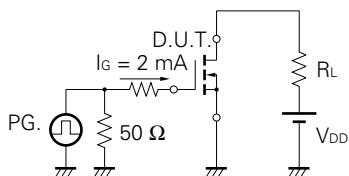
## Test Circuit 1 Avalanche Capability



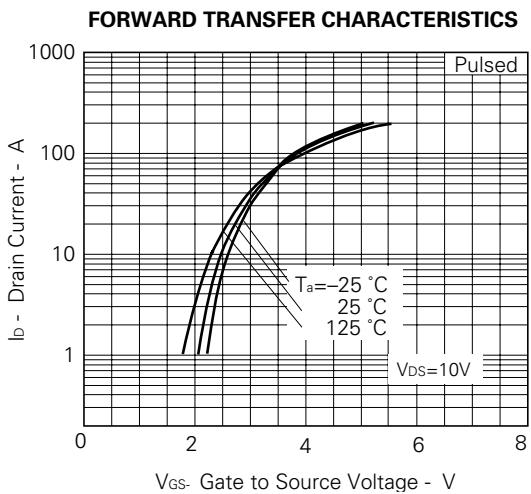
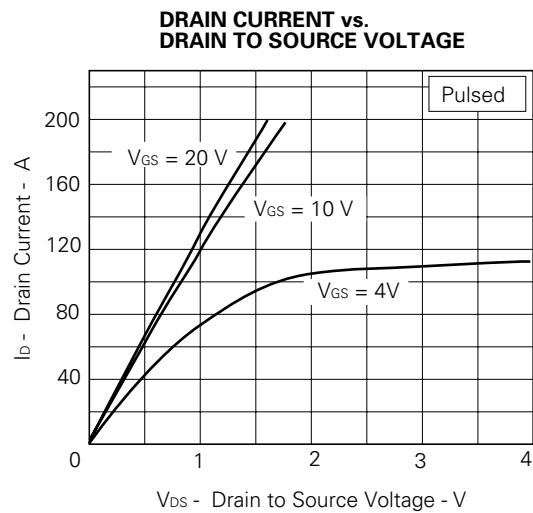
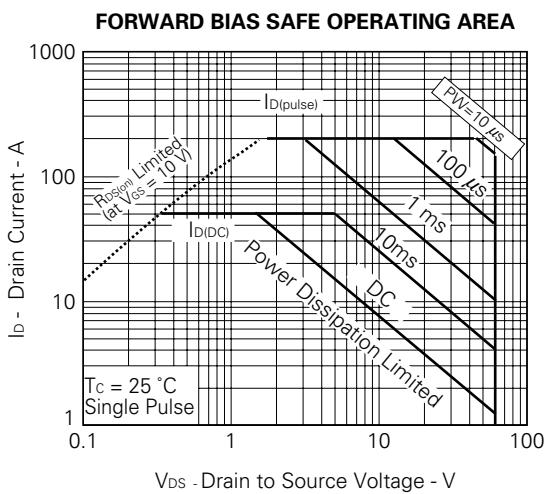
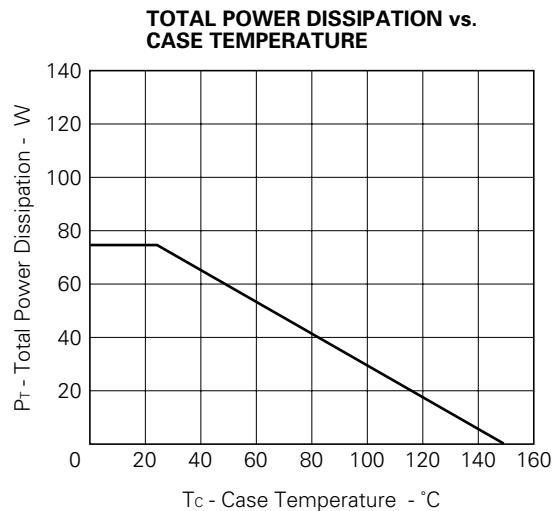
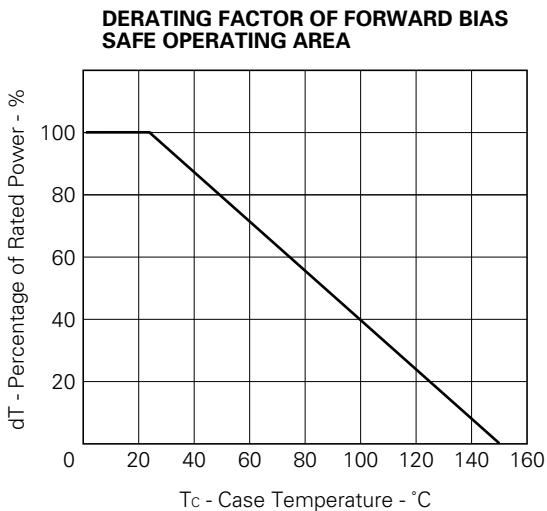
## Test Circuit 2 Switching Time



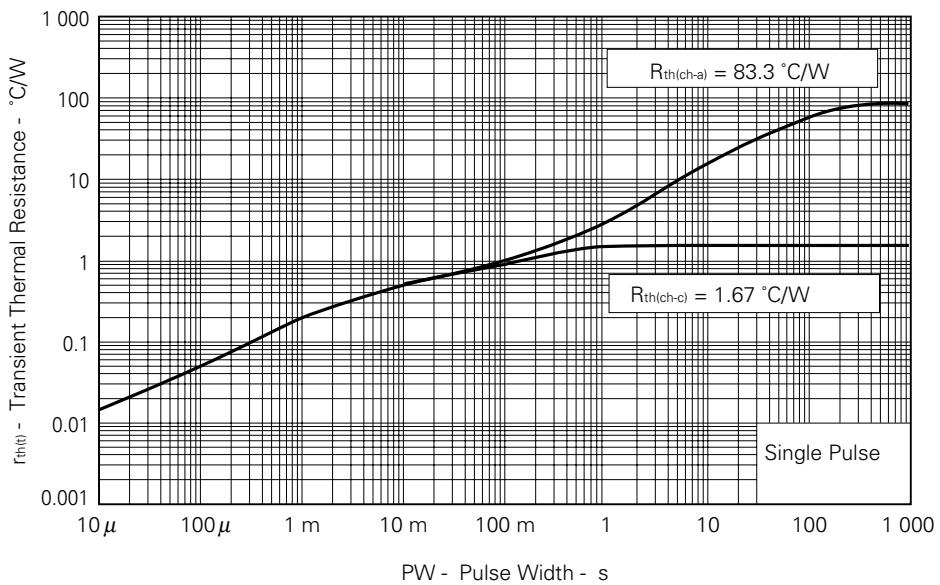
## Test Circuit 3 Gate Charge



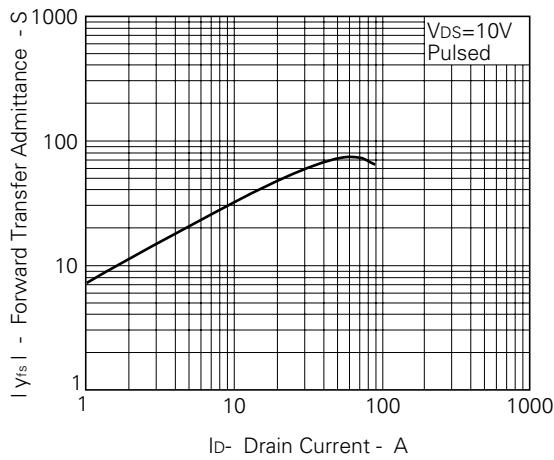
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

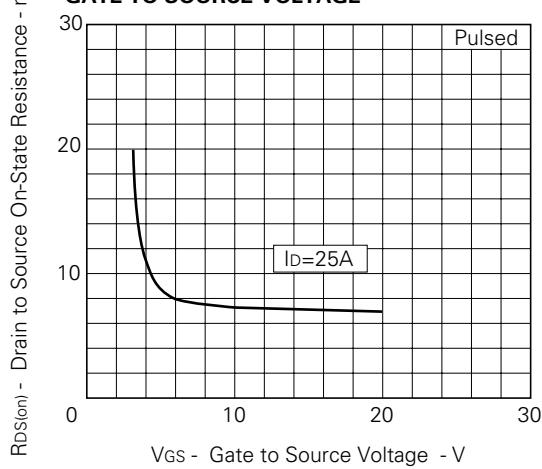
## TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



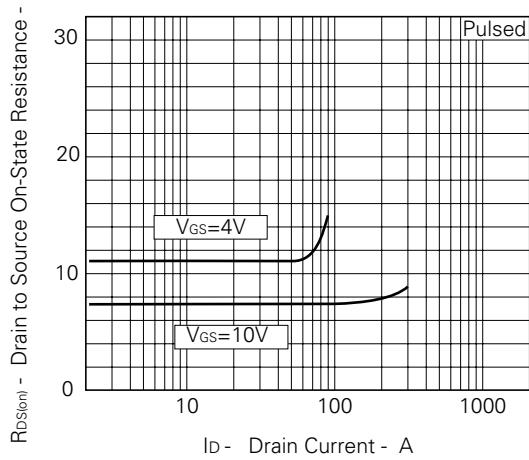
## FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



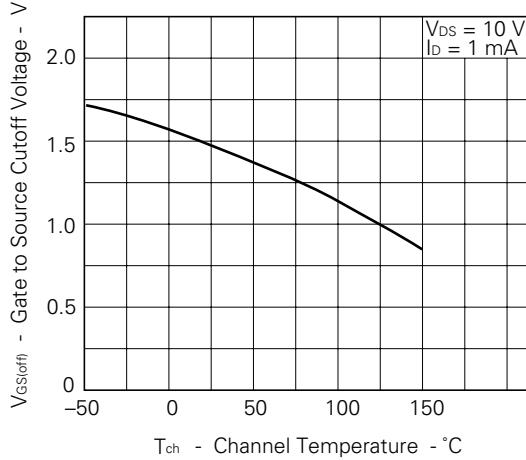
## DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

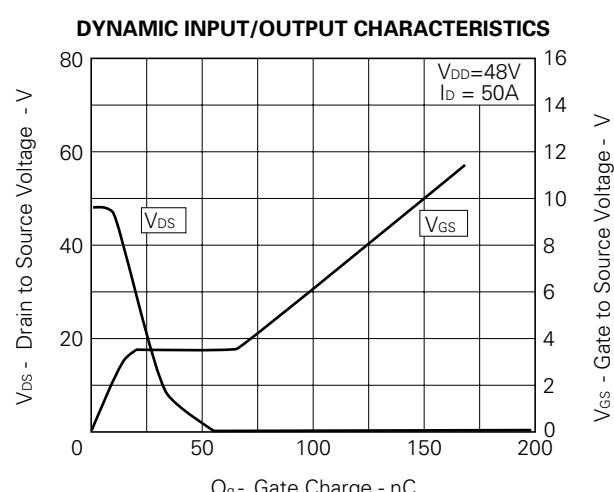
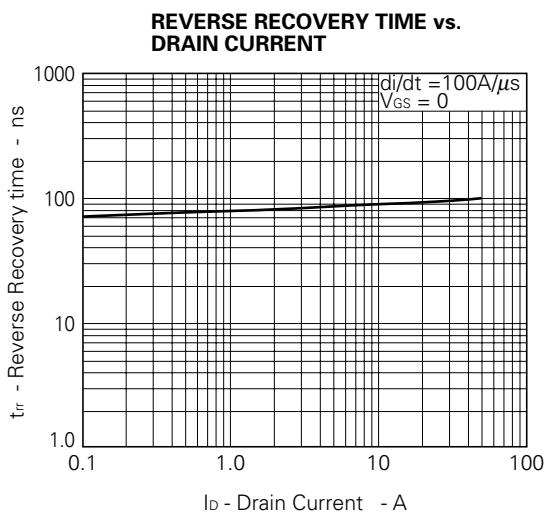
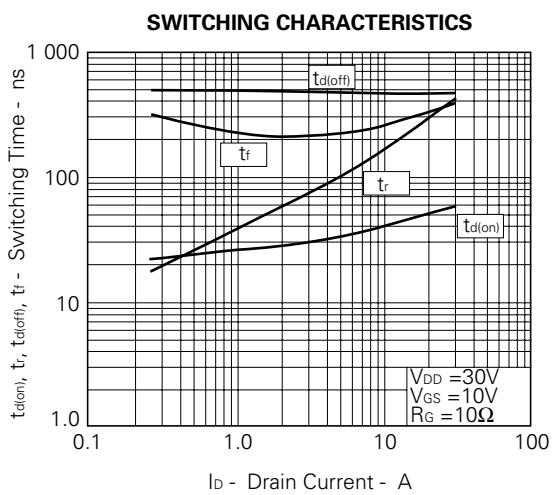
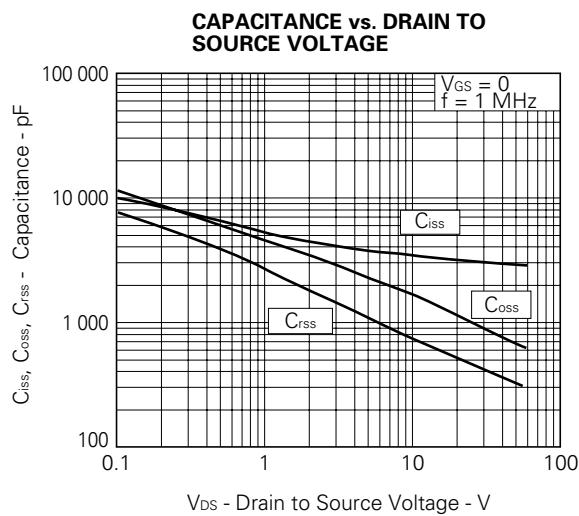
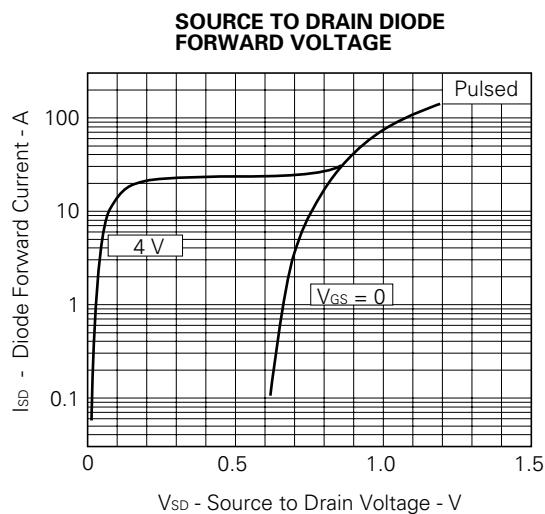
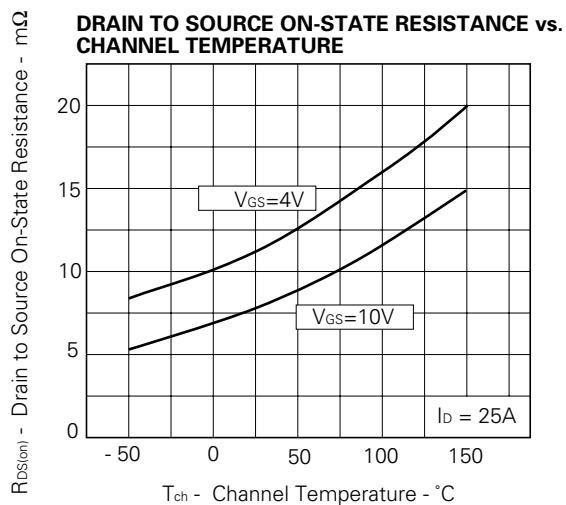


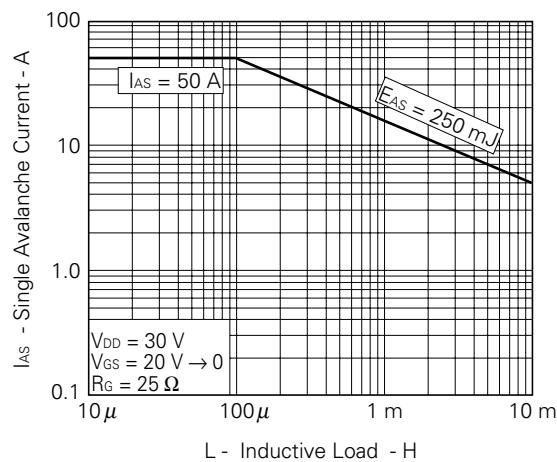
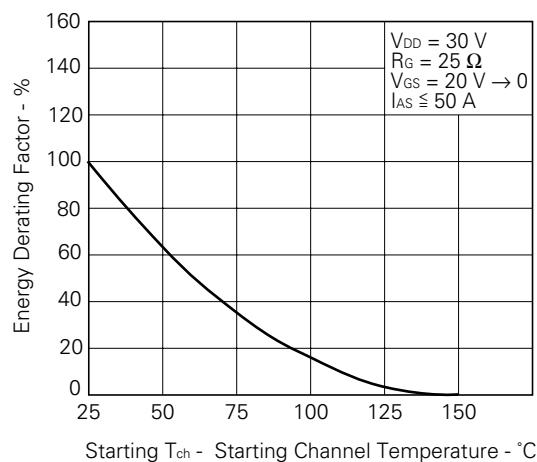
## DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



## GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE





**SINGLE AVALANCHE CURRENT vs.  
INDUCTIVE LOAD****SINGLE AVALANCHE ENERGY  
DERATING FACTOR**

**REFERENCE**

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	TEI-1202
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207
Semiconductor device package manual.	IEI-1213
Guide to quality assurance for semiconductor devices.	MEI-1202
Semiconductor selection guide.	MF-1134
Power MOS FET features and application switching power supply.	TEA-1034
Application circuits using Power MOS FET.	TEA-1035
Safe operating area of Power MOS FET.	TEA-1037

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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