MEMORY Mobile FCRAM™

CMOS

16M Bit (1M word x 16 bit)

Mobile Phone Application Specific Memory

MB82D01160-90/90L

CMOS 1,048,576-WORD x 16 BIT
Fast Cycle Random Access Memory
with Low Power SRAM Interface

■ DESCRIPTION

The Fujitsu MB82D01160 is a CMOS Fast Cycle Random Access Memory (FCRAM) with asynchronous Static Random Access Memory (SRAM) interface containing 16,777,216 storages accessible in a 16-bit format. This MB82D01160 is suited for low power applications such as Cellular Handset and PDA.

■ FEATURES

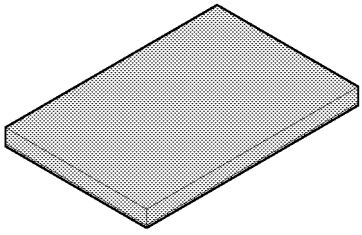
- Asynchronous SRAM Interface
- Fast Random Cycle Time
  t_{RC} = 90ns
- Low Power Consumption
  I_{DDS1} = 200µA, 100µA (L version)
- Wide Operating Condition
  V_{DD} = +2.3V to +2.7V or
  +2.7V to +3.0V
  T_A = -25°C to +85°C
- Byte Write Control
- Dual Chip Enable

■ PRODUCT LINE

	MB82D01160-90	MB82D01160-90L
Read Cycle Time (t_{RC})	90ns min	90ns min
Standby Current (I_{DDS1})	200µA max	100µA max

■ PACKAGE

48-pin Plastic FBGA Package

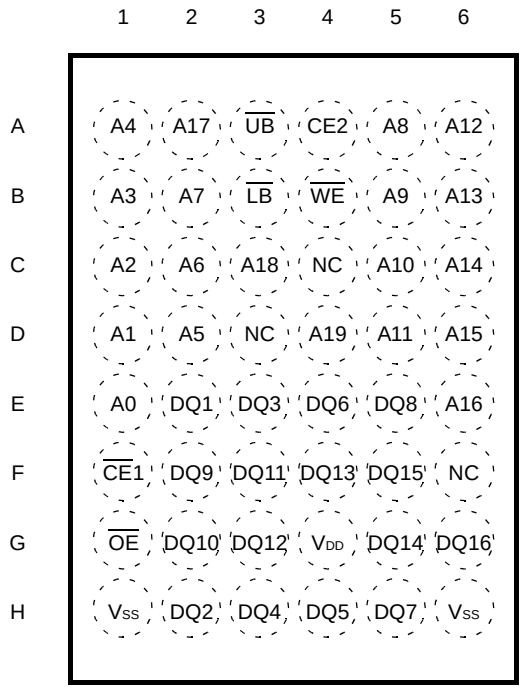


(BGA-48P-M16)

Notice: FCRAM is a trademark of Fujitsu Limited, Japan

■ PIN ASSIGNMENT

(TOP VIEW)

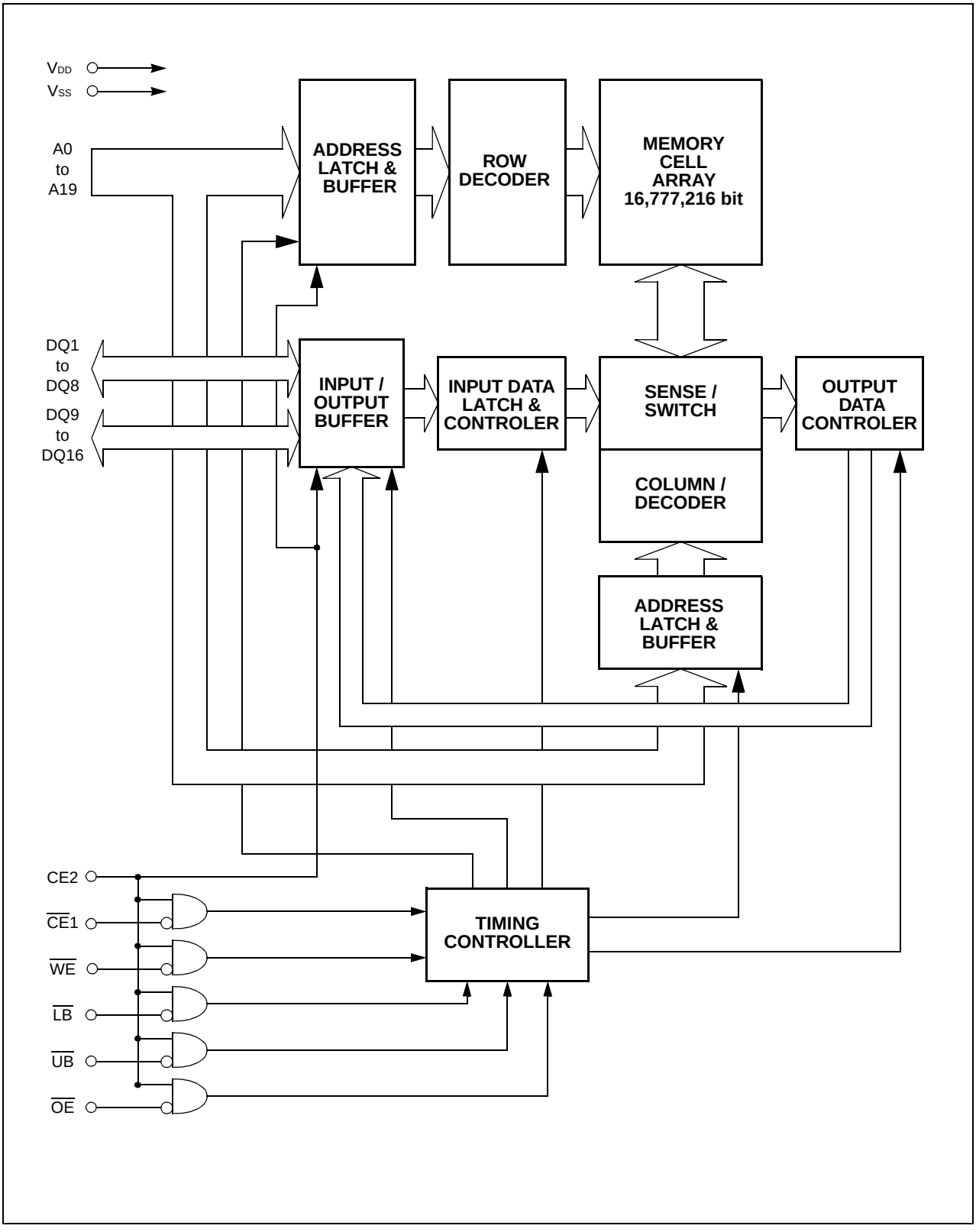


(BGA-48P-M16)

■ PIN DESCRIPTION

Pin Name	Description
A_0 to A_{19}	Address Input
$\overline{CE}1$	Chip Enable (Low Active)
CE2	Chip Enable (High Active)
$\overline{WE}$	Write Enable (Low Active)
$\overline{OE}$	Output Enable (Low Active)
$\overline{LB}$	Lower Byte Write Control (Low Active)
$\overline{UB}$	Upper Byte Write Control (Low Active)
DQ_{1-8}	Lower Byte Data Input/Output
DQ_{9-16}	Upper Byte Data Input/Output
V_{DD}	Power Supply
V_{SS}	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

Mode	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	DQ1-8	DQ9-16	I_{DD}
Inhibit *1	X	L	X	X	X	X	High-Z	High-Z	I_{DDS}
Standby (Deselect)	H	H	X	X	X	X			
Output Disable *2	L	H	H	H	X	X	High-Z	High-Z	I_{DDA}
Read *3				L	X	X	Output Valid	Output Valid	
Write			L	H	L	L	Input Valid	Input Valid	
Write (Upper Byte)					L	H	Input Valid	Invalid	
Write (Lower Byte)					H	L	Invalid	Input Valid	

Note: L = VIL, H = VIH, X can be either VIL or VIH, High-Z = High Impedance

*1: CE2=L state should only be used at Power-up stage.

*2: Output Disable condition should not be kept longer than 1μs.

*3: Byte control at Read operation is not supported.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage of V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.5 to +3.3	V
Voltage at Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to +3.3	V
Short Circuit Output Current	I_{OUT}	±50	mA
Storage Temperature	T_{STG}	-55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS (See WARNING below.)

(Referenced to V_{SS})

Parameter	Notes	Symbol	Min.	Max.	Unit
Supply Voltage		$V_{DD\ (27)}$	2.7	3.0	V
		$V_{DD\ (23)}$	2.3	2.7	V
		V_{SS}	0	0	V
High Level Input Voltage	*1	$V_{IH\ (27)}$	2.3	V_{DD}+0.3	V
		$V_{IH\ (23)}$	2.0	V_{DD}+0.3	V
Low Level Input Voltage	*1	V_{IL}	-0.3	0.4	V
Ambient Temperature		T_A	-25	85	°C

Notes: *1: Minimum DC voltage on input or I/O pins are -0.3V. During voltage transitions, inputs may negative overshoot V_{SS} to -1.0V for periods of up to 5ns. Maximum DC voltage on input and I/O pins are V_{DD}+0.3V. During voltage transitions, outputs may positive overshoot to V_{DD}+1.0V for periods of up to 5 ns.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ PACKAGE PIN CAPACITANCE

Symbol	Description	Test Setup	Typ.	Max.	Unit
C_{IN1}	Address Input Capacitance	V_{IN} = 0V	—	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	—	8	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0V	—	5	pF

Note: Test conditions T_A = 25°C, f = 1.0 MHz

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

Parameter		Symbol	Test Conditions		Min.	Typ.	Max.	Unit
Input Leakage Current		I_{LI}	V_{IN} = V_{SS} to V_{DD}		-1.0	—	+1.0	µA
Output Leakage Current		I_{LO}	V_{OUT} = V_{SS} to V_{DD}, Output Disable		-1.0	—	+1.0	µA
Output High Voltage Level		V_{OH}	I_{OH} = –0.5mA		1.8	—	—	V
Output Low Voltage Level		V_{OL}	I_{OL} = 1mA		—	—	0.4	V
V_{DD} Standby Current		I_{DDS}	$\overline{V_{DD}}$ = V_{DD} max., V_{IN} = V_{IH} or V_{IL} $\overline{CE1}$ = CE2 = V_{IH}, I_{OUT}=0mA		—	1.5	2	mA
	L version				—	1	1.5	
		I_{DDS1}	V_{DD} = V_{DD} max., V_{IN} ≤ 0.2V or $\overline{V_{IN}}$ ≥ V_{DD} – 0.2V, $\overline{CE1}$ = CE2 ≥ V_{DD} – 0.2V, I_{OUT}=0mA		—	160	200	µA
	L version				—	80	100	
V_{DD} Active Current		I_{DDA1}	V_{DD} = V_{DD} max., $\overline{V_{IN}}$ = V_{IH} or V_{IL}, $\overline{CE1}$ = V_{IL} and CE2= V_{IH}, I_{OUT}=0mA	t_{RC} / t_{WC} = minimum	—	15	20	mA
		I_{DDA2}		t_{RC} / t_{WC} = maximum	—	2.5	3.0	mA

Notes: *1: All voltages are referenced to Vss.

*2: DC Characteristics are measured after following POWER-UP timing.

*3: I_{DDA} depends on the output load conditions.

2. AC Characteristics

(1) Read Operation

Parameter	Symbol	-90/-90L		Unit	Notes
		Min.	Max.		
Read Cycle Time	t_{RC}	90	1000	ns	*1
Address Setup Time at $\overline{CE}1$ High to Low Transition	t_{ASC}	–5	—	ns	
Address Hold Time during $\overline{CE}1$ Low	t_{AHC}	90	—	ns	*2
Address Access Time	t_{AA}	—	90	ns	*3
Chip Enable Access Time	t_{CE}	—	90	ns	*3
Output Enable Access Time	t_{OE}	—	60	ns	*3
Output Data Hold Time	t_{OH}	5	—	ns	*3
$\overline{CE}1$ Low to Output Low-Z	t_{CLZ}	10	—	ns	*4
$\overline{OE}$ Low to Output Low-Z	t_{OLZ}	0	—	ns	*4
$\overline{CE}1$ High to Output High-Z	t_{CHZ}	—	25	ns	*4
$\overline{OE}$ High to Output High-Z	t_{OHZ}	—	15	ns	*4
$\overline{CE}1$ High Pulse Width	t_{CP}	10	—	ns	
$\overline{CE}1$ High to Address Hold Time	t_{CHAH}	–5	—	ns	*5
Address Invalid Time during Read ($\overline{CE}1$=Low)	t_{AX}	—	10	ns	

Notes: *1: Maximum value is a reference and is applied to Output Disable condition.

*2: t_{AHC} must be satisfied every address valid state after t_{AX} during $\overline{CE}1$=Low.

*3: The output load is 30pF.

*4: The output load is 5pF.

*5: If actual address change before $\overline{CE}1$ High transition is earlier than t_{CHAH} (min), t_{CP} ($\overline{CE}1$ High period) should be kept at least t_{RC} (min) period.

2. AC Characteristics (Continued)

(2) Write Operation

Parameter	Symbol	-90/-90L		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{WC}	90	1000	ns	*1
Address Setup Time	t_{AS}	0	—	ns	
Address Hold Time	t_{AH}	40	—	ns	
$\overline{CE}1$ Write Setup Time	t_{CS}	0	1000	ns	*2
$\overline{CE}1$ Write Hold Time	t_{CH}	0	1000	ns	*2
$\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Setup Time	t_{BS}	0	—	ns	
$\overline{WE}$, $\overline{LB}$, $\overline{UB}$ Hold Time	t_{BH}	0	—	ns	
$\overline{OE}$ Setup Time	t_{OES}	0	—	ns	
$\overline{OE}$ Hold Time	t_{OEH}	15	—	ns	
$\overline{OE}$ High to $\overline{CE}1$ Low Setup Time	t_{OHCL}	–5	—	ns	*3
$\overline{OE}$ High to Address Hold Time	t_{OHAH}	0	—	ns	*4
$\overline{CE}1$ Write Pulse Width	t_{CW}	60	—	ns	*5, *6
$\overline{WE}$ Write Pulse Width	t_{WP}	60	—	ns	*5, *6
$\overline{CE}1$ Write Recovery Time	t_{WRC}	15	—	ns	*7
$\overline{WE}$ Write Recovery Time	t_{WR}	15	1000	ns	*2, *7
Data Setup Time	t_{DS}	20	—	ns	
Data Hold Time	t_{DH}	10	—	ns	
$\overline{CE}1$ Low to Output in Low-Z	t_{CLZ}	10	—	ns	*8
$\overline{OE}$ Low to Output in Low-Z	t_{OLZ}	0	—	ns	*8

Notes: *1: Maximum value is a reference and applied to Output Disable condition.

*2: Maximum value is applied to Output Disable condition.

*3: t_{OHCL} (min) must be satisfied if read operation is not performed prior to write operation. In case $\overline{OE}$ is disabled after t_{OHCL} (min), $\overline{WE}$ Low must be asserted after t_{RC} (min) from $\overline{CE}1$ Low.

*4: Applicable if $\overline{CE}1$ stays Low after read operation.

*5: t_{WHP} (max) must be satisfied for the high pulse noise.

*6: t_{CW} and t_{WP} are applied if write operation is initiated by $\overline{CE}1$ and $\overline{WE}$, respectively.

*7: t_{WRC} and t_{WR} are applied if write pulse is terminated by $\overline{CE}1$ and $\overline{WE}$, respectively.

*8: The output load is 5pF.

2. AC Characteristics (Continued)

(3) Other Timing Parameter

Parameter	Symbol	-90/-90L		Unit	Note
		Min.	Max.		
$\overline{CE}1$ High to $\overline{OE}$ Invalid Time for Standby Entry	t_{CHOX}	10	—	ns	
$\overline{CE}1$ High to $\overline{WE}$ Invalid Time for Standby Entry	t_{CHWX}	20	—	ns	
$\overline{CE}1$ and CE2 Active Glitch Pulse Width	t_{CAP}	—	5	ns	*1
$\overline{CE}1$ or $\overline{WE}$ High Glitch Pulse Width during Write Cycle	t_{WHP}	—	5	ns	*2
CE2 Low Hold Time after Power-up	t_{C2LP}	350	—	µs	*3
$\overline{CE}1$ High Hold Time following CE2 High after Power-up	t_{C1HP}	300	—	µs	*4

Notes: *1: Active means a condition where $\overline{CE}1 = V_{IL}$ and CE2 $=V_{IH}$.

*2: Specified to the one time high pulse width during t_{CW} or t_{WP} and excluded 10ns from beginning and end of the write cycle.

*3: Requires at least two dummy read cycles.

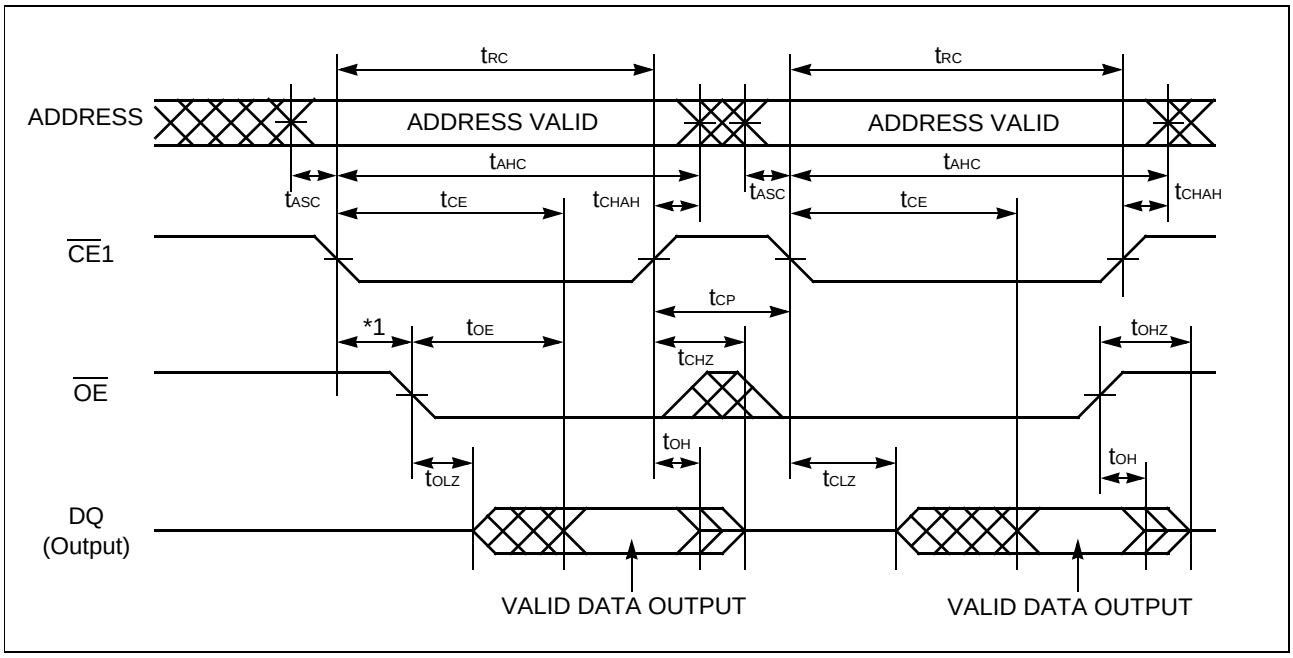
*4: Required when dummy read cycles are not performed.

(4) AC Test Conditions

Symbol	Description	Test Setup	Value	Unit
V_{IH}	Input High Level	V_{DD} = 2.7V to 3.0V	2.3	V
		V_{DD} = 2.3V to 2.7V	2.0	
V_{IL}	Input Low Level	—	0.4	V
V_{REF}	Input Timing Measurement Level	V_{DD} = 2.7V to 3.0V	1.3	V
		V_{DD} = 2.3V to 2.7V	1.1	V
t_T	Input Transition Time	Between V_{IL} and V_{IH}	5	ns

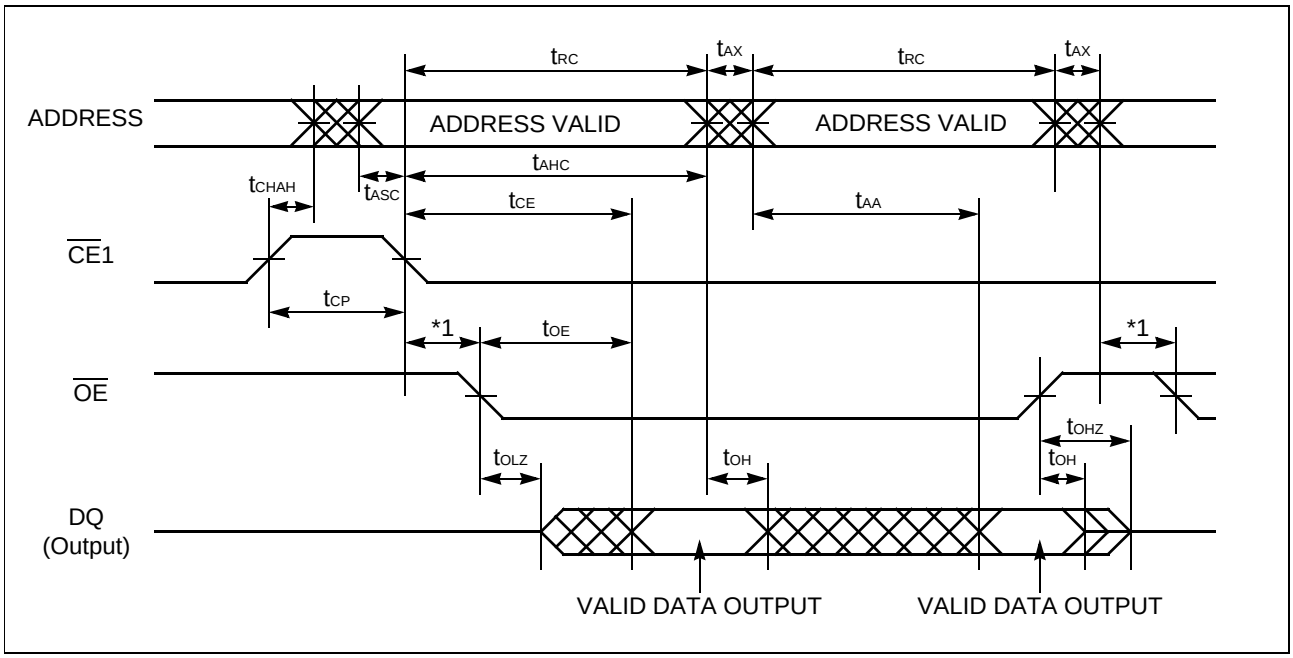
■ TIMING DIAGRAMS

1. READ Timing #1 ($\overline{CE}$1 Control)



Note: CE2 and $\overline{WE}$ must be HIGH for entire read cycle.
*1: Output Disable condition before new Read data valid should not be kept longer than 1µs.

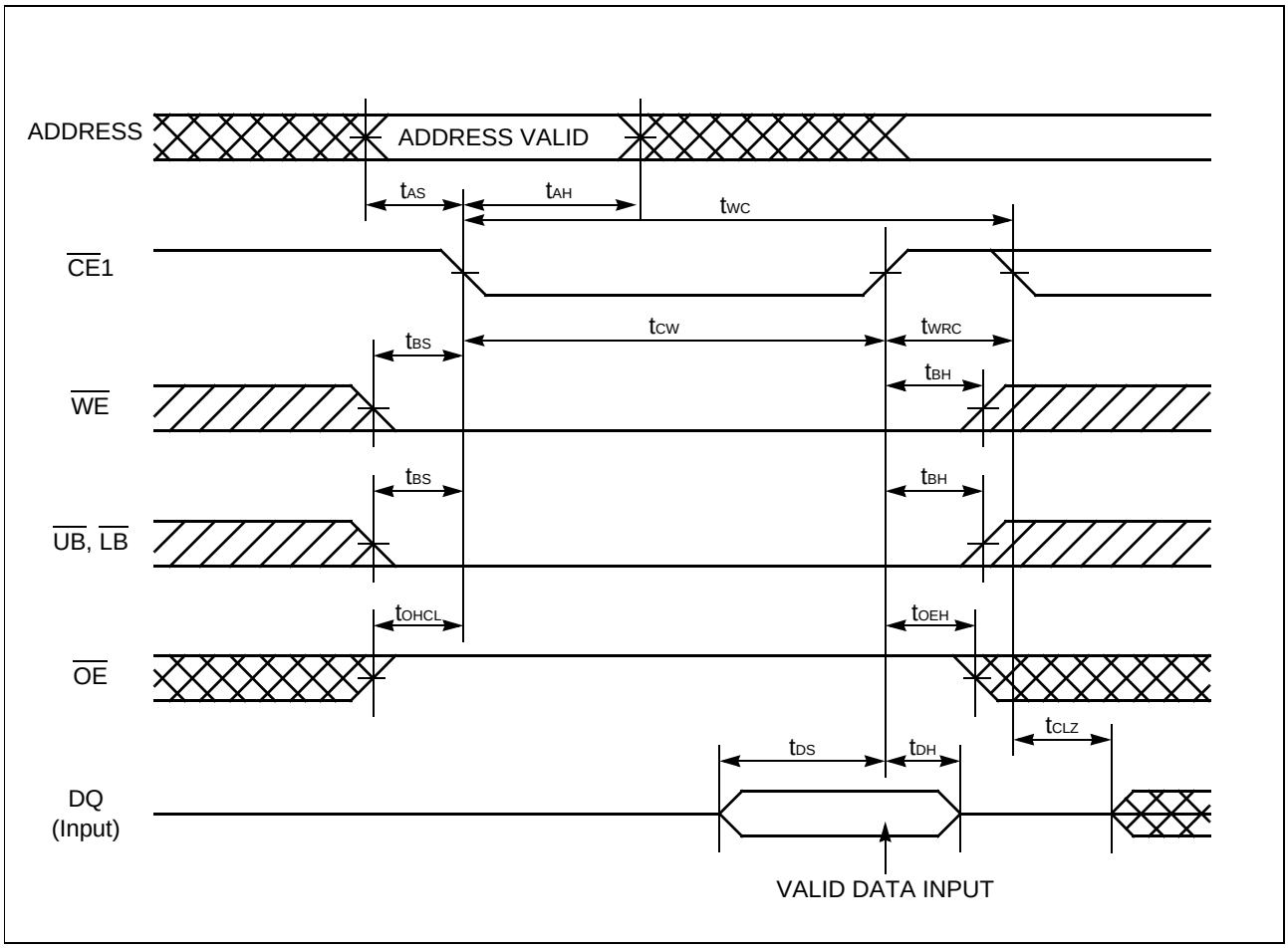
2. READ Timing #2 (Address Access)



Note: CE2 and $\overline{WE}$ must be HIGH for entire read cycle.
*1: Output Disable condition before new Read data valid should not be kept longer than 1µs.

■ TIMING DIAGRAMS (Continued)

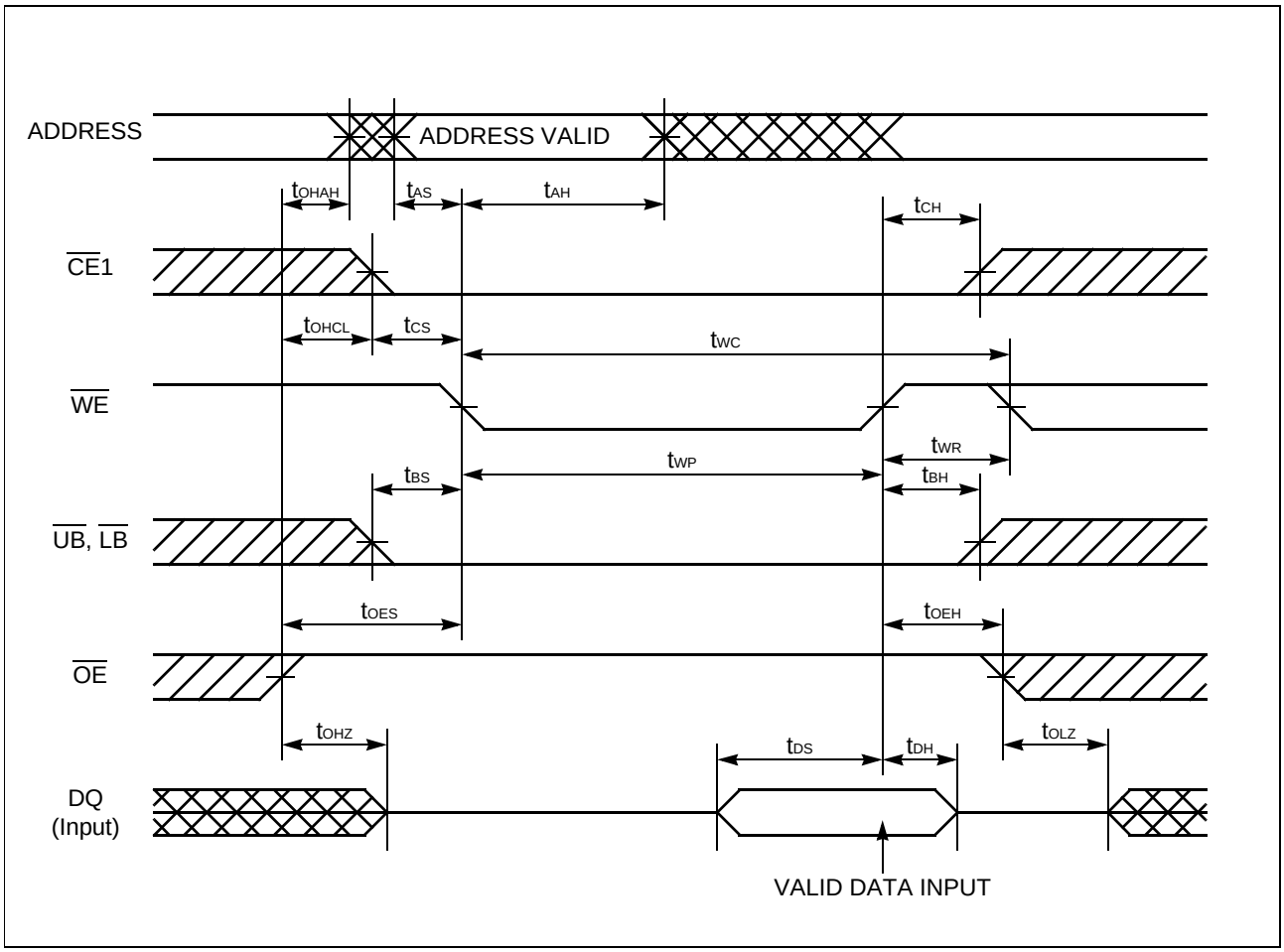
3. WRITE Timing #1 ($\overline{CE}$1 Control)



Note: CE2 must be HIGH for write cycle.

■ TIMING DIAGRAMS (Continued)

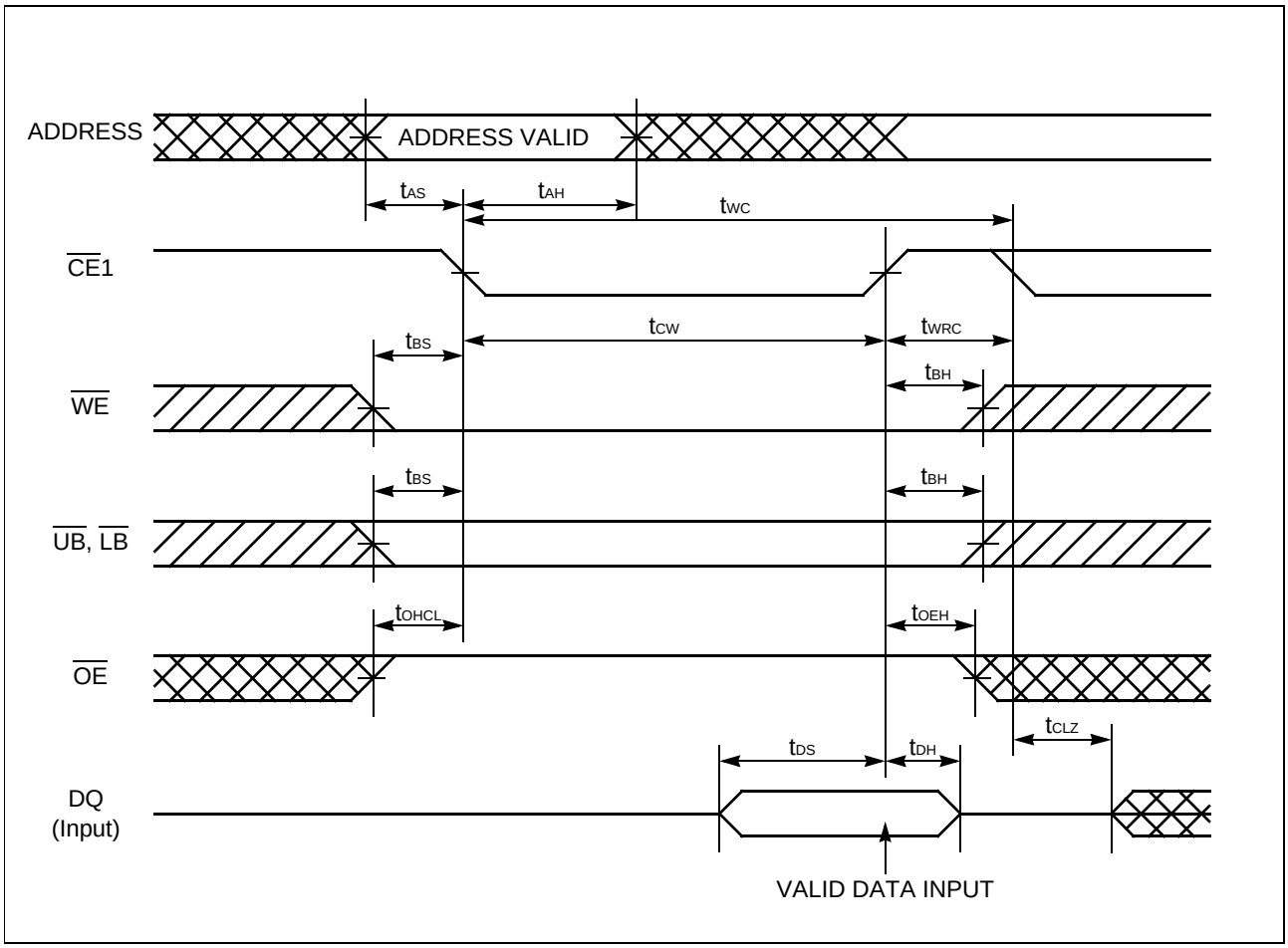
4. WRITE Timing #2 ($\overline{WE}$ Control)



Note: CE2 must be HIGH for write cycle.

■ TIMING DIAGRAMS (Continued)

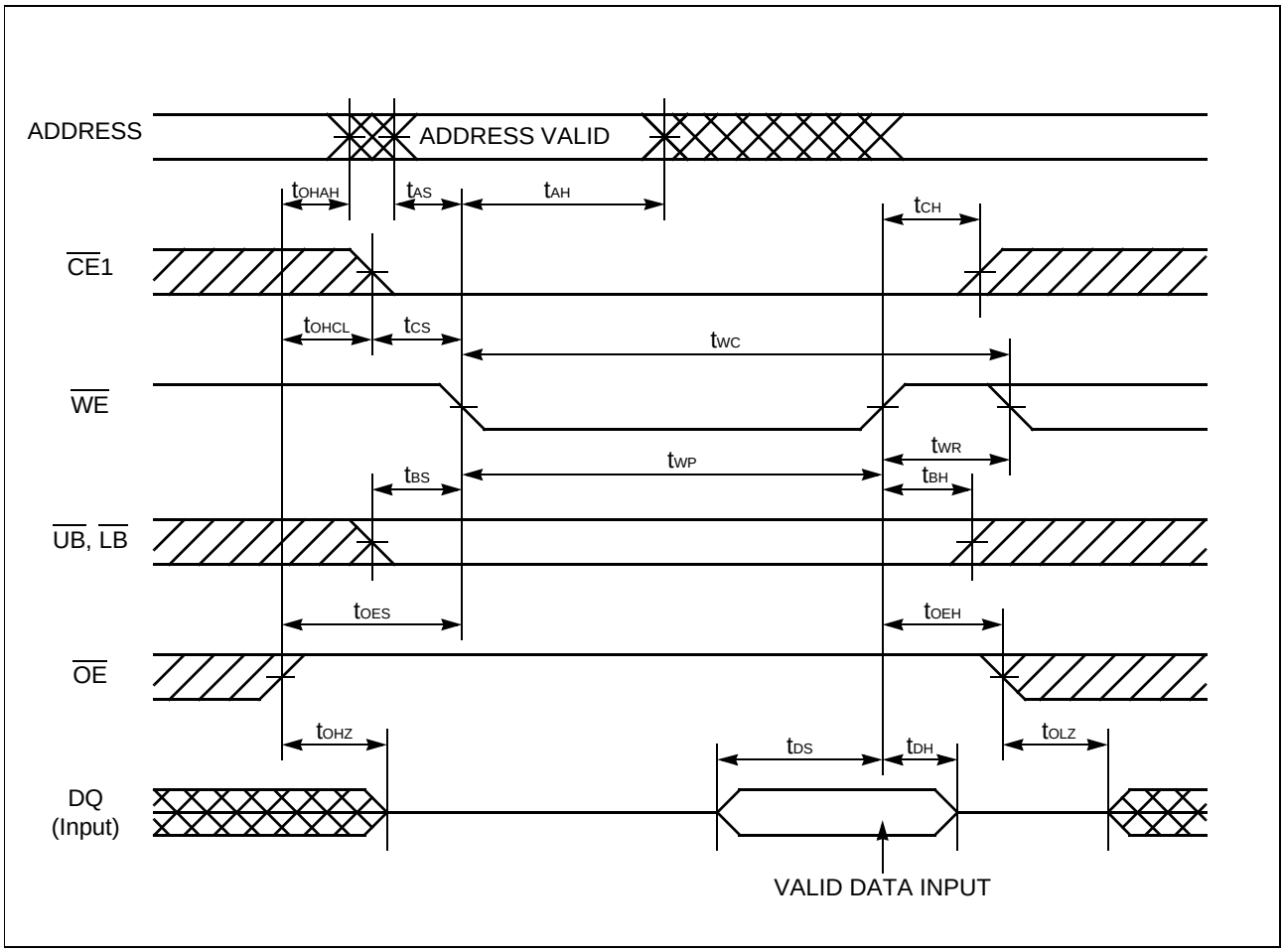
5. BYTE WRITE Timing #1 ($\overline{CE}$1 Control)



Note: CE2 must be HIGH and either $\overline{LB}$ or $\overline{UB}$ must be LOW for byte write cycle.

■ TIMING DIAGRAMS (Continued)

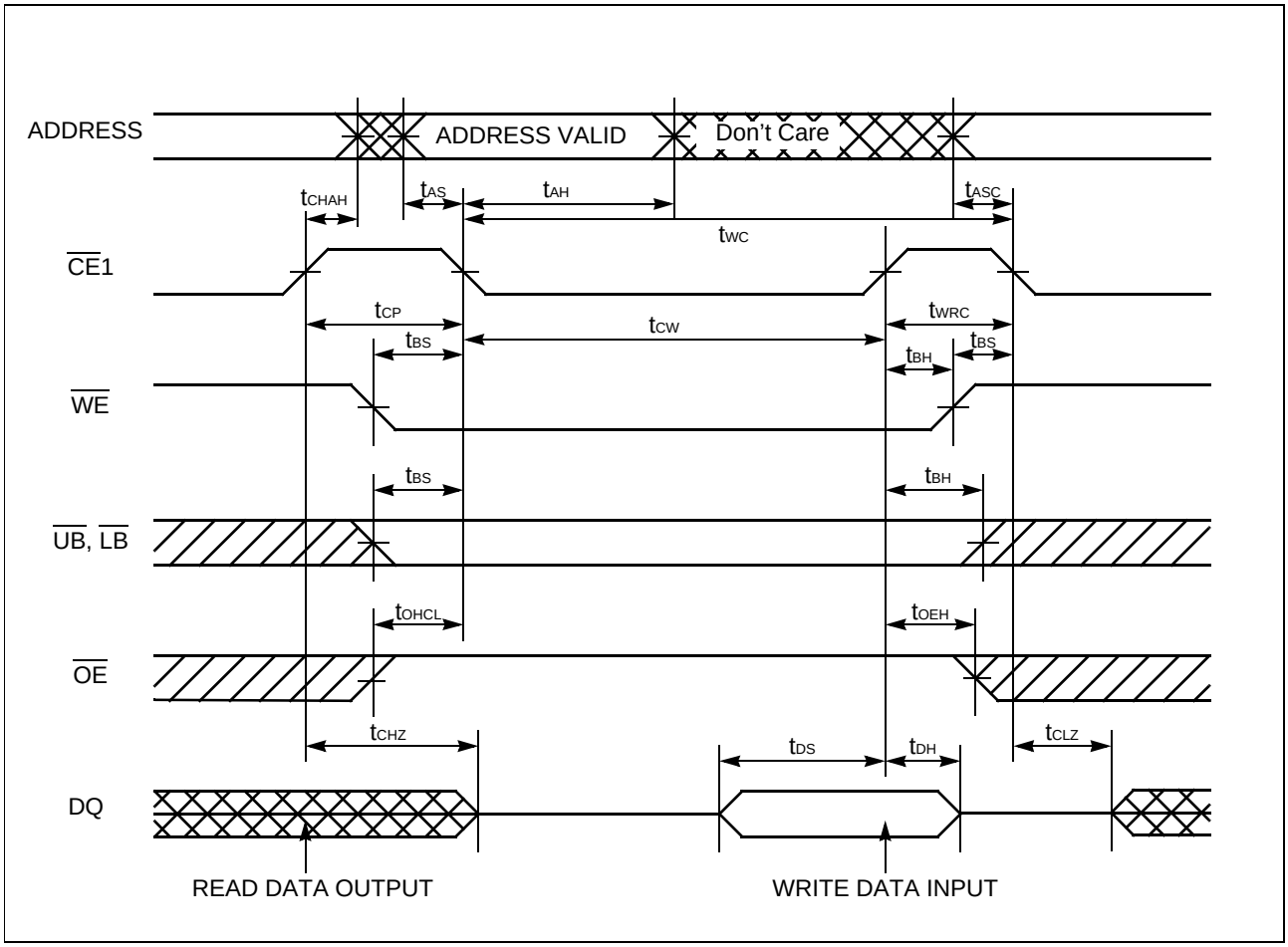
6. BYTE WRITE Timing #2 ($\overline{WE}$ Control)



Note: CE2 must be HIGH and either $\overline{LB}$ or $\overline{UB}$ must be LOW for byte write cycle.

■ TIMING DIAGRAMS (Continued)

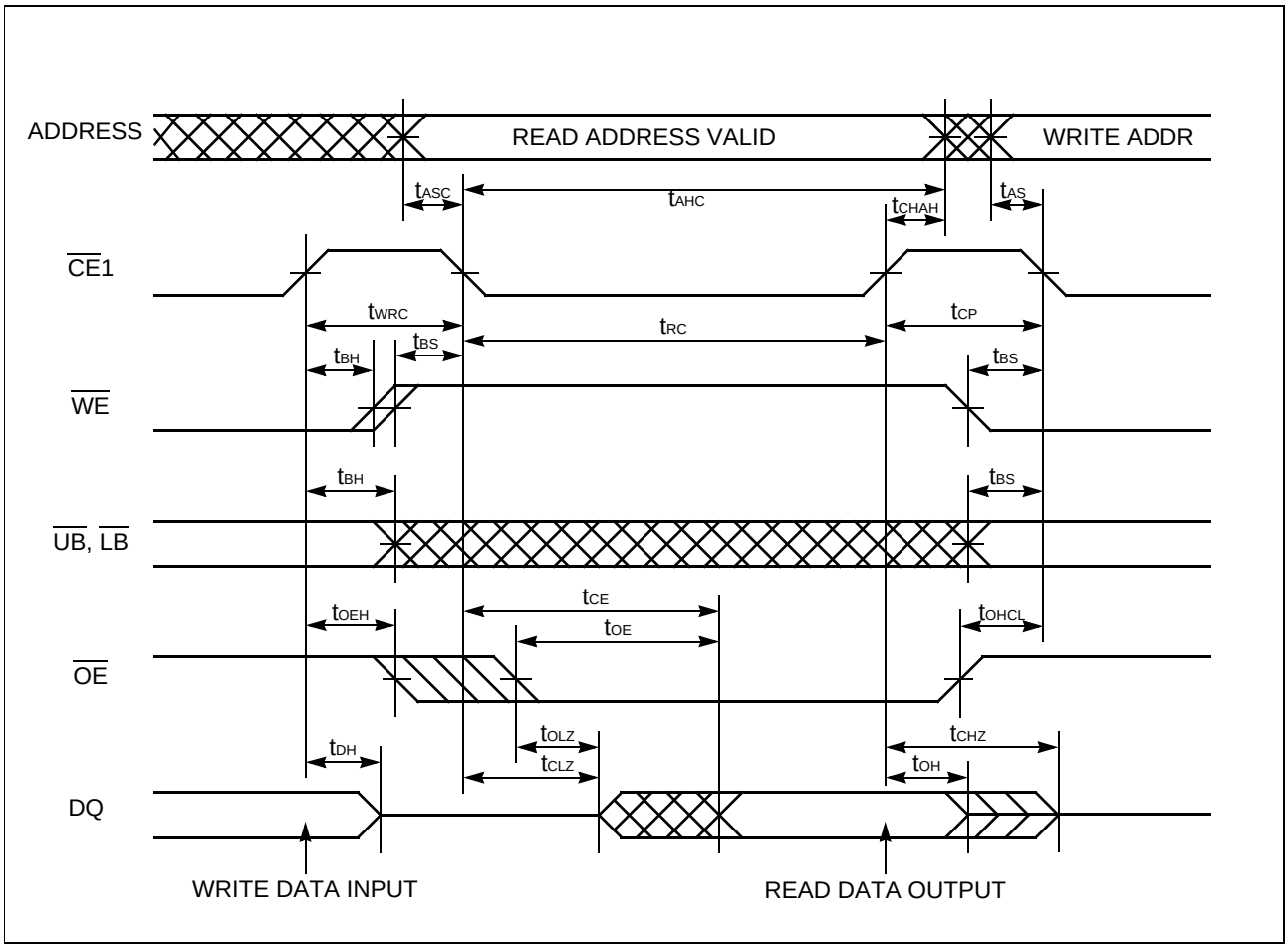
7. READ / WRITE Timing #1-1 ($\overline{CE}$ Control)



Note: Write address is edge trigger of either $\overline{CE}1$ or $\overline{WE}$ falling edge.

■ TIMING DIAGRAMS (Continued)

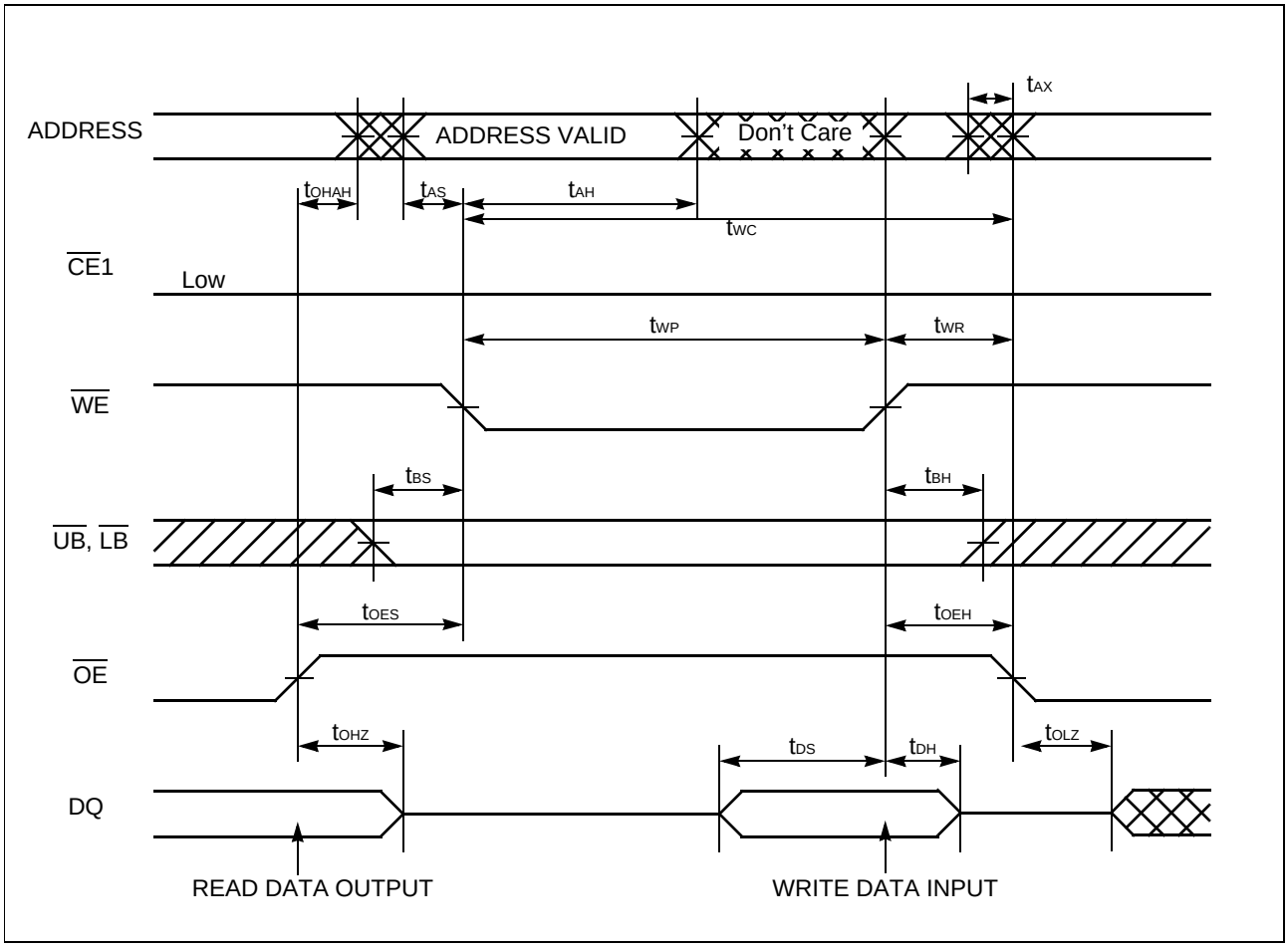
8. READ / WRITE Timing #1-2 ($\overline{CE}$ Control)



Note: $\overline{WE}$ must be HIGH for read cycle.

■ TIMING DIAGRAMS (Continued)

9. READ / WRITE Timing #2-1 ($\overline{OE}$ and $\overline{WE}$ Control)

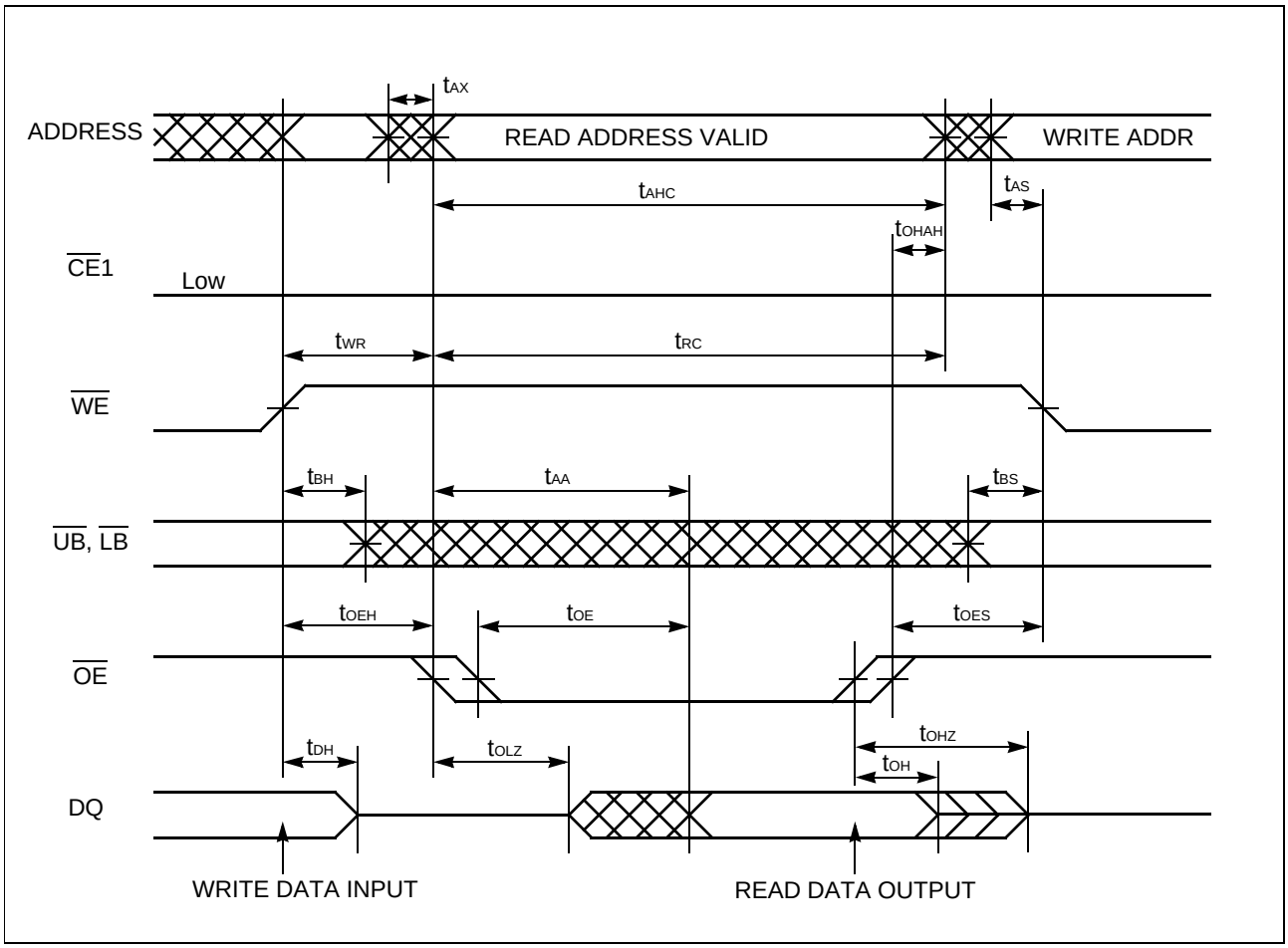


Note: $\overline{CE}1$ can be tied to LOW for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}1$ is tied to LOW, output is exclusively controlled by $\overline{OE}$ and read address can be issued after $\overline{WE}$ is brought to High.

WARNING: The read address following write operation must be changed if $\overline{CE}1$ stays LOW.

■ TIMING DIAGRAMS (Continued)

10. READ / WRITE Timing #2-2 ($\overline{OE}$ and $\overline{WE}$ Control))

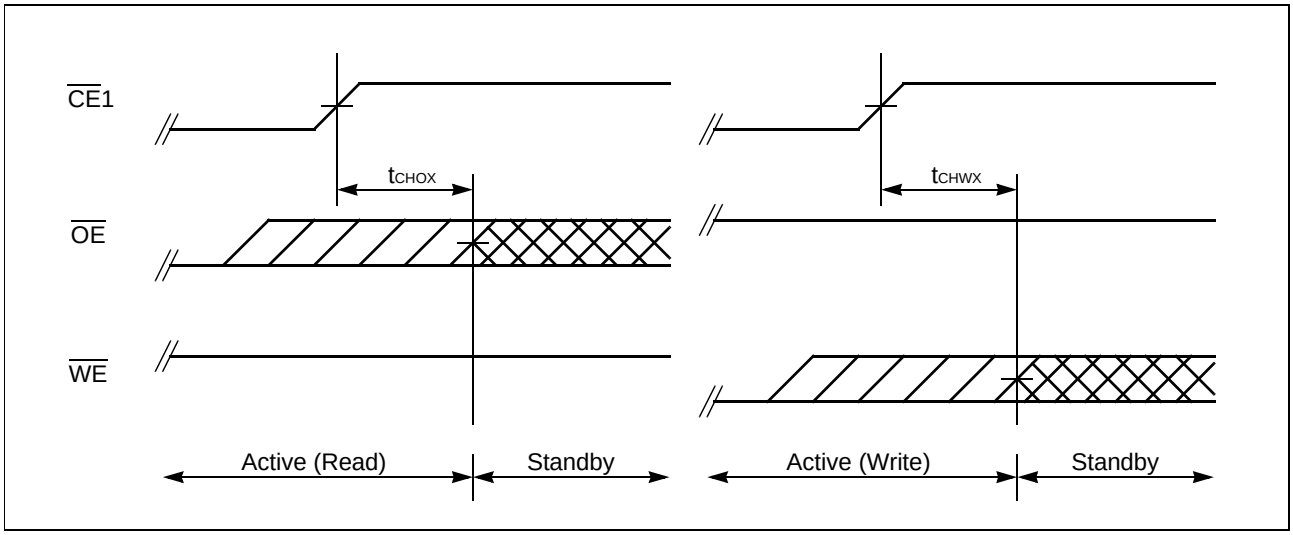


Note: $\overline{CE}$1 can be tied to LOW for $\overline{WE}$ and $\overline{OE}$ controlled operation.
When $\overline{CE}$1 is tied to LOW, output is exclusively controlled by $\overline{OE}$ and read address can be issued after $\overline{WE}$ is brought to High.

WARNING: The read address following write operation must be changed if $\overline{CE}$1 stays LOW.

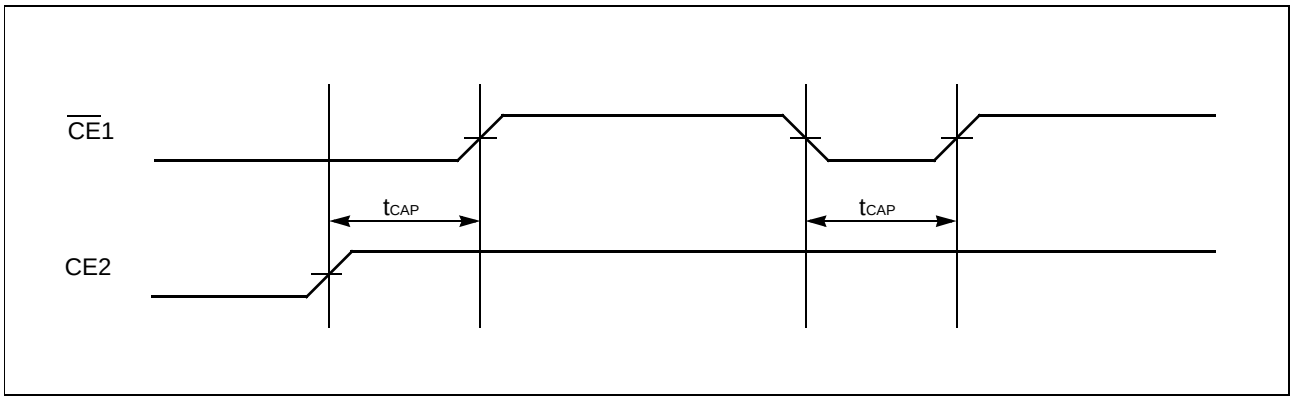
■ TIMING DIAGRAMS (Continued)

11. Standby Entry Timing after Read or Write



Note: Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (min) period from either last address transition or $\overline{CE}1$ Low to High transition.

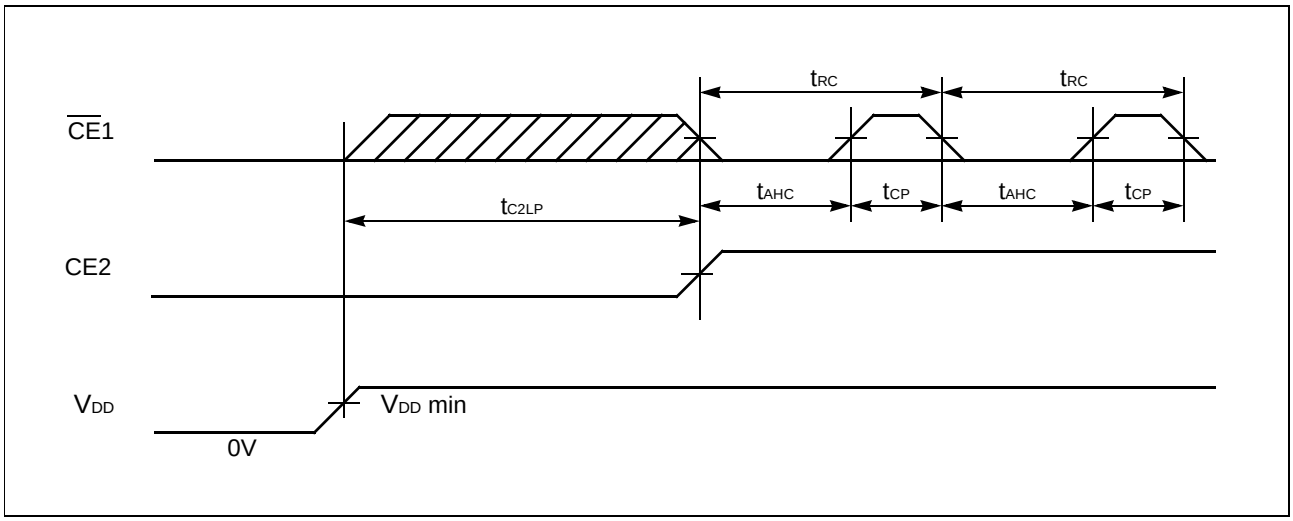
12. Chip Enable Timing



Note: t_{CAP} is not applicable CE2 HIGH pulse width while $\overline{CE}1$ stays LOW and CE2 should not be used for any operation control after Power-up.

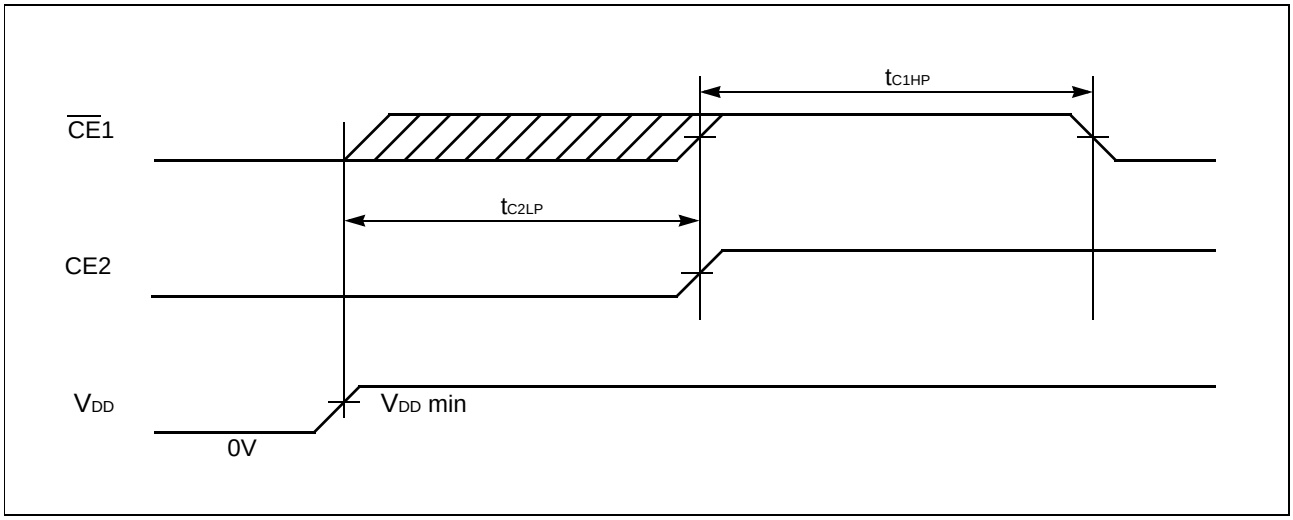
■ TIMING DIAGRAMS (Continued)

13. Power-Up Timing #1



Note: A minimum of two dummy read cycle must be performed prior to regular read and write operation after t_{C2LP}.

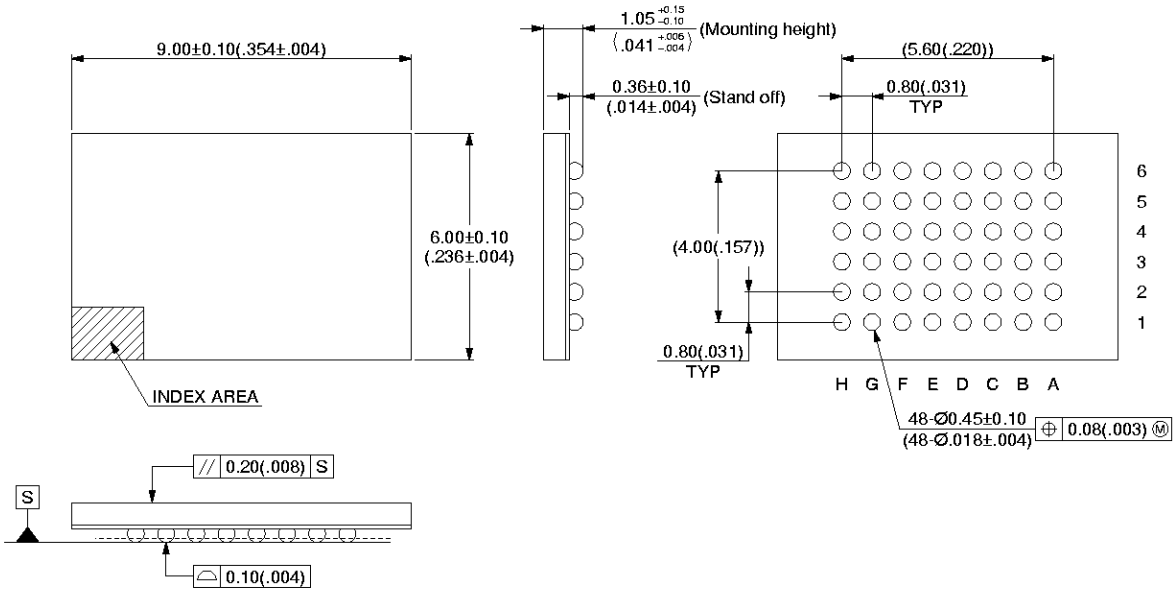
14. Power-Up Timing #2



Note: No dummy read cycle is required if t_{C1HP} is satisfied.

■ PACKAGE DIMENTIONS

48-pin plastic FBGA
(BGA-48P-M16)



Dimensions in mm

■ ORDERING INFORMATION

Part Number	Package	Remarks
MB82D01160-90PBT	Plastic FBGA 48-ball (BGA-48P-M16)	I_{DDS1} = 200 µA max.
MB82D01160-90LPBT	Plastic FBGA 48-ball (BGA-48P-M16)	I_{DDS1} = 100 µA max.

MEMO

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Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with FUJITSU sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Control Law of Japan, the prior authorization by Japanese government should be required for export of those products from Japan.