FAIRCHILD SEMICONDUCTOR®

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100ELT22
5V Dual TTL to Differential PECL Translator

General Description

The 100ELT22 is a TTL to differential PECL translator operating from a single +5V supply.

Both outputs of a differential pair should be terminated in 50Ω to V_{CC} - 2.0V even if only one output is being used. If an output pair is unused both outputs can be left open (un-terminated).

The 100 series is temperature compensated.

Features

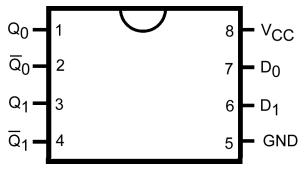
- Typical propagation delay of 300 ps
- <100 ps between outputs
- Max I_{CC} of 30 mA
- Fairchild MSOP-8 package is a drop-in replacement to ON TSSOP-8
- Flow through pinout
- Meets or exceeds JEDEC specification EIA/JESD78 IC latch-up test
- Moisture Sensitivity Level 1
- ESD Performance:
  - Human Body Model > 2000V
  - Machine Model > 200V

Ordering Code:

Order Number	Package Number	Product Code Top Mark	Package Description
100ELT22M	M08A	KLT22	8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
100ELT22M8 (Preliminary)	MA08D	KT22	8-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide

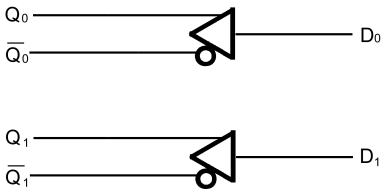
Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Connection Diagram



Top View

Logic Diagram



Pin Descriptions

Pin Name	Description
Q_n, $\overline{Q}_n$	PECL Differential Outputs
D_0, D_1	TTL Inputs
V_{CC}	Positive Supply
GND	Ground

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	0.0V to +7.0V
Input Voltage (V_I) $V_I \le V_{CC}$	0.0V to + 7.0V
DC Output Current (I_{OUT})	
Continuous	50 mA
Surge	100 mA
Storage Temperature (T_{STG})	−65°C to + 150°C

Recommended Operating Conditions

Power Supply Operating	V_{CC} = 4.2V to 5.5V
TTL Input Voltage	0.0V to V_{CC}
Free Air Operating Temperature (T_A)	−40°C to +85°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

PECL DC Electrical Characteristics V_{CC} = 5.0V; GND = 0.0V (Note 2)

Symbol	Parameter	−40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{CC}	Power Supply Current			30			30			30	mA
V_{OH}	Output HIGH Voltage (Note 3)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
V_{OL}	Output LOW Voltage (Note 3)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV

Note 2: Output parameters vary 1 to 1 with V_{CC}. V_{CC} can vary +0.5V/−0.8V.

Note 3: Outputs are terminated through a 50Ω Resistor to V_{CC} − 2.0V.

Note: Devices are designed to meet the DC specifications after thermal equilibrium has been established. Circuit is tested with air flow greater than 500LFPM maintained.

TTL DC Electrical Characteristics V_{CC} = 5.0V; GND = 0.0V (Note 4); T_A = −40°C to +85°C

Symbol	Parameter	Min	Typ	Max	Units	Condition
I_{IH}	Input HIGH Current			20	µA	V_{IN} = 2.7V
				100		V_{IN} = V_{CC}
I_{IL}	Input LOW Current			−200	µA	V_{IN} = 0.5V
V_{IK}	Clamp Diode Voltage			−1.2	V	I_{IN} = −18 mA
V_{IH}	Input HIGH Voltage	2.0			V	
V_{IL}	Input LOW Voltage			0.8	V	

Note 4: V_{CC} can vary +0.5V/−0.8V.

AC Electrical Characteristics V_{CC} = 5.0V; GND = 0.0V (Note 5)

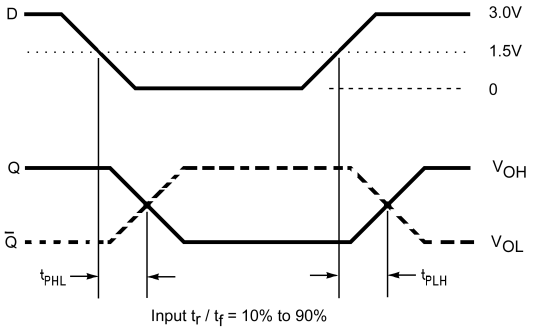
Symbol	Parameter	−40°C			25°C			85°C			Units	Figure Number
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
f_{MAX}	Maximum Input Frequency		TBD			TBD			TBD		MHz	
t_{JITTER}	Cycle-to-Cycle Jitter		TBD			TBD			TBD		ps	
t_{PLH}, t_{PHL}	Propagation Delay to Output (Note 6)	100		600	100		600	100		600	ps	Figure 1
t_r, t_f	Output Rise Time/Fall Times (20% to 80%)	200		500	200		500	200		500	ns	Figure 2
t_{skpp}	Part to Part Skew			500			500			500	ps	
t_{skew}	Within Device Skew (Note 7)			100			100			100	ps	

Note 5: V_{CC} can vary +0.5V/−0.8V.

Note 6: Specifications for standard TTL input signal (see Figure 1).

Note 7: Within-device skew is defined as identical transitions on similar paths through a device.

Switching Waveforms



Note: V_M varies 1:1 with V_{EE}

FIGURE 1. TTL to Differential PECL Propagation Delay

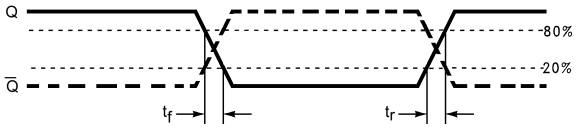
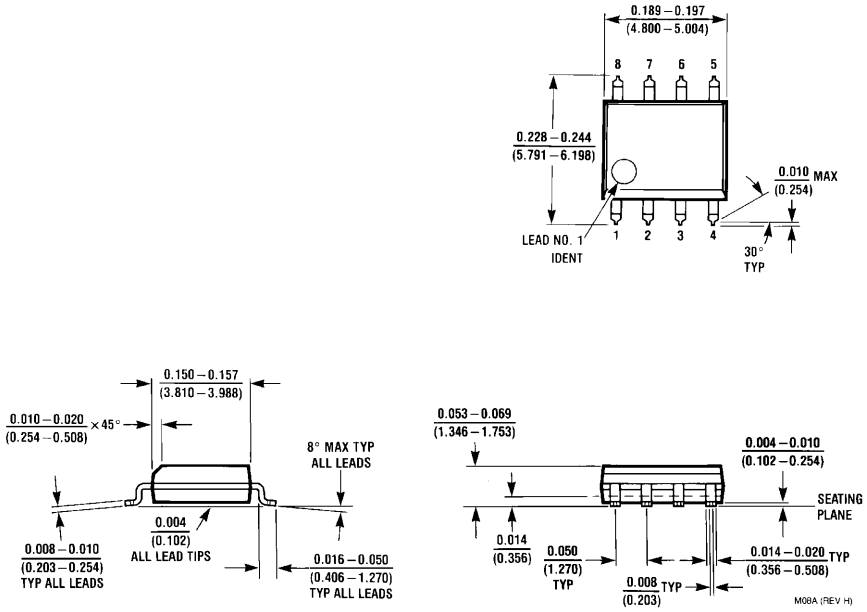


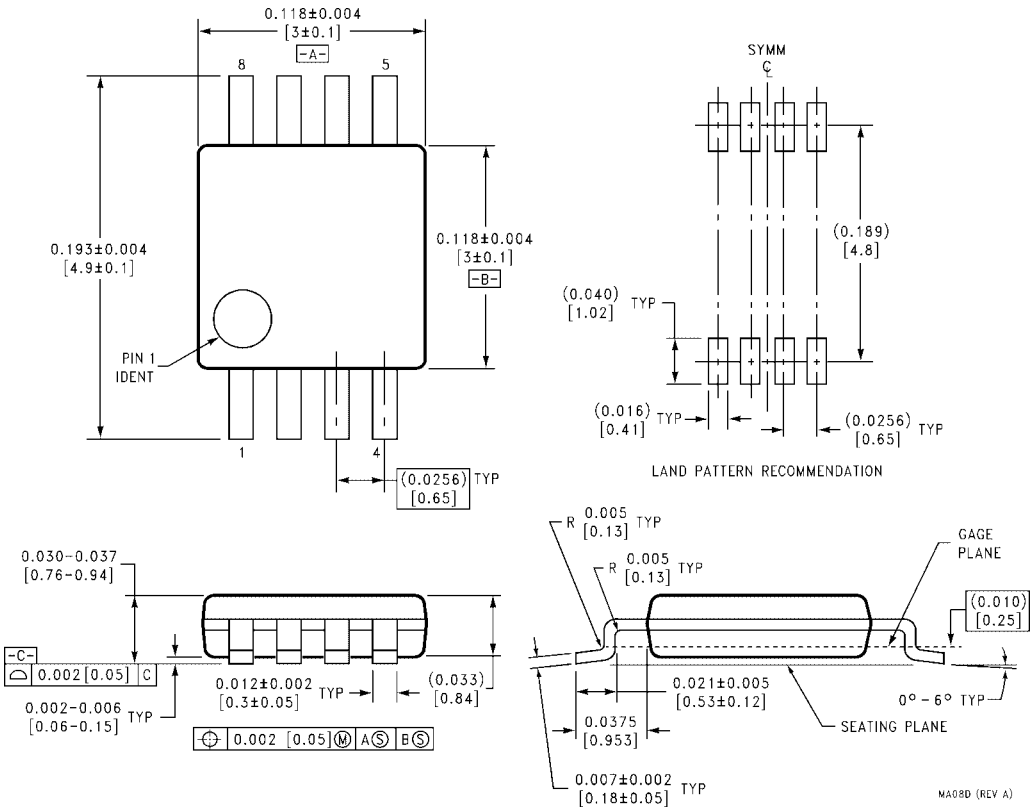
FIGURE 2. Differential Output Edge Rates

Physical Dimensions inches (millimeters) unless otherwise noted



8-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M08A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



8-Lead Molded Small Outline Package (MSOP), JEDEC MO-187, 3.0mm Wide
Package Number MA08D