MAXIM

CMOS 12-Bit A/D Converters With Track-and-Hold

General Description

The MAX163, MAX164, and MAX167 are complete CMOS sampling 12-bit analog-to-digital converters (ADCs) that combine an on-chip track-and-hold and voltage reference along with high conversion speed and low power consumption. A conversion time of 8.33µs includes settling time for the track-and-hold. An internal buried zener reference provides low drift with low noise.

The three A/Ds differ only in their analog input range. The MAX163 accepts 0V to +5V inputs, the MAX164 accepts -5V to +5V inputs, and the MAX167's input range is -2.5V to +2.5V. External components are limited to only decoupling capacitors for the power supply and reference voltages. On-chip clock circuitry can either be driven from an external clock source or a crystal.

The MAX163/164/167 employ a standard microprocessor interface. Three-state data outputs can be configured for 8- or 12-bit data buses. Data access and bus release timing specs are compatible with most popular microprocessors without resorting to wait states.

Applications

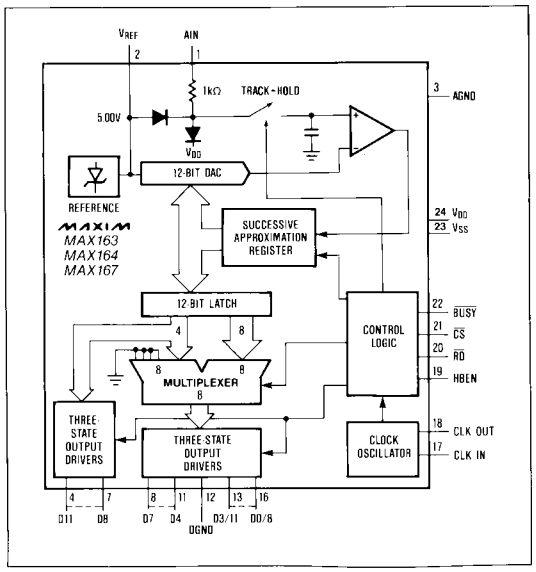
Digital Signal Processing (DSP)

Audio and Telecom Processing

High Accuracy Process Control

High Speed Data Acquisition

Functional Diagram



Features

- ◆ 12-Bit Resolution
- ◆ 8.33µs Conversion Time
- ◆ Internal Analog Track-Hold
- ◆ 6MHz Full Power Bandwidth
- ◆ On-Chip Voltage Reference
- ◆ High Input Resistance (500MΩ)
- ◆ 100ns Data Access Time
- ◆ 180mW (Max) Power Consumption
- ◆ AD7572/MAX162/MAX172 Plug-In Replacement
- ◆ 24 Lead Narrow DIP and SO Packages

Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX167ACNG	0°C to +70°C	Plastic DIP	±½ LSB
MAX167BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX167CCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX167ACWG	0°C to +70°C	Wide SO	±½ LSB
MAX167BCWG	0°C to +70°C	Wide SO	±1 LSB
MAX167CCWG	0°C to +70°C	Wide SO	±1 LSB
MAX167AEWG	-40°C to +85°C	Wide SO	±½ LSB
MAX167BEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX167CEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX167CC/D	0°C to +70°C	Dice**	±1 LSB
MAX167AENG	-40°C to +85°C	Plastic DIP	±½ LSB

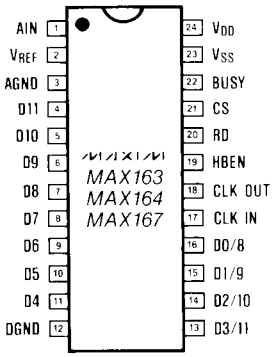
** All devices—24 lead packages*

***Consult factory for dice specifications*

Ordering information continued on last page.

Pin Configuration

Top View



Call toll free 1-800-998-8800 for free samples or literature.

CMOS 12-Bit A/D Converters With Track-and-Hold

ABSOLUTE MAXIMUM RATINGS

V_{DD} to DGND ..... -0.3 to +7V
V_{SS} to DGND ..... +0.3V to -17V
AGND to DGND ..... -0.3V to V_{DD} +0.3V
AIN to AGND ..... -15V to +15V
Digital Input Voltage to DGND ..... -0.3V to V_{DD} +0.3V
(Pins 17, 19-21)
Digital Output Voltage to DGND ..... -0.3V to V_{DD} +0.3V
(Pins 4-11, 13-16, 18, 22)

Operating Temperature Ranges
MAX16XXC ..... 0°C to +70°C
MAX16XXE ..... -40°C to +85°C
MAX16XXM ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +160°C
Power Dissipation (any Package) 1000mW
Derates Above +75°C by ..... 10mW/°C
Lead Temperature (Soldering 10 seconds) ..... +300°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not

ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, Slow Memory Mode (see text), T_A = T_{MIN} to T_{MAX}, f_{CLK} = 1.6MHz unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY							
Resolution				12			Bits
Integral Non-Linearity	INL	MAX16XB, MAX16XC MAX167A				±1 ±1/2	LSB
Differential Non-Linearity	DNL	Guaranteed Monotonic Over Temperature				±1	LSB
Offset Error (Note 1)		MAX163 MAX164, MAX167				±4 ±6	LSB
Full Scale Error (Note 2)		T_A = 25°C, Includes Reference Error				±10	LSB
Full Scale Tempco (Notes 3, 5)		Excludes Internal Reference Drift				±5	ppm/°C
Conversion Time	t_{CONV}	Synchronous (12.5 Clock Cycles) (13 Clock Cycles)				7.81 8.13	µs
Clock Frequency	f_{CLK}			0.1		1.6	MHz
DYNAMIC ACCURACY (Sample Rate = 100kHz)							
Signal to Noise plus Distortion Ratio	S/(N+D)	10kHz Input Signal, T_A = 25°C		70			dB
Total Harmonic Distortion (up to the 5th harmonic)	THD	10kHz Input Signal, T_A = 25°C	MAX167			-80	dB
			MAX163, MAX164			-76	
Peak Harmonic or Spurious Noise		10kHz Input Signal, T_A = 25°C	MAX167			-80	dB
			MAX163, MAX164			-76	
Full Power Sampling Bandwidth		In Track Mode, Under Sampled Waveform			6		MHz
ANALOG INPUT							
Input Voltage Range (Note 4)		MAX163 MAX164 MAX167		0 -5 -2.5		+5 +5 +2.5	V
Input Leakage Current						±1	µA
Input Capacitance (Note 5)						20	pF
Track-Hold Acquisition Time				1			µs

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +5V ±5%, V_{SS} = -11.4V to -15.75V, Slow Memory Mode (see text), T_A = T_{MIN} to T_{MAX}, f_{CLK} = 1.6MHz unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REFERENCE						
V_{REF} Output Voltage		T_A = 25°C	-4.98	-5.00	-5.02	V
V_{REF} Output Tempco (Note 6)		MAX16XB, MAX16XA MAX16XC			25 45	ppm/°C
Reference Load Sensitivity		ΔFS/ΔI_{REF}, I_{REF} Load Change: 0 to 5mA		0.2	1	LSB/mA
Output Sink Current					5	mA
LOGIC INPUTS						
Input Low Voltage	V_{IL}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN			0.8	V
Input High Voltage	V_{IH}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN	2.4			V
Input Capacitance (Note 5)	C_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN, CLK IN			10	pF
Input Current	I_{IN}	V_{IN} = 0V to V_{DD} — $\overline{CS}$, $\overline{RD}$, HBEN V_{IN} = 0V to V_{DD} — CLK IN			10 20	μA
LOGIC OUTPUTS						
Output Low Voltage	V_{OL}	D11-D0/8, $\overline{BUSY}$, CLK OUT I_{SINK} = 1.6mA			0.4	V
Output High Voltage	V_{OH}	D11-D0/8, $\overline{BUSY}$, CLK OUT I_{SOURCE} = 200μA	4			V
Three-State Leakage Current	I_L	D11-D0/8, V_{OUT} = 0V to V_{DD}			±10	μA
Three-State Output Capacitance	C_O	(Note 5)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}	±5% For Specified Performance		5		V
Negative Supply Voltage	V_{SS}	±5% For Specified Performance	-12		-15	V
Positive Supply Rejection		FS Change, V_{SS} = -15V or -12V V_{DD} = 4.75V to 5.25V		±1/2		LSB
Negative Supply Rejection		FS Change, V_{DD} = 5V V_{SS} = -14.25V to -15.75V V_{SS} = -11.4V to -12.6V		±1/8 ±1/8		LSB
Positive Supply Current	I_{DD}	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		4	6	mA
Negative Supply Current	I_{SS}	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN = 5V		7	10	mA
Power Dissipation		V_{DD} = +5V, V_{SS} = -12V		104	150	mW

Note 1: Typical change over temp is ±1 LSB.
Note 2: Ideal last code transition = FS - 3/2 LSB, adjusted for offset.
Note 3: Full Scale Tempco = ΔFS/ΔT, where ΔFS is full scale change from T_A = 25°C to T_{MIN} or T_{MAX}.
Note 4: V_{IN} must not exceed V_{DD} for specified accuracy.
Note 5: Guaranteed by design, not subject to test.
Note 6: V_{REF} Tempco = ΔV_{REF}/ΔT, where ΔV_{REF} is reference voltage change from T_A = 25°C to T_{MIN} or T_{MAX}.

CMOS 12-Bit A/D Converters With Track-and-Hold

TIMING CHARACTERISTICS (See Figures 9-12)

(V_{DD} = +5V, V_{SS} = -12V or -15V, T_A = T_{MIN} to T_{MAX}, Note 7, specifications in bold type are 100% tested, others are guaranteed by design, unless otherwise noted).

PARAMETER	SYMBOL (Figures 9-12)	CONDITIONS	T_A = 25°C MIN	TYP	MAX	MAX16XXC/E MIN	MAX	MAX16XXM MIN	MAX	UNITS
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			0		0		ns
$\overline{RD}$ to $\overline{BUSY}$ Delay (Note 8)	t_2	CL = 50pF		**80**	**170**		**220**		**260**	ns
Data Access Time (Notes 8, 9)	t_3	CL = 100pF		**50**	**100**		**130**		**150**	ns
$\overline{RD}$ Pulse Width	t_4		100			130		150		ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			0		0		ns
Data Setup Time After $\overline{BUSY}$ (Notes 8, 9)	t_6			**40**	**80**		**105**		**120**	ns
Bus Relinquish Time (Notes 8, 10)	t_7			**30**	**50**		**65**		**75**	ns
HBEN to $\overline{RD}$ Setup Time	t_8		0			0		0		ns
HBEN to $\overline{RD}$ Hold Time	t_9		0			0		0		ns
Delay Between READ Operations	t_{10}		200			200		200		ns
Delay Between Conversions	t_{11}		1			1		1		µs
Aperture Delay	t_{12}	Jitter < 50ps		25						ns
CLK to $\overline{BUSY}$ Delay	t_{13}			80	170		220		260	ns

Note 7: All input control signals are specified with t_r = t_f = 5ns (10% to 90% of +5V) and timed from a voltage level of +1.6V.
Note 8: This specification is 100% production tested.
Note 9: t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
Note 10: t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.

CMOS 12-Bit A/D Converters With Track-and-Hold

Pin Description

PIN	NAME	FUNCTION
1	AIN	Sampling Analog Input, MAX163: 0V to +5V Unipolar MAX164: ±5V Bipolar MAX167: ±2.5V Bipolar
2	V_{REF}	-5.00V Reference Output
3	AGND	Analog Ground
4-11	D11-D4	Three-State Data Outputs
12	DGND	Digital Ground
13-16	D3/11-D0/8	Three-State Data Outputs
17	CLK IN	Clock Input. An external TTL compatible clock may be connected, or a crystal may be connected between CLK IN and CLK OUT.
18	CLK OUT	Clock Output. An inverted CLK IN signal appears at this pin.
19	HBEN	High Byte Enable Input. Used to multiplex the internal 12-bit conversion result into the lower order outputs (D7-D0/8). HBEN also disables conversion starts when HIGH.
20	$\overline{RD}$	READ Input. This active low input starts a conversion when $\overline{CS}$ and HBEN are low. $\overline{RD}$ also enables the output drivers when $\overline{CS}$ is low.
21	$\overline{CS}$	The CHIP SELECT Input must be low for the ADC to recognize $\overline{RD}$ and HBEN inputs.
22	$\overline{BUSY}$	The $\overline{BUSY}$ Output is low when a conversion is in progress.
23	V_{SS}	Negative Supply, -15V or -12V
24	V_{DD}	Positive Supply, +5V

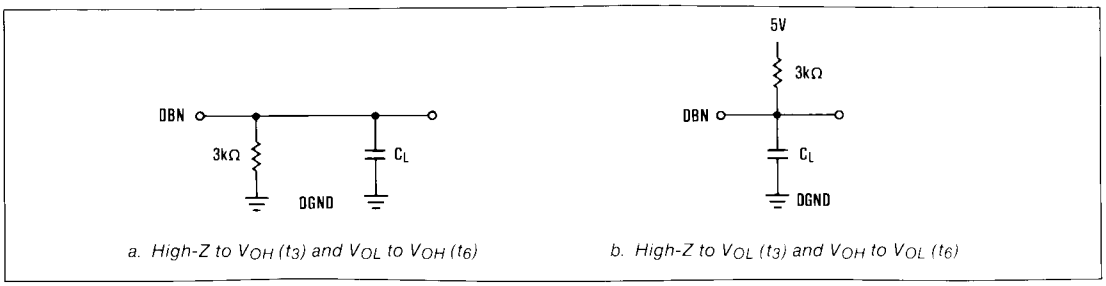
A/D Converter Operation

The MAX163/164/167 use successive approximation and input track-and-hold circuitry to convert an analog signal to a series of 12-bit digital output codes. The control logic provides easy interface to microprocessors so that most applications require only passive components to perform analog-to-digital conversions. No "hold" capacitor is required. Figure 3 shows the MAX163/164/167 in their simplest operational configuration.

Analog Input—Track-and-Hold

In Figure 4, the equivalent input circuit illustrates the sampling architecture of the ADC's analog comparator. The comparator's input capacitance acts as the "hold" capacitor and must be completely charged by the input signal with every A/D conversion (but NOT every clock cycle). The capacitance is charged through an internal 1kΩ protection resistor in series with the input.

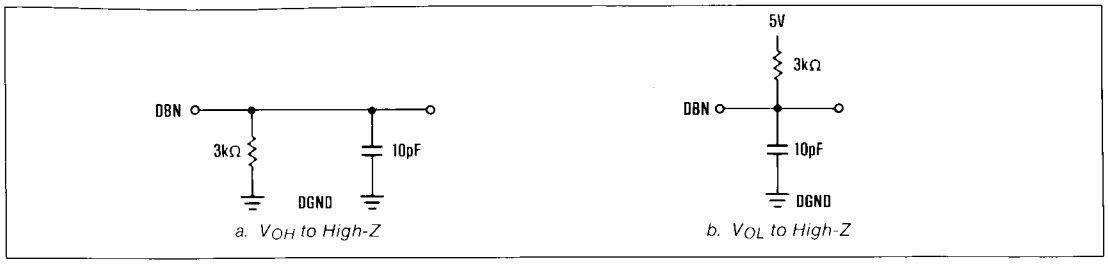
To an input signal, AIN appears as a capacitor switching between analog ground and the input signal. Between conversions (BUSY high and $\overline{RD}$ or $\overline{CS}$ or HBEN high) the capacitor is connected to AIN. When a conversion starts, the capacitor disconnects from AIN, thus sampling the input, and is internally discharged. At the end of the conversion it reconnects to the input and charges to the input signal. The loading effect of AIN on the analog signal is such that a high speed input buffer is usually NOT needed. This is because the A/D disconnects from the input during the actual conversion.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)

b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z

b. V_{OL} to High-Z

Figure 2. Load Circuits for Bus Relinquish Time

CMOS 12-Bit A/D Converters With Track-and-Hold

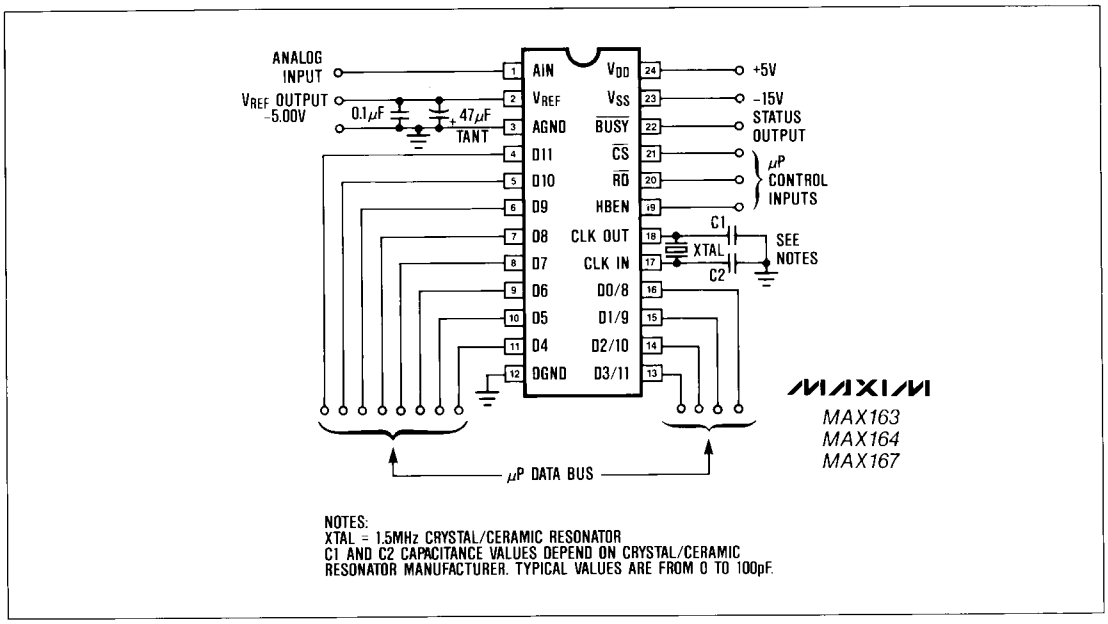


Figure 3. MAX163/164/167 Operational Diagram

The track-and-hold enters its "tracking" mode when the ADC is deselected (CS high) and BUSY is high. "Hold" mode starts approximately 25ns after a conversion is initiated. The variation in this delay from one conversion to the next (aperture jitter) is less than 50ps. Figures 9 through 12 detail the track-and-hold and interface timing for the various interface modes. The internal track-and-hold control logic is shown in Figure 5.

The time required for the track-and-hold to acquire an input signal is a function of how quickly the input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. Acquisition time is calculated by:

$t_{ACQ} = 10(R_S + R_{IN})20pF$ (but never less than $1\mu s$)

Where $R_{IN} = 1k\Omega$, and R_S = source impedance of the ADC's input signal.

Input Bandwidth

The A/D's input tracking circuitry has excellent large signal and wide bandwidth behavior. It is not slew limited like many other ADC track-and-holds. Remarkably, the MAX163/164/167 track-and-hold's full power bandwith is typically 6MHz. This makes it possible to digitize high speed transient events and to measure periodic signals whose bandwidth exceeds the ADC's sample rate (>100kHz) by using under sampling techniques. It is important to note here that if under sampling is used to measure high frequency signals, special care must be taken to avoid aliasing errors. Without adequate input filtering, high frequency noise may be aliased into the measurement band.

Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and V_{REF}, work with an internal series resistance to allow over drives of up to ±15V at AIN

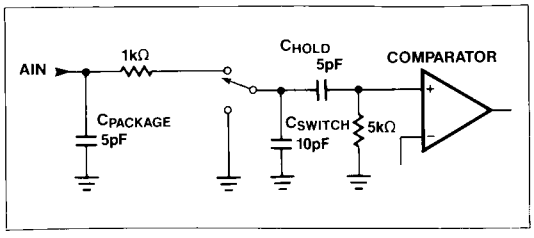


Figure 4. Equivalent Input Circuit

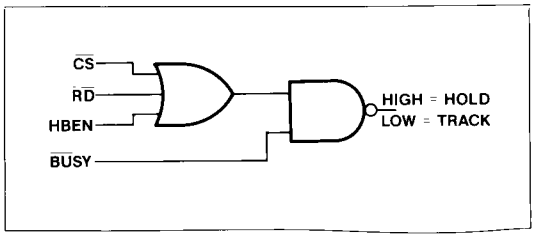


Figure 5. Track-Hold Internal Control Logic

with no risk of damage to the A/D. However, for accurate conversions near full scale (MAX163 and MAX164 only), AIN should not exceed V_{DD} because A/D accuracy is affected while the protection diodes are even slightly turned on.

Starting a Conversion

The ADC is controlled by the $\overline{CS}$, $\overline{RD}$ and HBEN inputs. The track-and-hold enters Hold Mode and a conversion starts at the falling edge of CS and RD while HBEN is low. The BUSY output goes low as soon as the conversion starts. On the falling edge of the 13th input clock pulse after the conversion starts, BUSY goes high and the conversion result is latched into three-state output buffers.

Internal/External Clock

Figure 6 shows the MAX163/164/167 clock circuitry. The capacitive load on the CLK OUT pin must be minimized to avoid digital coupling of the CLK OUT buffer currents to the ADC's analog comparator. If an external clock source drives CLK IN, then CLK OUT should be left open. Acceptable external clock duty cycles are between 20% and 80%, so a precise square wave is not required. If the internal oscillator is used, a crystal or ceramic resonator is connected between CLK OUT and CLK IN as shown in Figure 6.

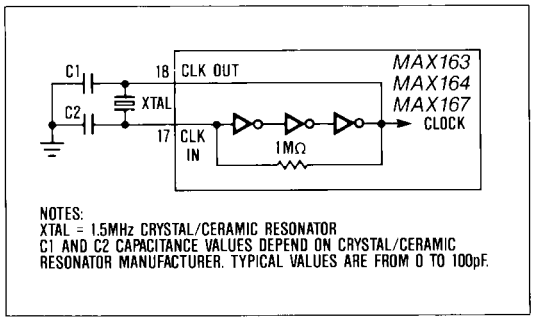


Figure 6. Internal Clock Circuit

Internal Reference

The MAX163/164/167 have a -5.00V buried zener reference which biases the internal DAC. The reference output is available at V_{REF} (Pin 2) and should be bypassed to AGND (Pin 3) with a 47µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor. This minimizes noise and maintains a low impedance at high frequencies. A resistor should NOT be connected between the bypass capacitors and Pin 2. The internal reference output buffer can sink up to 5mA.

Digital Interface

Clock and Control Synchronization

For best analog performance, the MAX163/164/167 clock should be synchronized to the RD and CS control inputs as shown in Figure 7, with at least 100ns separating convert start from the nearest clock edge. This ensures that transitions at CLK IN and CLK OUT do not couple to the analog input and get sampled by the track-and-hold. The magnitude of this feedthrough is only a few millivolts, but if CLK and convert start ($\overline{CS}$ and $\overline{RD}$) are asynchronous, frequency components caused by mixing of the clock and convert signals may increase the apparent input noise.

When the clock and convert signals are synchronized, small endpoint errors (offset and full scale) are the most that can be generated by clock feedthrough. Even these errors (which can be trimmed out) can be eliminated by ensuring that the start of a conversion ($\overline{RD}$ and $\overline{CS}$ falling edge) does not occur within 100ns of a clock transition, as in Figure 7. Nevertheless, even without observing this guideline, the MAX163/164/167 are still compatible with either the MAX162/172 or the MX7572 synchronization modes, with no increase in linearity error. This means that either the falling or rising edge of CLK IN may be near $\overline{RD}$'s falling edge.

Output Data Format

The 12 data bits can be output either in full parallel or as two 8-bit bytes. The data bus output format is shown in Table 1. To obtain parallel output for 16-bit processors, HBEN is permanently tied low. The output data, DB11-DB0, is then right justified, i.e., DB0, the LSB, is the right most bit in the 16-bit word.

For a two byte read, outputs D7 through D0/8 are used. Byte selection is controlled by HBEN which multiplexes the data outputs. When HBEN is low, the lower 8 bits are presented at the data outputs. When HBEN is high, the upper 4 bits are presented at DB0-DB3 with the leading 4 bits low in locations D4-D7. Note that the 4 MSBs always appear at D11-D8 whenever the outputs are enabled, regardless of the state of HBEN.

Timing And Control

Conversion start and data read operations are controlled by three digital inputs, HBEN, $\overline{CS}$ and $\overline{RD}$. Figure 8 shows the logic equivalent for the conversion and data output control circuitry. A logic low is required on all three inputs to start a conversion and once the conversion is in progress, it cannot be re-started. $\overline{BUSY}$ remains low during the entire conversion cycle.

Two modes of operation are outlined in the timing diagrams of Figures 9-12. Slow Memory Mode is intended for processors that can be forced into a WAIT state during the ADC's conversion time. ROM Mode is for processors that cannot be forced into a wait state. In both modes, a processor READ operation to the ADC address starts the conversion. In the ROM mode, a second READ operation accesses the conversion result.

CMOS 12-Bit A/D Converters With Track-and-Hold

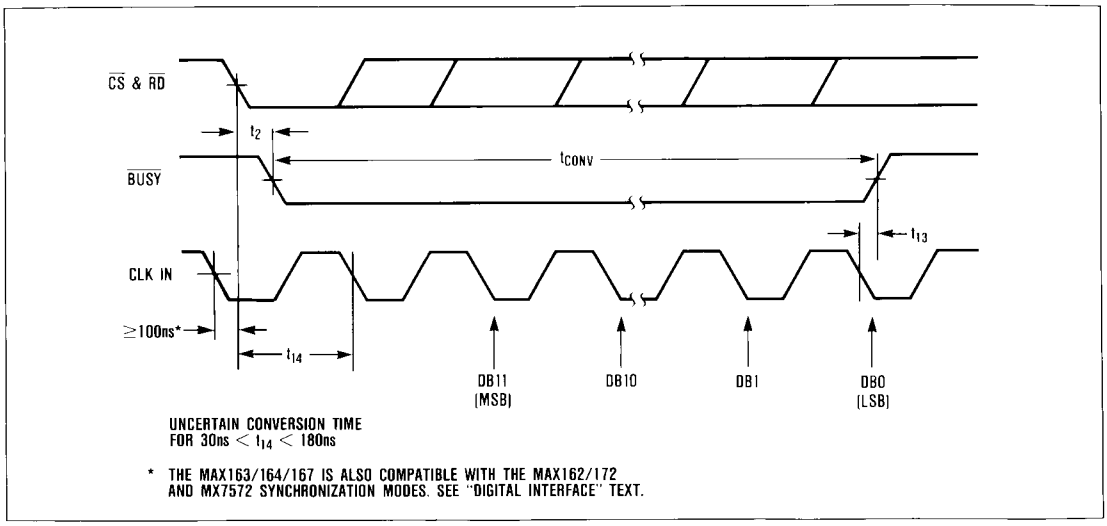


Figure 7. $\overline{RD}$ and CLK IN for Synchronous Operation

Table 1. Data Bus Output, $\overline{CS}$ & $\overline{RD}$ = LOW

	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
MNEMONIC*	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
HBEN = LOW	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
HBEN = HIGH	DB11	DB10	DB9	DB8	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

Note: *D11 ... D0/8 are the ADC data output pins.
DB11 ... DB0 are the 12-bit conversion results, DB11 is the MSB.

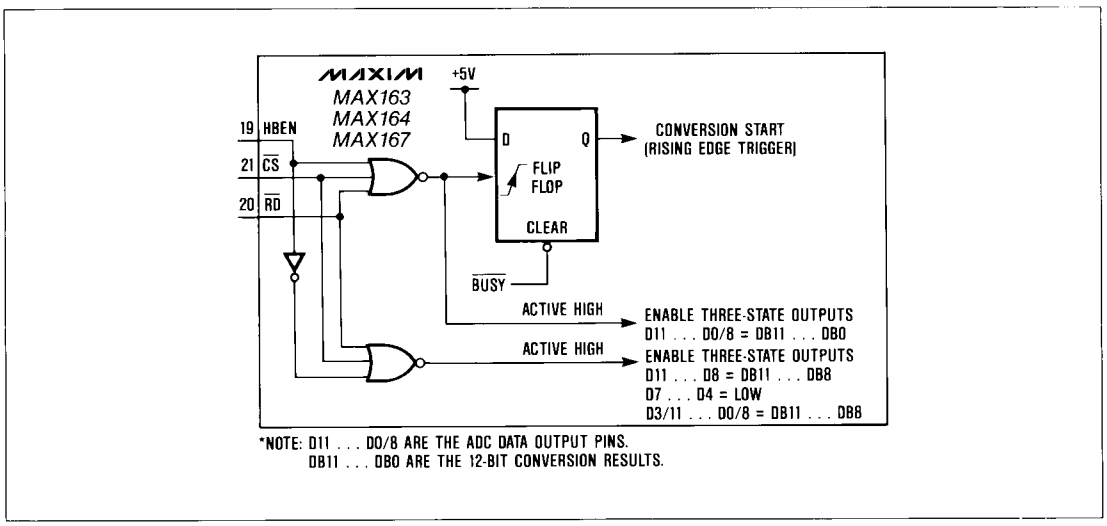


Figure 8. Logic Equivalent for $\overline{RD}$, $\overline{CS}$ and HBEN Inputs

Slow Memory Mode, Parallel Read (HBEN = LOW)

See Figure 9 and Table 2. Taking $\overline{CS}$ and $\overline{RD}$ low starts the conversion. $\overline{BUSY}$ remains low while the conversion is in progress. The PREVIOUS (old) result appears at the digital outputs until the end of the conversion when $\overline{BUSY}$ returns high. The output latches are then updated with the newest result on D11-D0/8.

Slow Memory Mode, Two Byte Read

See Figure 10 and Table 3. Outputs D7-D0/8 are used for a two byte read. The start and read operations for the 8 LSBs are identical to the Slow Memory Mode, Parallel Read. A second read operation with HBEN high places the 4 MSBs, with 4 leading zeros, on data outputs D7-D0/8. This second read operation does not start another conversion since HBEN is high.

ROM Mode, Parallel Read (HBEN = LOW)

See Figure 11 and Table 4. ROM Mode avoids using processor wait states. A conversion starts with a read operation and the 12 data bits from the PREVIOUS conversion appear at D11-D0/8. The data from the first read in a sequence is often disregarded when this interface mode is used. A second read accesses the results of the first conversion and also starts a new conversion. The time between successive READs must be longer than the MAX163/164/167 conversion times.

ROM Mode, Two Byte Read

See Figure 12 and Table 5. As in the Slow Memory Mode, only D7-D0/8 are used for two byte reads. A conversion starts with a read operation with HBEN low. At this point the data outputs contain the 8 LSBs from the PREVIOUS conversion. Two more read operations are needed to access the conversion result. The first occurs with HBEN high, where the 4 MSBs with 4 leading zeros are accessed. The second read, with HBEN low, outputs the 8 LSBs and also starts a new conversion.

Application Hints

Initialization After Power Up

In some applications it may be desirable to remove power from the ADC during periods of inactivity. This is increasingly common in battery powered systems. To initialize the MAX163/164/167 at power up, perform a read operation with HBEN low and ignore the data outputs.

Digital Bus Noise

If the data bus connected to the ADC is active during a conversion, errors can be caused by coupling from the data pins to the ADC comparator. Using the Slow Memory Mode avoids this problem by placing the processor in a wait state during the conversion. In the ROM Mode, if the data bus is going to be active during the conversion, the bus should be isolated from the ADC using three-state drivers.

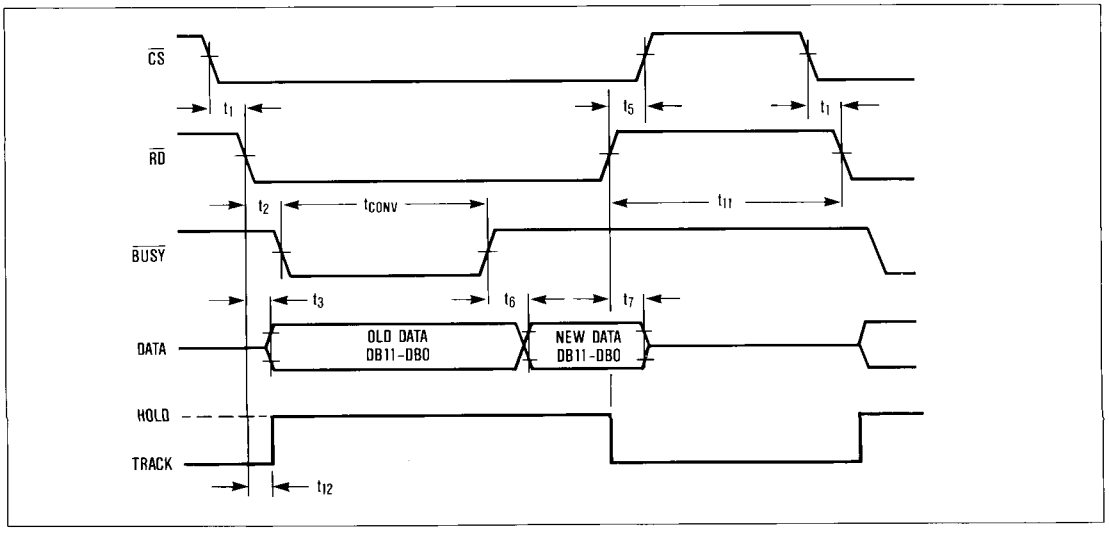


Figure 9. Slow Memory Mode, Parallel Read Timing Diagram

Table 2. Slow Memory Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

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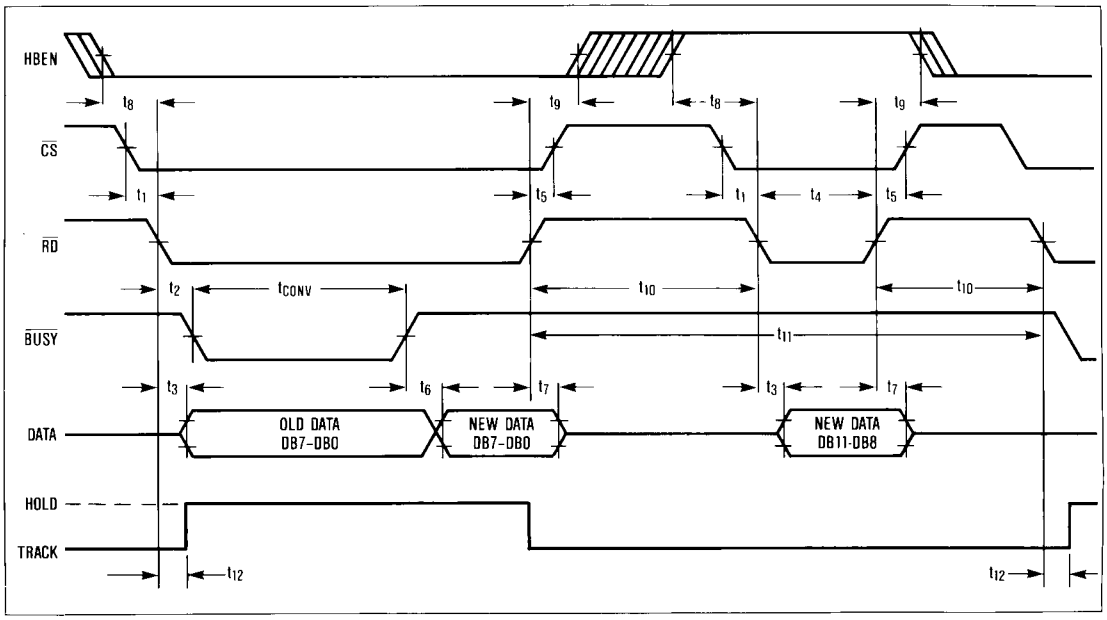

Figure 10. Slow Memory Mode, Two Byte Read Timing Diagram

Table 3. Slow Memory Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8

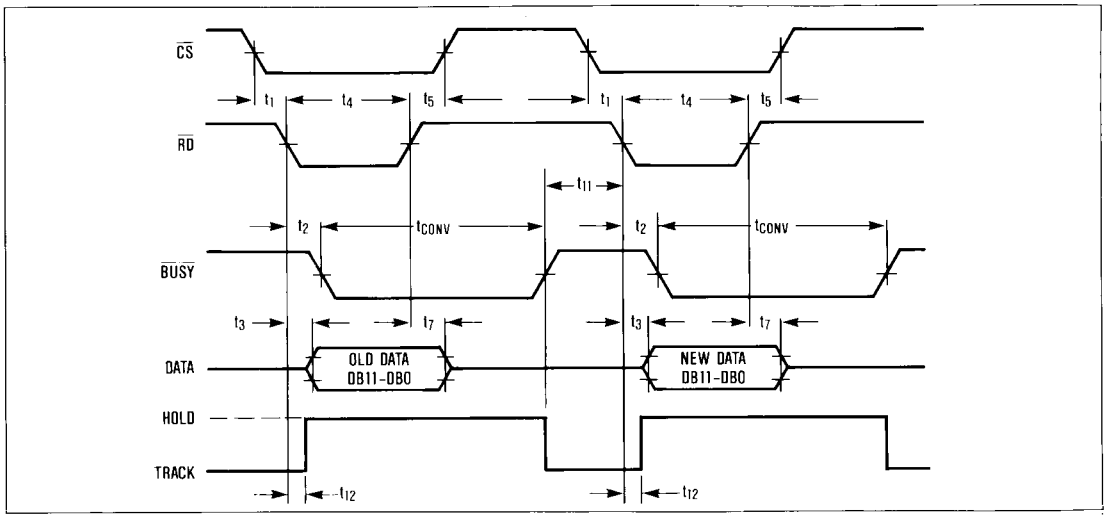

Figure 11. ROM Mode, Parallel Read Timing Diagram

Table 4. ROM Mode, Parallel Read Data Bus Status

Data Outputs	D11	D10	D9	D8	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

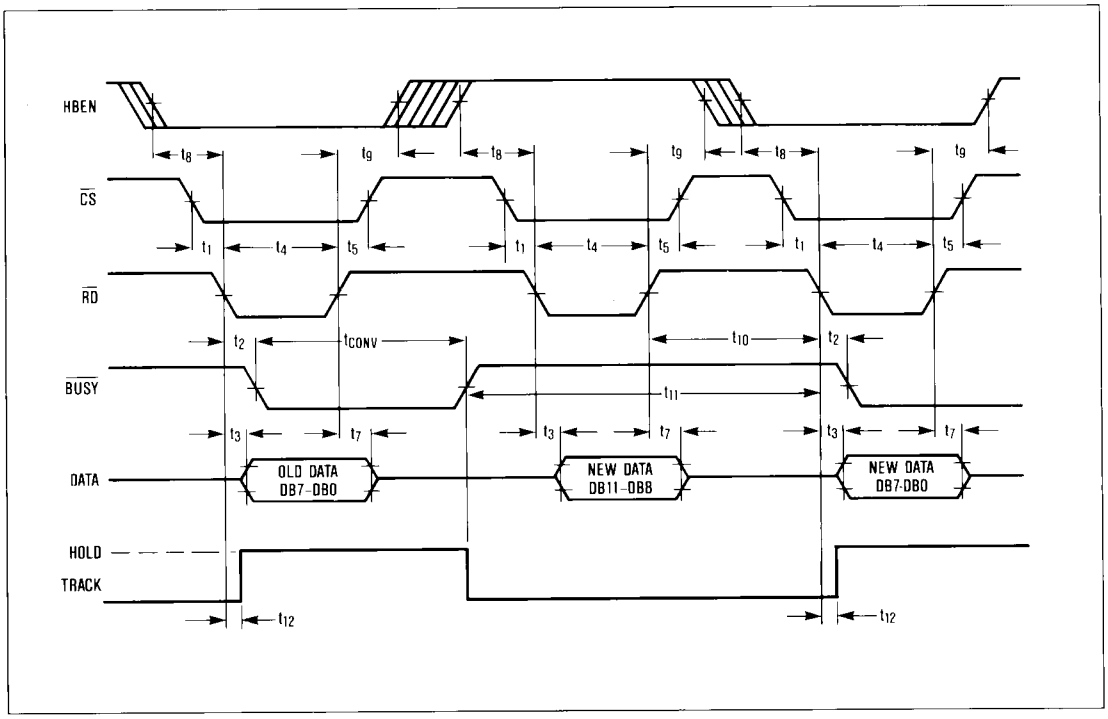

Figure 12. ROM Mode, Two Byte Read Timing Diagram

Table 5. ROM Mode, Two Byte Read Data Bus Status

Data Outputs	D7	D6	D5	D4	D3/11	D2/10	D1/9	D0/8
First Read (Old Data)	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Second Read	LOW	LOW	LOW	LOW	DB11	DB10	DB9	DB8
Third Read	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

In ROM Mode, considerable digital noise is generated in the ADC when $\overline{RD}$ or $\overline{CS}$ go high and the output data drivers are disabled after a conversion is started. This noise can affect the ADC comparator and cause large errors if it coincides with the time the SAR is latching a comparator decision. To avoid this problem, $\overline{RD}$ and $\overline{CS}$ should be active for less than one clock cycle. If this is not possible, $\overline{RD}$ or $\overline{CS}$ must go high at a rising edge of CLK IN, since the comparator output is always latched at falling edges of CLK IN.

Layout, Grounding, Bypassing

For best system performance printed circuit boards should be used. Wire wrap boards are not recommended. The layout of the board should ensure that digital and analog signal lines are kept separated from each other as much as possible. Care should be taken not to run analog and digital (especially clock) lines parallel to one another or digital lines underneath the ADC package.

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Figure 13 shows the recommended system ground connections. A single point analog STAR ground should be established at Pin 3 (AGND) separate from the logic ground. All other analog grounds and Pin 12 (DGND) should be connected to this STAR ground and no other digital system grounds should be connected here. The ground return to the power supply from this STAR ground should be low impedance and as short as possible for noise-free operation.

The high speed comparator in the ADC is sensitive to high frequency noise in the V_{DD} and V_{SS} power supplies. These supplies should be bypassed to the analog STAR ground with 0.1μF and 10μF bypass capacitors. Capacitor leads should have minimum length for best supply noise rejection. If the +5V power supply is very noisy, a small (4.7Ω-20Ω) resistor can be connected as shown in Figure 13 to filter this noise.

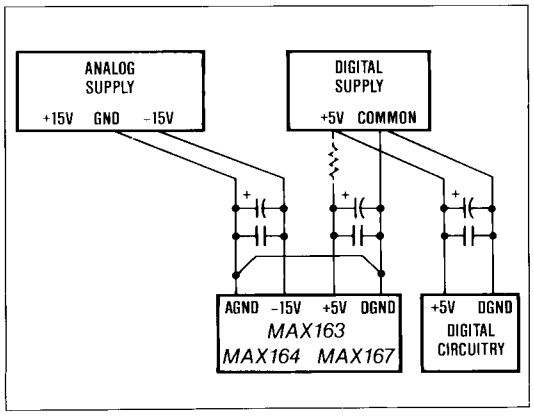

Figure 13. Power Supply Grounding Practice

Gain and Offset Adjustment

The plot in Figure 14 graphs the nominal unipolar input/output transfer function of the MAX163. Code transitions occur half way between successive integer LSB values. Output coding is natural binary with 1 LSB = 1.22mV (5V/4096). Figure 15 shows the bipolar input transfer function for the MAX164/167, where output coding is offset binary.

In applications where gain (full scale range) adjustment is required, the connection shown in Figure 16 provides ±0.5%, or ±20 LSBs, of adjustment range. If both offset and full scale range need adjustment, the circuit in Figure 17 is recommended. Offset should be adjusted before gain. For the MAX163 (0V to +5V input range), apply +1/2 LSB (0.61mV) to the analog input and adjust R12 so the digital output code changes between 0000 0000 0000 and 0000 0000 0001. To adjust full scale, apply FS - 1-1/2 LSB (4.99817V) and adjust R8 until the output code changes between 1111 1111 1110 and 1111 1111 1111. There may be slight interaction between adjustments. If an input gain of two is acceptable, the connection in Figure 17 can be simplified by removing R5 and R6.

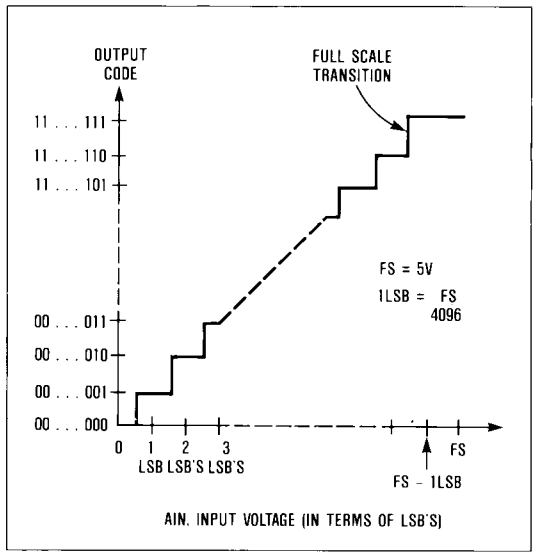

Figure 14. MAX163 Unipolar Transfer Function

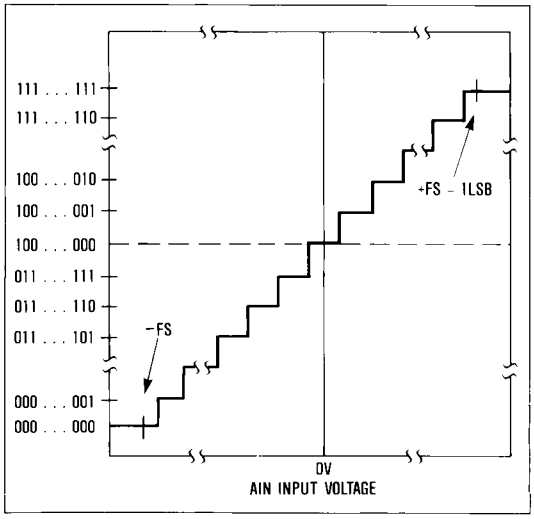

Figure 15. MAX164/167 Bipolar Transfer Function

To adjust bipolar offset (MAX164 ±5V, MAX167 ±2.5V), apply +1/2 LSB (1.22mV for MAX164, 0.61mV for MAX167) to the analog input and adjust R12 for output code flicker between 1000 0000 0000 and 1000 0000 0001. For full scale, apply FS - 1-1/2 LSB (+4.99634V for the MAX164, 2.49817V for the MAX167) to the input and adjust R8 so the output code flickers between 1111 1111 1110 and 1111 1111 1111. There may be some interaction between these adjustments.

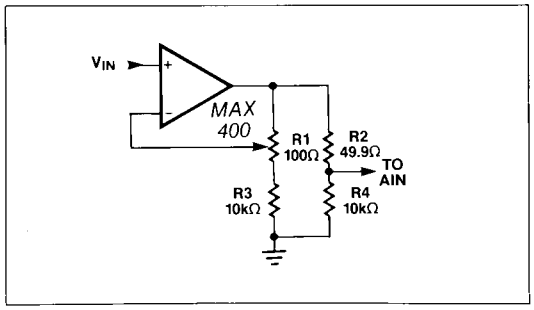

Figure 16. Trim Circuit for Gain Only (±0.5%)

Dynamic Performance

High speed sampling capability and 100kHz throughput make the MAX163/164/167 ideal for wideband signal processing. To support these and other related applications, FFT (Fast Fourier Transform) test techniques are used to guarantee the A/D's dynamic frequency response, distortion, and noise at the rated throughput. Specifically, this involves applying a low distortion sinewave to the ADC input and recording the digital conversion results for a specified time. The data is then analyzed using an FFT algorithm which determines its spectral content. Conversion errors are then seen as spectral elements outside of the fundamental input frequency.

A-to-D converters have traditionally been evaluated by specifications such as Zero and Full Scale Error, Integral Non-linearity (INL), and Differential Non-linearity (DNL). Such parameters are widely accepted for specifying performance with DC and slowly varying signals but are less useful in signal processing applications where the A/D's impact on the system transfer function is the main concern. The significance of various DC errors does not translate well to the dynamic case, so different tests are required.

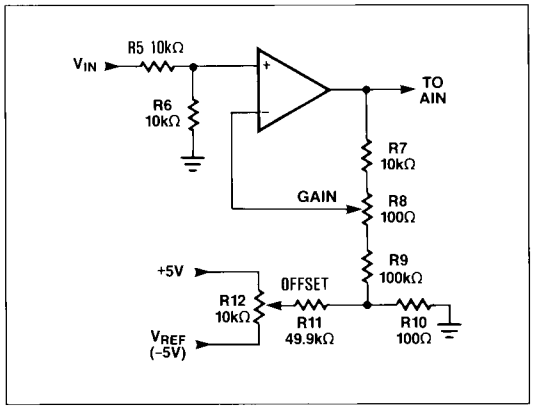

Figure 17. Offset (±20mV) and Gain (±0.5%) Trim Circuit

Signal-to-Noise Ratio and Effective Number of Bits

The ratio between the RMS amplitude of the fundamental input frequency to the RMS amplitude of all other A/D output signals is the Signal-to-Noise Ratio (SNR). The output band is limited to frequencies above DC and below one half the A/D sample (conversion) rate. This usually (but not always) includes distortion as well as noise components. For this reason the ratio is sometimes referred to as "Signal-to-Noise + Distortion".

The theoretical minimum A/D noise is caused by quantization error and is a direct result of the A/D's resolution: SNR = (6.02N + 1.76)dB, where N is the number of bits of resolution. A perfect 12-bit A/D can, therefore, do no better than 74dB. Figure 18 shows the result of sampling a pure 10kHz sinusoid at a 100kHz rate with the MAX167. An FFT plot of the output shows the output level in various spectral bands.

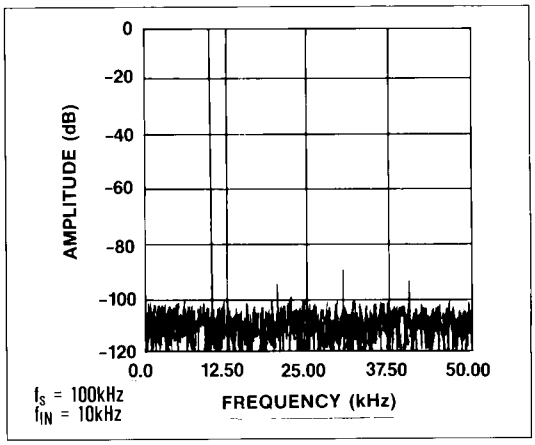

Figure 18. FFT Plot for the MAX167

By transposing the equation which converts resolution to SNR, we can, from the measured SNR, determine the effective resolution or the "Effective Number of Bits" that the A/D provides: N = (SNR - 1.76)/6.02. Figure 19 shows the effective number of bits as a function of the input frequency for the MAX167.

Total Harmonic Distortion

The ratio of the RMS sum of all harmonics of the input signal (in the frequency band above DC and below one half the sample rate) to the fundamental itself is Total Harmonic Distortion (THD). This is expressed as:

$$THD = 20Log\left[\sqrt{(V_2^2 + V_3^2 + V_4^2 + V_4^2 + ... + V_N^2)/V_1}\right]$$

where V_1 is the fundamental RMS amplitude and V_2 to V_N are the amplitudes of the 2nd through Nth harmonics.

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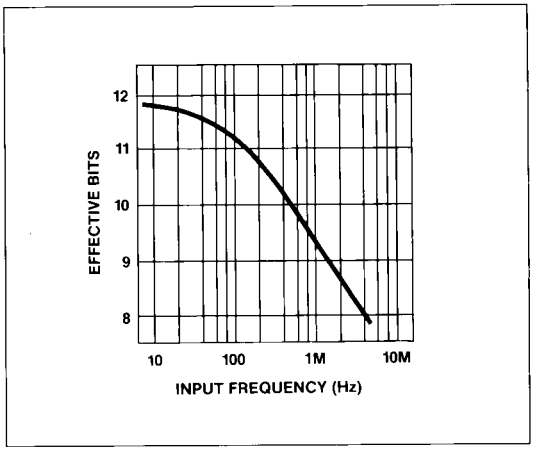
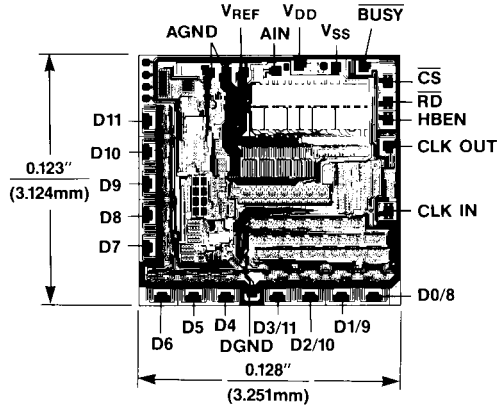


Figure 19. MAX167 Effective Bits vs. Input Frequency

Peak Harmonic or Spurious Noise

The ratio of the fundamental RMS amplitude to the amplitude of the next largest spectral component (in the frequency band above DC and below one half the sample rate) is referred to as the Peak Harmonic (or Spurious) Noise. Usually this peak occurs at some harmonic of the input frequency, but if the ADC is exceptionally linear, it may occur only at a random peak in the ADC's noise floor.

Chip Topography



Ordering Information (continued)

PART	TEMP. RANGE	PACKAGE*	ERROR
MAX167BENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX167CENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX167AMRG	-55°C to +125°C	CERDIP	±½ LSB
MAX167BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX167CMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX163BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX163CCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX163BCWG	0°C to +70°C	Wide SO	±1 LSB
MAX163CCWG	0°C to +70°C	Wide SO	±1 LSB
MAX163BEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX163CEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX163CC/D	0°C to +70°C	Dice**	±1 LSB
MAX163BENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX163CENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX163BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX163CMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX164BCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX164CCNG	0°C to +70°C	Plastic DIP	±1 LSB
MAX164BCWG	0°C to +70°C	Wide SO	±1 LSB
MAX164CCWG	0°C to +70°C	Wide SO	±1 LSB
MAX164BEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX164CEWG	-40°C to +85°C	Wide SO	±1 LSB
MAX164CC/D	0°C to +70°C	Dice**	±1 LSB
MAX164BENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX164CENG	-40°C to +85°C	Plastic DIP	±1 LSB
MAX164BMRG	-55°C to +125°C	CERDIP	±1 LSB
MAX164CMRG	-55°C to +125°C	CERDIP	±1 LSB

** All devices—24 lead packages*
***Consult factory for dice specifications*