UCC2915, UCC3915
15-V PROGRAMMABLE HOT SWAP POWER MANAGER

SLUS198C – FEBUARY 2000 - REVISED - JUNE 2001

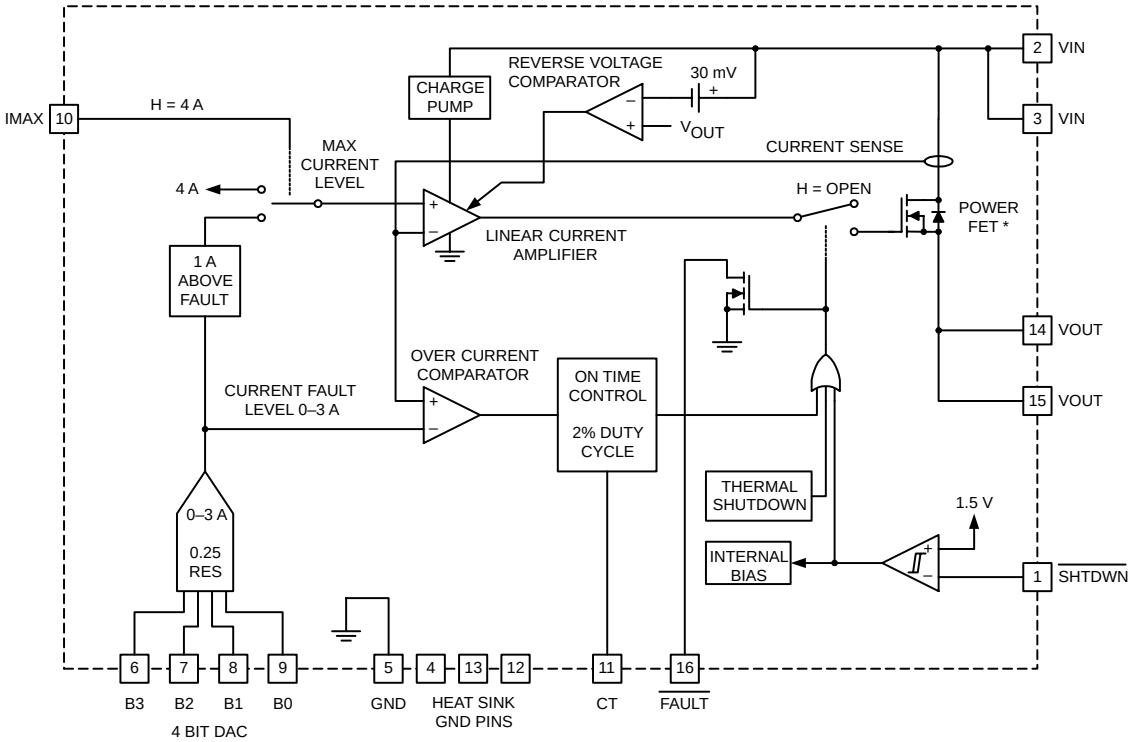
- **Integrated 0.15-Ω Power MOSFET**
- **7-V to 15-V Operation**
- **Digital-Programmable Current Limit from 0 A to 3 A**
- **100-μA I_{CC} When Disabled**
- **Programmable On Time**
- **Programmable Start Delay**
- **Fixed 2% Duty Cycle**
- **Thermal Shutdown**
- **Fault-Output Indicator**
- **Maximum-Output Current Can Be Set to 1 A Above the Programmed-Fault Level or to a Full 4 A**
- **Power SOIC and TSSOP, Low Thermal Resistance Packaging**

description

The UCC3915 programmable hot swap power manager provides complete power-management, hot-swap capability, and circuit breaker functions. The only external component required to operate the device, other than power supply bypassing, is the fault-timing capacitor, C_T. All control and housekeeping functions are integrated, and externally programmable. These include the fault current level, maximum output sourcing current, maximum fault time, and startup delay. In the event of a constant fault, the internal fixed 2% duty cycle ratio limits average output power.

The internal 4-bit DAC allows programming of the fault-level current from 0 A to 3 A with 0.25-A resolution. The IMAX control pin sets the maximum-sourcing current to 1 A above the trip level or to a full 4 A of output current for fast output capacitor charging. (continued)

block diagram



UDG-99174

NOTE: Pin numbers refer to DIL-16 and SOIC-16 packages.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

description (continued)

When the output current is below the fault level, the output MOSFET is switched on with a nominal ON resistance of 0.15 Ω. When the output current exceeds the fault level, but is less than the maximum-sourcing level, the output remains switched on, but the fault timer starts, charging CT. Once CT charges to a preset threshold, the switch is turned off, and remains off for 50 times the programmed fault time. When the output current reaches the maximum sourcing level, the MOSFET transitions from a switch to a constant current source.

The UCC3915 can be put into sleep mode, drawing only 100 μA of supply current. Other features include an open-drain fault-output indicator, thermal shutdown, undervoltage lockout, 7-V to 15-V operation, and low-thermal resistance SOIC and TSSOP power packages.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

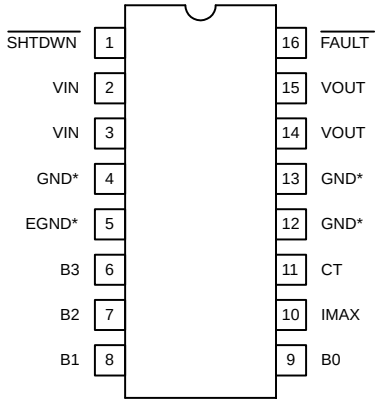
VIN	15.5 V
VOUT – VIN	.0.3 V
$\overline{\text{FAULT}}$ sink current	50 mA
$\overline{\text{FAULT}}$ voltage	–0.3 V to 8 V
Output current	Self limiting
TTL input voltage	–0.3 to VIN
Storage temperature, T_{stg}	–65°C to 150°C
Junction temperature, T_J	–55°C to 150°C
Lead temperature (soldering, 10 sec.)	300°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the *Interface Products Data Book* (TI Literature Number SLUD002) for thermal limitations and considerations of packages.

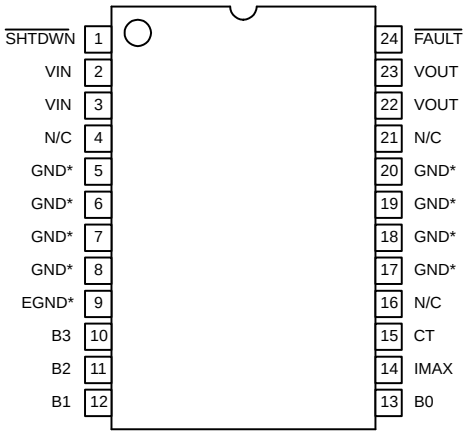
package information

DIL-16, SOIC-16
N, DP Package
(TOP VIEW)



*Pin 5 serves as lowest impedance to the electrical ground; Pins 4, 12, and 13 serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat. For N Package, pins 4, 12, and 13 are N/C.

TSSOP-24,
PWP Package
(TOP VIEW)



*Pin 9 serves as lowest impedance to the electrical ground; other GND pins serve as heat sink/ground. These pins should be connected to large etch areas to help dissipate heat.

electrical characteristics, these specifications apply for T_A = –40°C to 85°C for the UCC2915 and 0°C to 70°C for the UCC3915, VIN = 12 V, IMAX = 0.4 V, $\overline{\text{SHTDWN}}$ = 2.4 V, $T_A = T_J$, (unless otherwise stated)

supply

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage input range		7.0		15.0	V
Supply current			1.0	2.0	mA
Sleep mode current	$\overline{\text{SHTDWN}}$ = 0.2 V, no load		100	150	µA
Output leakage	$\overline{\text{SHTDWN}}$ = 0.2 V			20	µA

NOTE 1: All voltages are with respect to GND. Current is positive into and negative out of the specified terminal.

output

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Voltage drop	I_{OUT} = 1 A (10 V to 12 V)		0.15	0.3	V
	I_{OUT} = 2 A (10 V to 12 V)		0.3	0.6	V
	I_{OUT} = 3 A (10 V to 12 V)		0.45	0.9	V
	I_{OUT} = 1 A, VIN = 7 V and 15 V		0.2	0.4	V
	I_{OUT} = 2 A, VIN = 7 V and 15 V		0.4	0.8	V
	I_{OUT} = 3 A, VIN = 7 V, 12 V MAX		0.6	1.2	V
Initial startup time	See Note 2		100		µs
Short circuit response	See Note 2		100		ns
Thermal shutdown	See Note 2		165		°C
Thermal hysteresis	See Note 2		10		°C

NOTE 1: All voltages are with respect to GND. Current is positive into and negative out of the specified terminal.
NOTE 2: Ensured by design. Not production tested.

DAC

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Trip current	Code = 0000–0011 (device off)				
	Code = 0100	0.07	0.25	0.45	A
	Code = 0101	0.32	0.50	0.70	A
	Code = 0110	0.50	0.75	0.98	A
	Code = 0111	0.75	1.00	1.3	A
	Code = 1000	1.0	1.25	1.6	A
	Code = 1001	1.25	1.50	1.85	A
	Code = 1010	1.5	1.75	2.15	A
	Code = 1011	1.70	2.00	2.4	A
	Code = 1100	1.90	2.25	2.7	A
	Code = 1101	2.1	2.50	2.95	A

NOTE 1: All voltages are with respect to GND. Current is positive into and negative out of the specified terminal.

electrical characteristics, these specifications apply for T_A = –40°C to 85°C for the UCC2915 and 0°C to 70°C for the UCC3915, VIN = 12 V, IMAX = 0.4 V, $\overline{SHTDWN}$ = 2.4 V, $T_A = T_J$, (unless otherwise stated)

DAC (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Trip current	Code = 1110	2.30	2.75	3.25	A
	Code = 1111	2.50	3.0	3.50	A
Max output current over trip (current source mode)	Code = 0100 to 1111, I_{MAX} = 0 V	0.35	1.0	1.65	A
Max output current (current source mode)	Code = 0100 to 1111, I_{MAX} = 2.4 V	3.0	4.0	5.2	A

NOTE 1: All voltages are with respect to GND. Current is positive into and negative out of the specified terminal.

fault timer

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
CT charge current	V_{CT} = 1.0 V	–83	–62	–47	µA
CT discharge current	V_{CT} = 1.0 V	0.8	1.2	1.8	µA
Output duty cycle	V_{OUT} = 0 V	1.0%	1.9%	3.3%	
CT fault threshold		1.2	1.5	1.7	V
CT reset threshold		0.4	0.5	0.6	V

NOTE 1: All voltages are with respect to GND. Current is positive into and negative out of the specified terminal.

shutdown

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Shutdown threshold		1.1	1.5	1.9	V
Shutdown hysteresis			150		mV
Input current			100	500	nA

NOTE 1: All voltages are with respect to GND. Current is positive into and negative out of the specified terminal.

open drain output ($\overline{FAULT}$)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
High level output current	$\overline{FAULT}$ = 5 V			250	µA
Low level output voltage	I_{OUT} = 5 mA		0.2	0.8	V

NOTE 1: All voltages are with respect to GND. Current is positive into and negative out of the specified terminal.

TTL input dc characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TTL input voltage high		2.0			V
TTL input voltage low				0.8	V
TTL input high current	V_{IH} = 2.4 V		3	10	µA
TTL input low current	V_{IL} = 0.4 V			1	µA

NOTE 1: All voltages are with respect to GND. Current is positive into and negative out of the specified terminal.

pin descriptions

B0 – B3: These pins provide digital input to the DAC, which sets the fault-current threshold. They can be used to provide a digital soft-start and adaptive-current limiting.

CT: A capacitor connected to ground sets the maximum-fault time. The maximum-fault time must be more than the time required to charge the external capacitance in one cycle. The maximum-fault time is defined as $T_{FAULT} = 16.1 \times 10^3 \times C_T$. Once the fault time is reached the output will shutdown for a time given by $T_{SD} = 833 \times 10^3 \times C_T$, this equates to a 1.9% duty cycle.

$\overline{\text{FAULT}}$: Open-drain output, which pulls low upon any fault or interrupt condition, or thermal shutdown.

IMAX: When this pin is set to a logic low, the maximum-sourcing current will always be 1 A above the programmed-fault level. When set to a logic high, the maximum-sourcing current will be a constant 4 A for applications which require fast charging of load capacitance.

$\overline{\text{SHTDWN}}$: When this pin is brought to a logic low, the IC is put into a sleep mode drawing typically less than 100 μA of I_{CC}.The input threshold is hysteretic, allowing the user to program a startup delay with an external RC circuit.

VIN: Input voltage to the UCC3915. The recommended voltage range is 7 V to 15 V. Both VIN pins should be connected together and connected to the power source.

VOUT: Output voltage from the UCC3915. Both VOUT pins should be connected together and connected to the load. When switched the output voltage will be approximately $V_{IN} – (0.15\ \Omega \times I_{OUT})$. VOUT must not exceed VIN by greater than 0.3 V.

APPLICATION INFORMATION

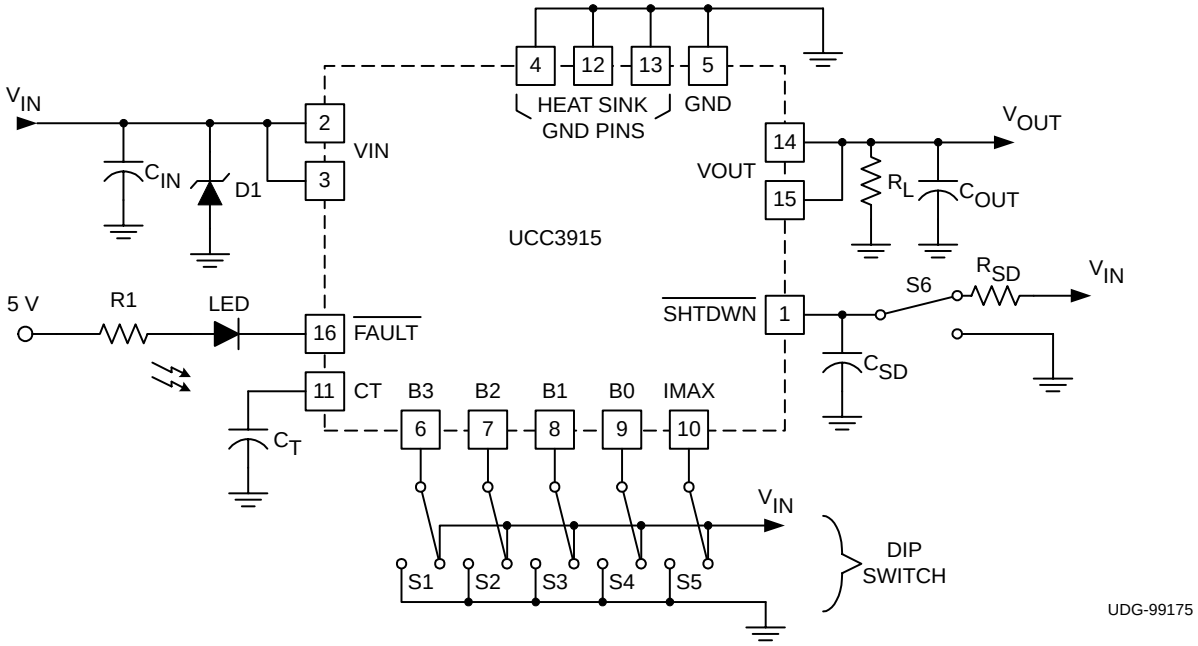


Figure 1. Evaluation Circuit

APPLICATION INFORMATION

protecting the UCC3915 from voltage transients

The parasitic inductance associated with the power distribution can cause a voltage spike at V_{IN} if the load current is suddenly interrupted by the UCC3915. It is important to limit the peak of this spike to less than 15 V to prevent damage to the UCC3915. This voltage spike can be minimized by:

- Reducing the power distribution inductance (e.g., twist the positive (+) and negative (–) leads of the power supply feeding V_{IN}, locate the power supply close to the UCC3915 or use PCB power and ground planes).
- Decoupling V_{IN} with a capacitor, C_{IN} (refer to Figure 1), located close to the V_{IN} pins. This capacitor is typically 1 μF or less to limit the inrush current.
- Clamping the voltage at V_{IN} below 15 V with a Zener diode, D1(refer to Figure 1), located close to the V_{IN} pins.

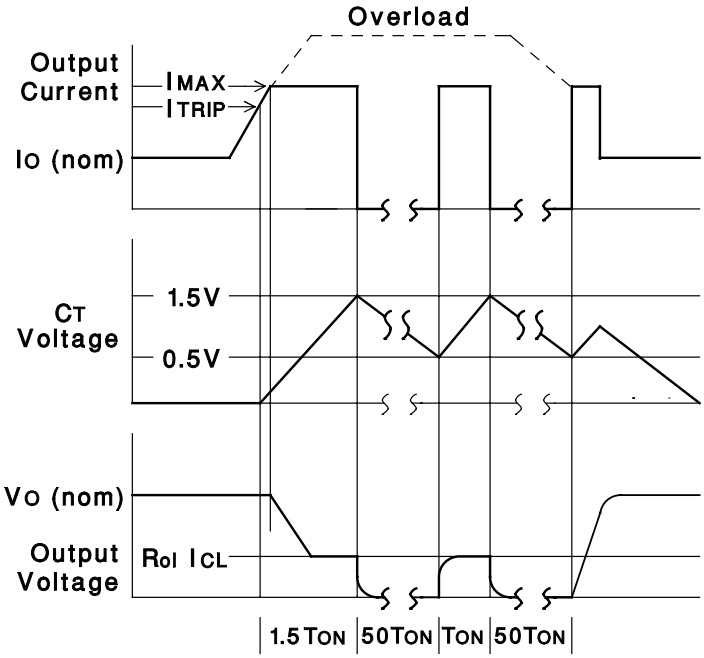


Figure 2. Load Current, Timing-Capacitor Voltage, and Output Voltage of the UCC3915 Under Fault Conditions

estimating maximum load capacitance

For hot-swap applications, the rate at which the total output capacitance can be charged depends on the maximum-output current available and the nature of the load. For a constant-current, current-limited application, the output will come up if the load asks for less than the maximum available short-circuit current.

To ensure recovery of a duty cycle from a short-circuited load condition, there is a maximum total output capacitance which can be charged for a given unit on time (fault time). The design value of on or fault time can be adjusted by changing the timing capacitor C_T.

APPLICATION INFORMATION

For worst-case constant-current load of value just less than the trip limit; $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left(I_{MAX} - I_{LOAD}\right) \times \left(\frac{16.1 \times 10^3 \times C_T}{V_{OUT}}\right)$$

Where V_{OUT} is the output voltage.

For a resistive load of value R_L, the value of $C_{OUT(max)}$ can be estimated from:

$$C_{OUT(max)} \approx \left(\frac{16.1 \times 10^3 \times C_T}{R_L \times \ell n\left[\frac{1}{1-\frac{V_{OUT}}{I_{MAX} \times R_L}}\right]}\right)$$

Long C_T times must consider the maximum temperature. Thermal shutdown protection may be the limiting fault time.

safety recommendations

Although the UCC3915 is designed to provide system protection for all fault conditions, all integrated circuits can ultimately fail short. For this reason, if the UCC3915 is intended for use in safety-critical applications where UL or some other safety rating is required, a redundant safety device such as a fuse should be placed in series with the device. The UCC3915 will prevent the fuse from blowing for virtually all fault conditions, increasing system reliability and reducing maintenance cost, in addition to providing the hot-swap benefits of the device.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2915DP	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2915DP	Samples
UCC2915DPG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2915DP	Samples
UCC3915DP	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3915DP	Samples
UCC3915DPG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3915DP	Samples
UCC3915DPTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3915DP	Samples
UCC3915PWP	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3915PWP	Samples
UCC3915PWPTR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3915PWP	Samples
UCC3915PWPTRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3915PWP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

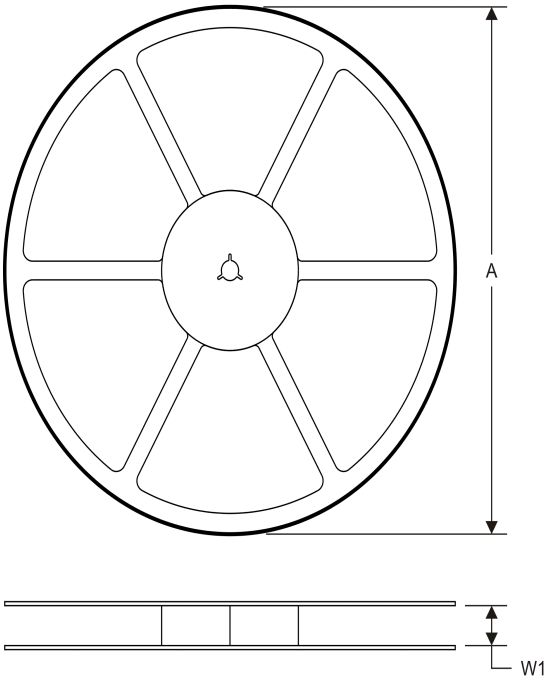
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

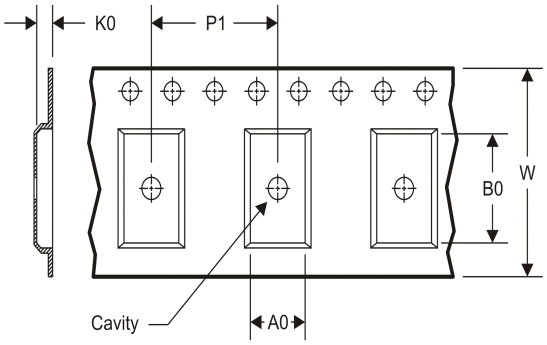
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



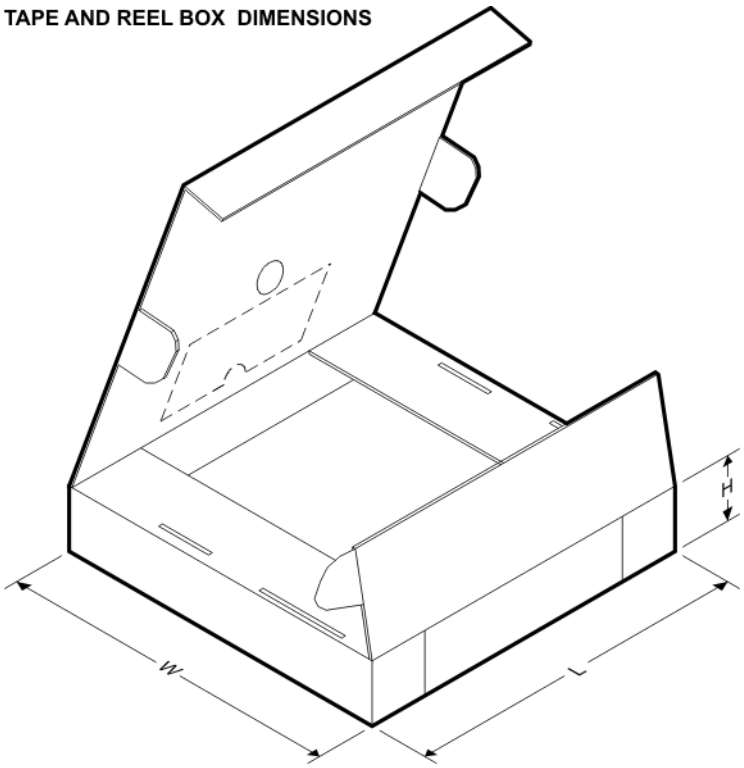
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC3915DPTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC3915PWPTR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

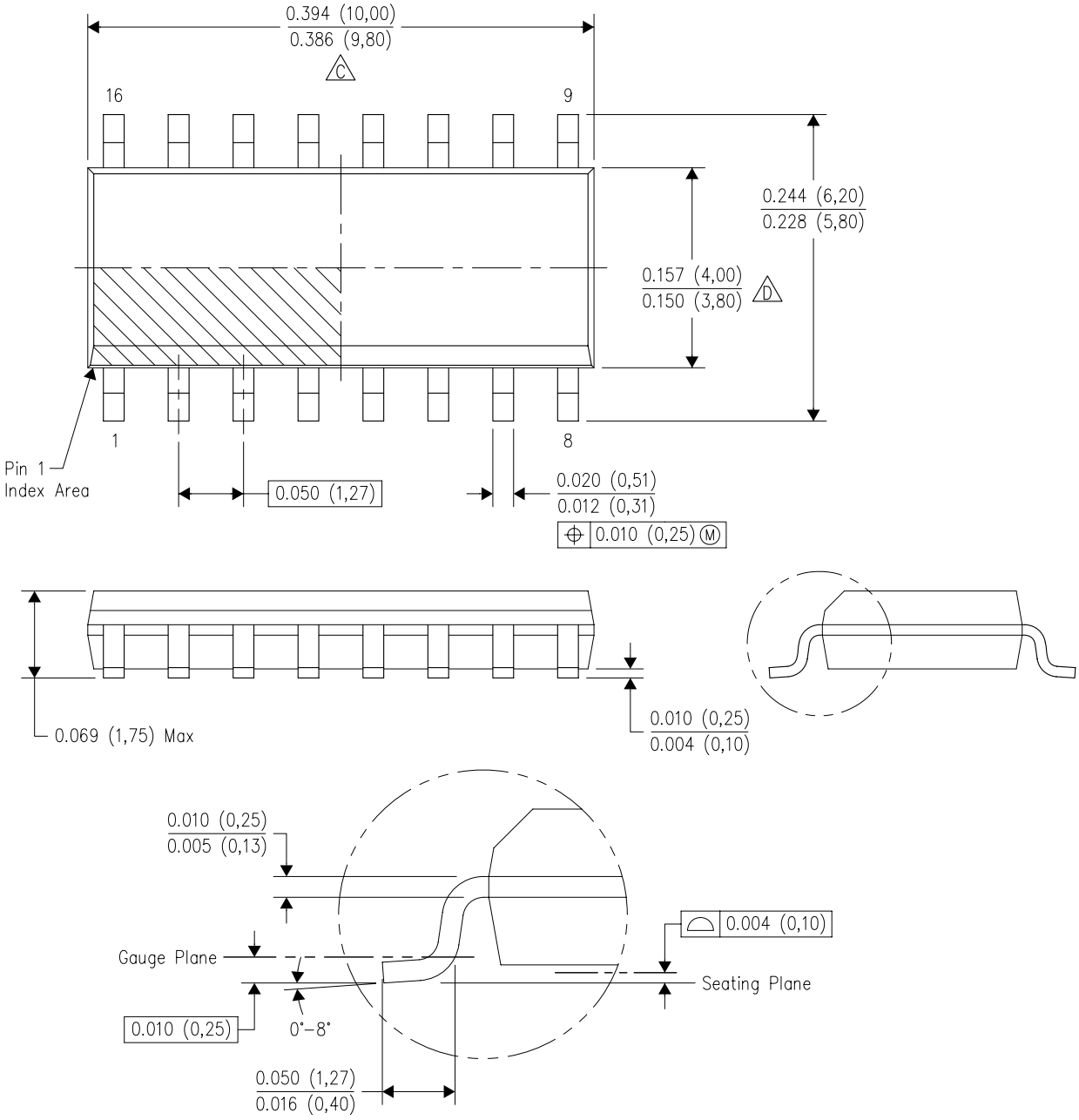
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC3915DPTR	SOIC	D	16	2500	367.0	367.0	38.0
UCC3915PWPTR	TSSOP	PW	24	2000	367.0	367.0	38.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

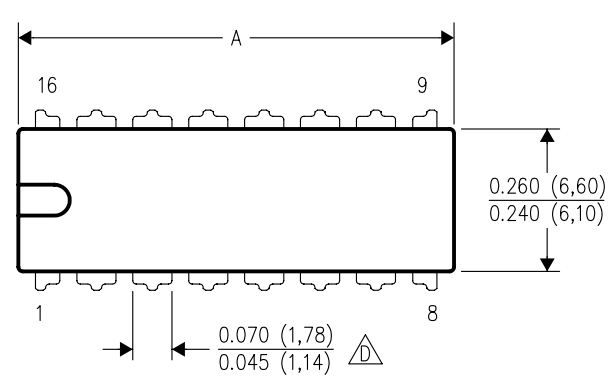


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

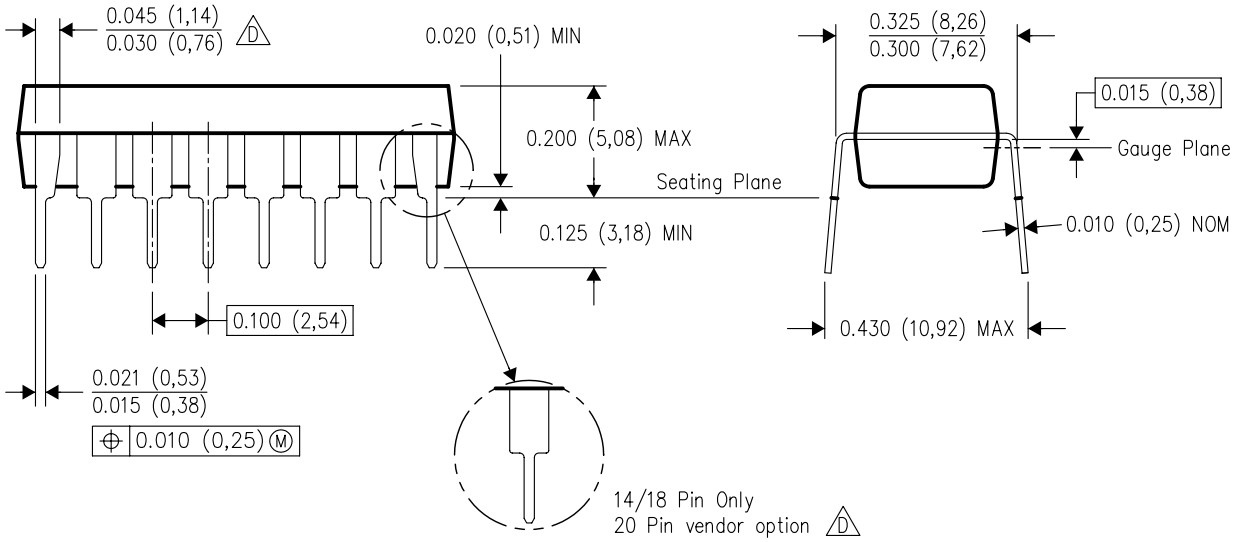
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



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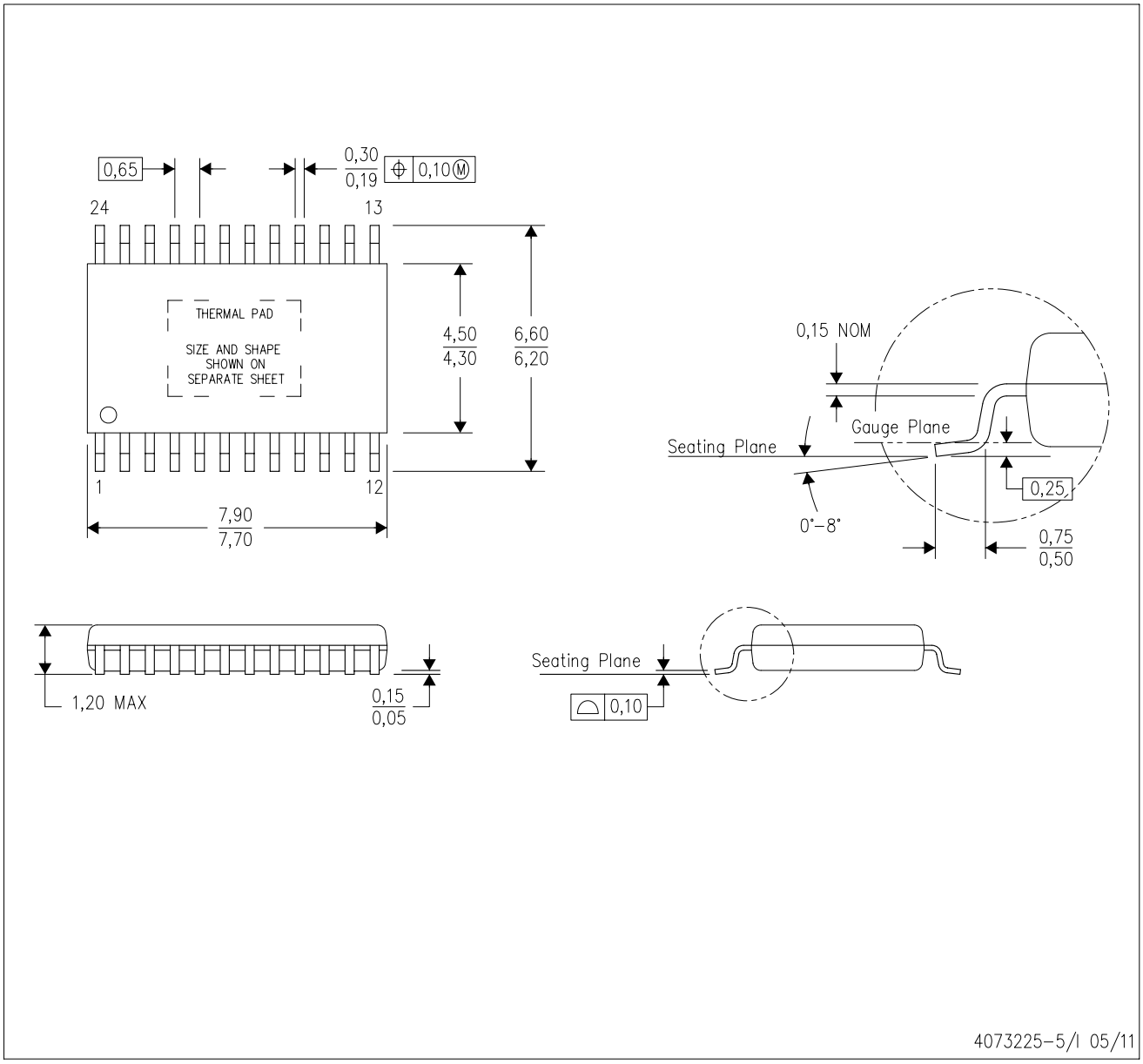
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PWP (R–PDSO–G24) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO–153

PowerPAD is a trademark of Texas Instruments.

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