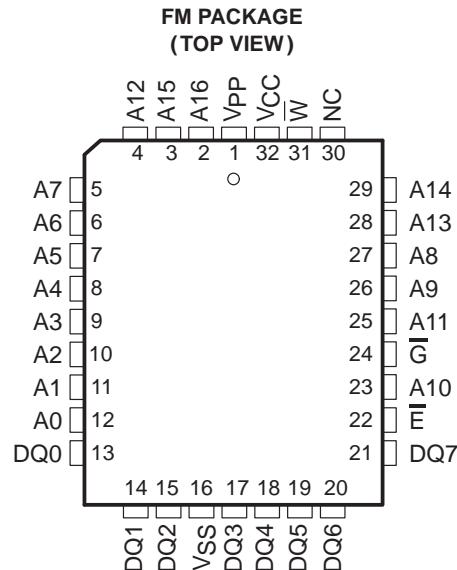


- Organization . . . 131072 by 8 Bits
- Pin Compatible With Existing 1-Megabit EPROMs
- V_{CC} Tolerance $\pm 10\%$
- All Inputs/Outputs TTL Compatible
- Maximum Access/Minimum Cycle Time
 - '28F010B-90 90 ns
 - '28F010B-10 100 ns
 - '28F010B-12 120 ns
 - '28F010B-15 150 ns
- Industry-Standard Programming Algorithm
- PEP4 Version Available With 168-Hour Burn-In, and Choice of Operating Temperature Ranges
- 100000 and 10000 Program/Erase-Cycle Versions Available
- Latchup Immunity of 250 mA on All Input and Output Lines
- Low Power Dissipation ($V_{CC} = 5.5$ V)
 - Active Write . . . 55 mW
 - Active Read . . . 165 mW
 - Electrical Erase . . . 82.5 mW
 - Standby . . . 0.55 mW
(CMOS-Input Levels)
- Automotive Temperature Range
 - -40°C to 125°C



PIN NOMENCLATURE	
A0–A16	Address Inputs
DQ0–DQ7	Inputs (programming)/Outputs
<u>E</u>	Chip Enable
G	Output Enable
NC	No Internal Connection
V _{CC}	5-V Power Supply
V _{PP}	12-V Power Supply†
<u>V_{SS}</u>	Ground
W	Write Enable

† Only in Program Mode

description

The TMS28F010B is a 131 072 by 8 bit (104 8576-bit), programmable read-only memory that can be electrically bulk-erased and reprogrammed. It is available in 100 000 and 10 000 program/erase-endurance-cycle versions.

The TMS28F010B Flash Memory is offered in a 32-lead plastic leaded chip-carrier package (shown above) using 1.25-mm (50-mil) lead spacing (FM suffix), a 32-lead thin small-outline package (DD suffix), and a reverse pinout TSOP package (DU suffix) both shown on the following page.



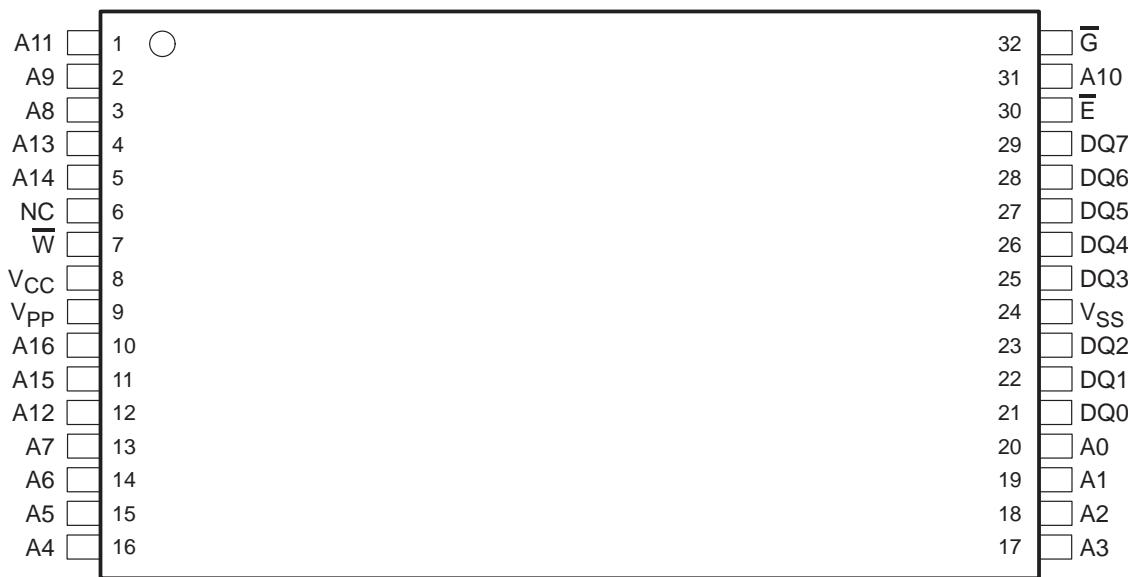
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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**DD PACKAGE
(TOP VIEW)**



**DU PACKAGE
REVERSE PINOUT
(TOP VIEW)**



device symbol nomenclature

TMS28F010B

-12

C5

FM

L

Temperature Range Designator

L = 0°C to 70°C
E = -40°C to 85°C
Q = -40°C to 125°C

Package Designator

FM = Plastic Leaded Chip Carrier
DD = Thin Small-Outline Package
DU = Thin Small-Outline Package,
Reverse Pinout

Program/Erase Endurance

C5 = 100000 Cycles
C4 = 10000 Cycles

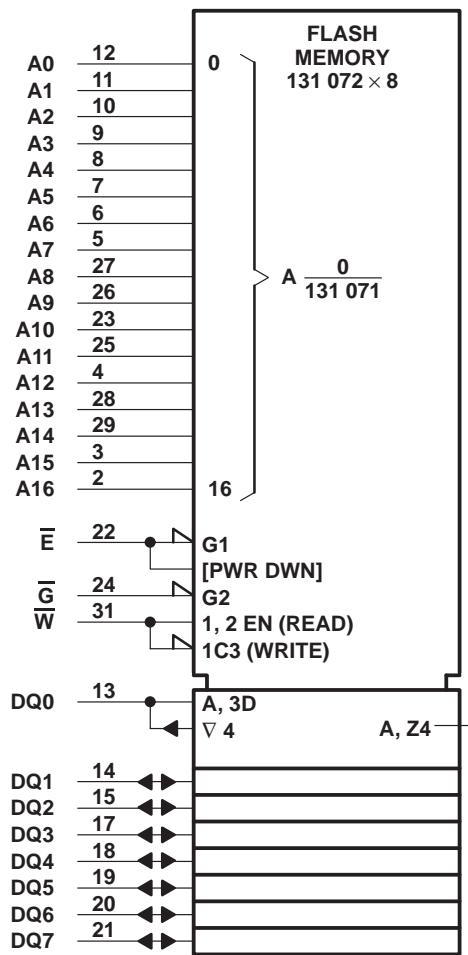
Speed Designator

-90 = 90 ns
-10 = 100 ns
-12 = 120 ns
-15 = 150 ns

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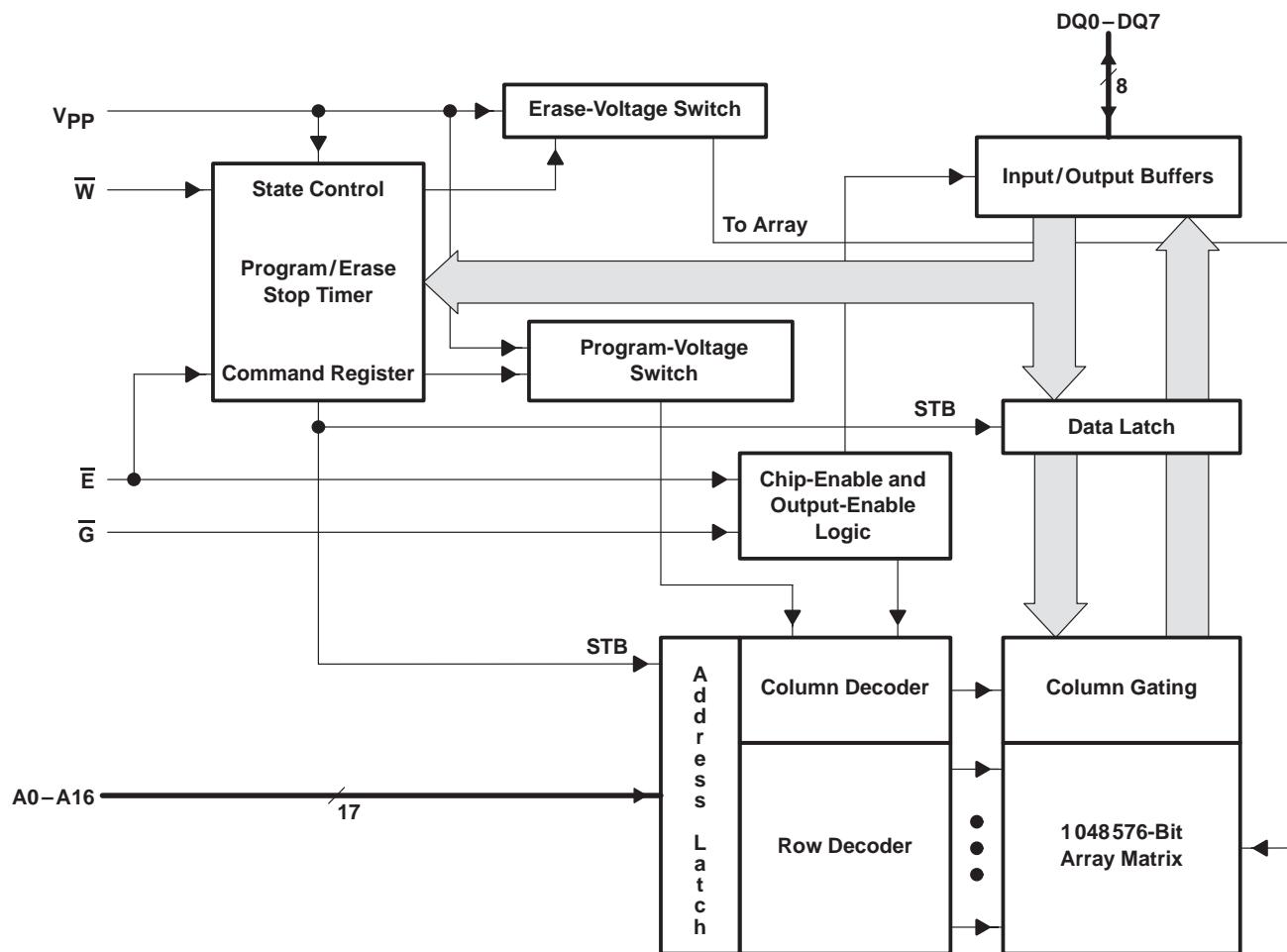
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for the FM package.

functional block diagram



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operation

Modes of operation are shown in Table 1.

Table 1. Operation Modes

MODE		FUNCTION [†]						
		V _{PP} [‡] (1)	Ē (22)	Ḡ (24)	A ₀ (12)	A ₉ (26)	W̄ (31)	DQ ₀ –DQ ₇ (13–15, 17–21)
Read	Read	V _{PPL}	V _{IL}	V _{IL}	X	X	V _{IH}	Data Out
	Output Disable	V _{PPL}	V _{IL}	V _{IH}	X	X	V _{IH}	Hi-Z
	Standby and Write Inhibit	V _{PPL}	V _{IH}	X	X	X	X	Hi-Z
	Algorithm-Selection Mode	V _{PPL}	V _{IL}	V _{IL}	V _{IL} V _{IH}	V _{ID}	V _{IH}	Mfr Equivalent Code 89h Device Equivalent Code B4h
Read/ Write	Read	V _{PPH}	V _{IL}	V _{IL}	X	X	V _{IH}	Data Out
	Output Disable	V _{PPH}	V _{IL}	V _{IH}	X	X	V _{IH}	Hi-Z
	Standby and Write Inhibit	V _{PPH}	V _{IH}	X	X	X	X	Hi-Z
	Write	V _{PPH}	V _{IL}	V _{IH}	X	X	V _{IL}	Data In

[†]X can be V_{IL} or V_{IH}.

[‡]V_{PPL} ≤ V_{CC} + 2 V; V_{PPH} is the programming voltage specified for the device. For more details, refer to the recommended operating conditions.

read/output disable

When the outputs of two or more TMS28F010Bs are connected in parallel on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of other devices. To read the output of the TMS28F010B, a low-level signal is applied to the Ē and Ḡ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins.

standby and write inhibit

Active I_{CC} current can be reduced from 30 mA to 1 mA by applying a high TTL level on Ē or to 100 μA with a high CMOS level on Ē. In this mode, all outputs are in the high-impedance state. The TMS28F010B draws active current when it is deselected during programming, erasure, or program/erase verification. It continues to draw active current until the operation is terminated.

algorithm-selection mode

The algorithm-selection mode provides access to a binary code identifying the correct programming and erase algorithms. This mode is activated when A₉ (pin 26) is forced to V_{ID}. Two identifier bytes are accessed by toggling A₀. All other addresses must be held low. A₀ low selects the manufacturer equivalent code 89h, and A₀ high selects the device equivalent code B4h, as shown in Table 2.

Table 2. Algorithm-Selection Modes

IDENTIFIER [§]	PINS									
	A ₀	DQ ₇	DQ ₆	DQ ₅	DQ ₄	DQ ₃	DQ ₂	DQ ₁	DQ ₀	HEX
Manufacturer Equivalent Code	V _{IL}	1	0	0	0	1	0	0	1	89
Device Equivalent Code	V _{IH}	1	0	1	1	0	1	0	0	B4

[§]Ē = Ḡ = V_{IL}, A₁–A₈ = V_{IL}, A₉ = V_{ID}, A₁₀–A₁₆ = V_{IL}, V_{PP} = V_{PPL}.

programming and erasure

In the erased state, all bits are at a logic 1. Before erasing the device, all memory bits must be programmed to a logic 0. Afterwards, the entire chip is erased. At this point, the bits, now logic 1s, can be programmed accordingly. Refer to the Fastwrite and Fasterase algorithms for further detail.



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command register

The command register controls the program and erase functions of the TMS28F010B. The algorithm-selection mode can be activated using the command register in addition to the previously described method. When V_{PP} is high, the contents of the command register and the function being performed can be changed. The command register is written to when \bar{E} is low and \bar{W} is pulsed low. The address is latched on the leading edge of the pulse, while the data is latched on the trailing edge. Accidental programming or erasure is minimized because two commands must be executed to invoke either operation. The command register is inhibited when V_{CC} is below the erase/write lockout voltage, V_{LKO} .

power supply considerations

Each device should have a $0.1\text{-}\mu\text{F}$ ceramic capacitor connected between V_{CC} and V_{SS} to suppress circuit noise. Changes in current drain on V_{PP} require it to have a bypass capacitor as well. Printed-circuit traces for both power supplies should be appropriate to handle the current demand.

command definitions

See Table 3 for command definitions.

Table 3. Command Definitions

COMMAND	REQUIRED BUS CYCLES	FIRST BUS CYCLE			SECOND BUS CYCLE		
		OPERATION†	ADDRESS	DATA	OPERATION	ADDRESS	DATA
Read	1	Write	X	00h	Read	RA	RD
Algorithm-Selection Mode	3	Write	X	90h	Read	0000 0001	89h B4h
Set-Up-Erase/Erase	2	Write	X	20h	Write	X	20h
Erase Verify	2	Write	EA	A0h	Read	X	EVD
Set-Up-Program/Program	2	Write	X	40h	Write	PA	PD
Program Verify	2	Write	X	C0h	Read	X	PVD
Reset	2	Write	X	FFh	Write	X	FFh

† Modes of operation are defined in Table 1.

Legend:

- EA Address of memory location to be read during erase verify
- RA Address of memory location to be read
- PA Address of memory location to be programmed. Address is latched on the falling edge of \bar{W}
- RD Data read from location RA during the read operation
- EVD Data read from location EA during erase verify
- PD Data to be programmed at location PA. Data is latched on the rising edge of \bar{W}
- PVD Data read from location PA during program verify

read command

Memory contents can be accessed while V_{PP} is high or low. When V_{PP} is high, writing 00h into the command register invokes the read operation. When the device is powered up, the default contents of the command register are 00h and the read operation is enabled. The read operation remains enabled until a different valid command is written to the command register.

algorithm-selection mode command

The algorithm-selection mode is activated by writing 90h into the command register. The manufacturer-equivalent code (89h) is identified by the value read from address location 0000h, and the device-equivalent code (B4h) is identified by the value read from address location 0001h.

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command definitions (continued)

set-up-erase/erase commands

The erase-algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the erase mode, write the set-up-erase command, 20h, into the command register. After the TMS28F010B is in the erase mode, writing a second erase command, 20h, into the command register invokes the erase operation. The erase operation begins on the rising edge of \overline{W} and ends on the rising edge of the next \overline{W} . The erase operation requires at least 9.5 ms to complete before the erase-verify command, A0h, can be loaded.

Maximum erase timing is controlled by the internal stop timer. When the stop timer terminates the erase operation, the device enters an inactive state and remains inactive until a command is received.

program-verify command

The TMS28F010B can be programmed sequentially or randomly because it is programmed one byte at a time. Each byte must be verified after it is programmed. The program-verify operation prepares the device to verify the most recently programmed byte. To invoke the program-verify operation, C0h must be written into the command register. The program-verify operation ends on the rising edge of \overline{W} .

While verifying a byte, the TMS28F010B applies an internal margin voltage to the designated byte. If the true data and programmed data match, programming continues to the next designated byte location; otherwise, the byte must be reprogrammed. Figure 1 shows how commands and bus operations are combined for byte programming.

erase-verify command

All bytes must be verified following an erase operation. After the erase operation is complete, an erased byte can be verified by writing the erase-verify command, A0h, into the command register. This command causes the device to exit the erase mode on the rising edge of \overline{W} . The address of the byte to be verified is latched on the falling edge of \overline{W} . The erase-verify operation remains enabled until a command is written to the command register.

To determine whether or not all the bytes have been erased, the TMS28F010B applies a margin voltage to each byte. If FFh is read from the byte, all bits in the designated byte have been erased. The erase-verify operation continues until all of the bytes have been verified. If FFh is not read from a byte, an additional erase operation needs to be executed. Figure 2 shows the combination of commands and bus operations for electrically erasing the TMS28F010B.

set-up-program/program commands

The programming algorithm initiates with $\overline{E} = V_{IL}$, $\overline{W} = V_{IL}$, $\overline{G} = V_{IH}$, $V_{PP} = V_{PPH}$, and $V_{CC} = 5$ V. To enter the programming mode, write the set-up-program command, 40h, into the command register. The programming operation is invoked by the next write-enable pulse. Addresses are latched internally on the falling edge of \overline{W} , and data is latched internally on the rising edge of \overline{W} . The programming operation begins on the rising edge of \overline{W} and ends on the rising edge of the next \overline{W} pulse. The program operation requires 10 μ s for completion before the program-verify command, C0h, can be loaded.

Maximum program timing is controlled by the internal stop timer. When the stop timer terminates the program operation, the device enters an inactive state and remains inactive until a command is received.

reset command

To reset the TMS28F010B after set-up-erase command or set-up-program command operations without changing the contents in memory, write FFh into the command register two consecutive times. After executing the reset command, the device defaults to the read mode.



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Fastwrite algorithm

The TMS28F010B is programmed using the Texas Instruments Fastwrite algorithm shown in Figure 1. This algorithm programs in a nominal time of two seconds.

Fasterase algorithm

The TMS28F010B is erased using the Texas Instruments Fasterase algorithm shown in Figure 2. The memory array needs to be completely programmed (using the Fastwrite algorithm) before erasure begins. Erasure typically occurs in one second.

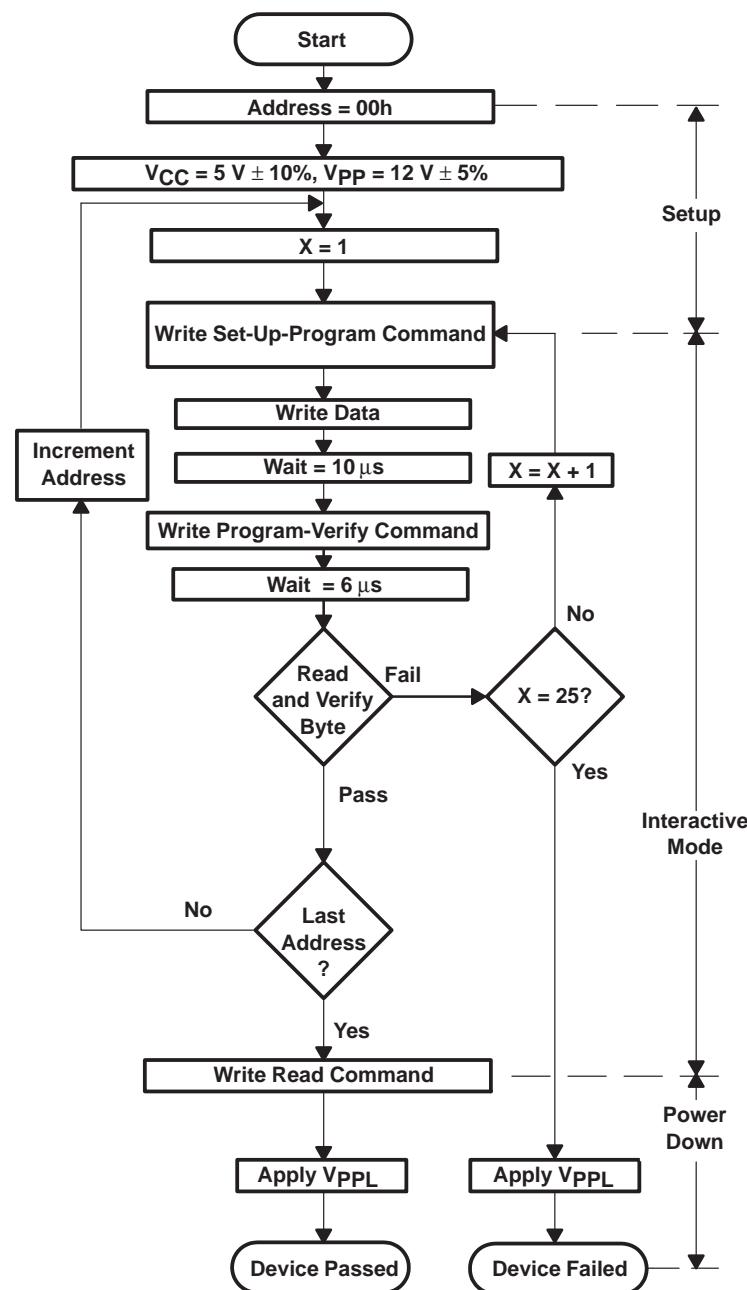
parallel erasure

To reduce total erase time, several devices can be erased in parallel. Since each Flash Memory can erase at a different rate, every device must be verified separately after each erase pulse. After a given device has been successfully erased, the erase command should not be issued to this device again. All devices that complete erasure should be masked until the parallel erasure process is finished (see Figure 3).

Examples of how to mask a device during parallel erase include driving the \bar{E} pin high, writing the read command (00h) to the device when the others receive a set-up-erase or erase command, or disconnecting it from all electrical signals with relays or other types of switches.

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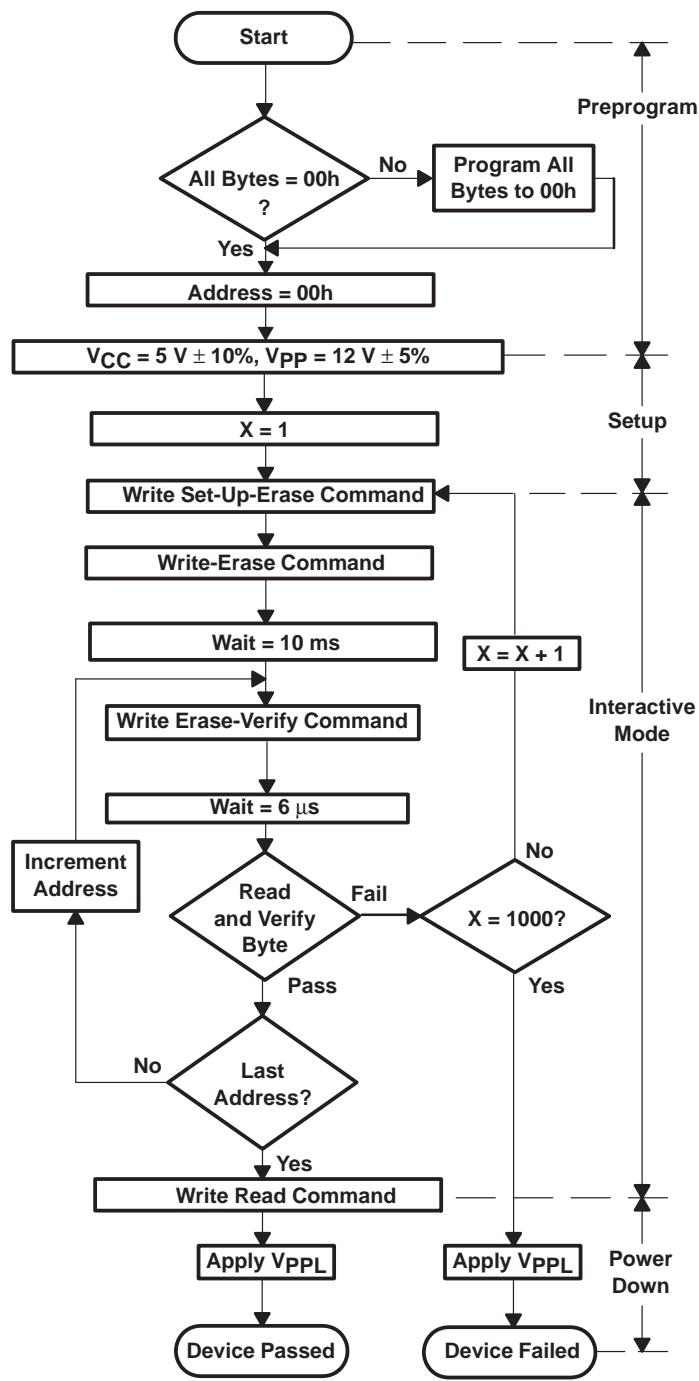
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Bus Operation	Command	Comments
<i>Initialize Address</i>		
<i>Standby</i>		Wait for VPP to ramp to VPPH (see Note A) Initialize pulse count
<i>Write</i>	Set-Up-Program Write	Data = 40h
<i>Write</i>	Write Data	Valid address/data
<i>Standby</i>		Wait = 10 µs
<i>Write</i>	Program-Verify	Data = C0h; ends Program operation
<i>Standby</i>		Wait = 6 µs
<i>Read</i>		Read byte to verify Programming; compare output to expected output
—	—	—
<i>Write</i>	Read	Data = 00h; resets register for read operations
<i>Standby</i>		Wait for VPP to ramp to VPPD (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of VPPH.
B. Refer to the recommended operating conditions for the value of VPPD.

Figure 1. Programming Flowchart: Fastwrite Algorithm



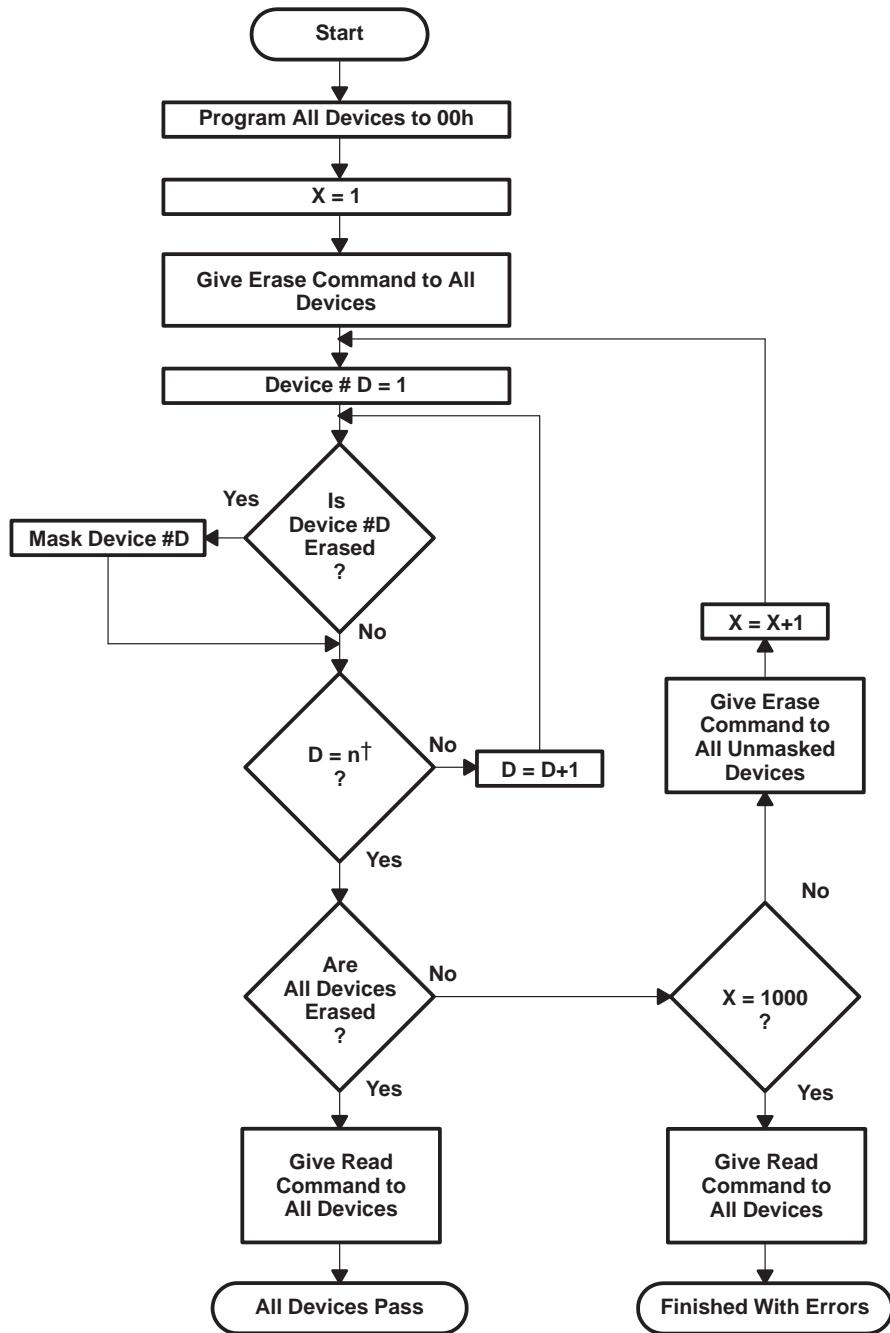
Bus Operation	Command	Comments
		Entire memory must = 00h before erasure
		Use Fastwrite programming algorithm
		Initialize addresses
<i>Standby</i>		Wait for Vpp to ramp to V _{PPH} (see Note A)
		Initialize pulse count
<i>Write</i>	Set-Up-Erase	Data = 20h
<i>Write</i>	Erase	Data = 20h
<i>Standby</i>		Wait = 10 ms
<i>Write</i>	Erase Verify	Addr = Byte to verify; Data = A0h; ends the erase operation
<i>Standby</i>		Wait = 6 µs
<i>Read</i>		Read byte to verify erasure; compare output to FFh
<i>Write</i>	Read	Data = 00h; resets register for read operations
<i>Standby</i>		Wait for Vpp to ramp to V _{PPL} (see Note B)

NOTES: A. Refer to the recommended operating conditions for the value of V_{PPH}.
B. Refer to the recommended operating conditions for the value of V_{PPL}.

Figure 2. Flash-Erase Flowchart: Fasterase Algorithm

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† n = number of devices being erased.

Figure 3. Parallel-Erase Flow Diagram

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to V_{SS} .

1. All voltage values are with respect to V_{SS} .
2. The voltage on any input pin can undershoot to -2 V for periods less than 20 ns .
3. The voltage on any output pin can overshoot to 7 V for periods less than 20 ns .

recommended operating conditions

			MIN	TYP	MAX	UNIT
V _{CC}	Supply voltage	During write/read/flash erase	4.5	5	5.5	V
V _{PP}	Supply voltage	During read only (V _{PPL})	0		V _{CC} + 2	V
		During write/read/flash erase (V _{PPH})	11.4	12	12.6	V
V _{IH}	High-level dc input voltage		TTL	2	V _{CC} + 0.5	V
			CMOS	V _{CC} - 0.5	V _{CC} + 0.5	
V _{IL}	Low-level dc input voltage		TTL	-0.5	0.8	V
			CMOS	GND - 0.2	GND + 0.2	
V _{ID}	Voltage level on A9 for algorithm-selection mode			11.5	13	V

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -2.5 mA	2.4	V _{CC} – 0.4	V
		I _{OH} = -100 µA			
V _{OL}	Low-level output voltage	I _{OL} = 5.8 mA	0.45	0.1	V
		I _{OL} = 100 µA			
I _{ID}	A9 algorithm-selection-mode current	A9 = V _{ID} max	200		µA
I _I	All except A9	V _I = 0 V to 5.5 V	±1	±200	µA
	A9	V _I = 0 V to 13 V			
I _O	Output current (leakage)	V _O = 0 V to V _{CC}	±10		µA
I _{PP1}	V _{PP} supply current (read/standby)	V _{PP} = V _{PPH} , Read mode	200		µA
		V _{PP} = V _{PPL}	±10		µA
I _{PP2}	V _{PP} supply current (during program pulse)	V _{PP} = V _{PPH}	30		mA
I _{PP3}	V _{PP} supply current (during flash erase)	V _{PP} = V _{PPH}	30		mA
I _{PP4}	V _{PP} supply current (during program/erase-verify) (see Note 4)	V _{PP} = V _{PPH}	5.0		mA
I _{CCS}	V _{CC} supply current (standby)	V _{CC} = 5.5 V, \bar{E} = V _{IH}	1		mA
		V _{CC} = 5.5 V, \bar{E} = V _{CC}	100		µA
I _{CC1}	V _{CC} supply current (active read)	V _{CC} = 5.5 V, \bar{E} = V _{IL} , f = 6 MHz, I _{OUT} = 0 mA	30		mA
I _{CC2}	V _{CC} average supply current (active write) (see Note 4)	V _{CC} = 5.5 V, \bar{E} = V _{IL} , Programming in progress	10		mA
I _{CC3}	V _{CC} average supply current (flash erase) (see Note 4)	V _{CC} = 5.5 V, \bar{E} = V _{IL} , Erasure in progress	15		mA
I _{CC4}	V _{CC} average supply current (program/erase-verify) (see Note 4)	V _{CC} = 5.5 V, \bar{E} = V _{IL} , V _{PP} = V _{PPH} , Program/erase-verify in progress	15		mA
V _{LKO}	V _{CC} erase/write-lockout voltage	V _{PP} = V _{PPH}	2.5		V

NOTE 4: Characterization data available.

**capacitance over recommended ranges of supply voltage and operating free-air temperature,
f = 1 MHz†**

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
C _i	Input capacitance	V _I = 0 V, f = 1 MHz	6		pF
C _o	Output capacitance	V _O = 0 V, f = 1 MHz	12		pF

† Capacitance measurements are made on sample basis only.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature

PARAMETER	TEST CONDITIONS	ALTERNATE SYMBOL	'28F010B-90		'28F010B-10		'28F010B-12		'28F010B-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	$C_L = 100 \text{ pF}$, 1 Series 74 TTL load, Input $t_f \leq 20 \text{ ns}$, Input $t_f \leq 20 \text{ ns}$	t_{AVQV}	90		100		120		150		ns
$t_{a(E)}$		t_{ELQV}	90		100		120		150		ns
$t_{en(G)}$		t_{GLQV}	35		45		50		55		ns
$t_{c(R)}$		t_{AVAV}	90		100		120		150		ns
$t_{d(E)}$		t_{ELQX}	0		0		0		0		ns
$t_{d(G)}$		t_{GLQX}	0		0		0		0		ns
$t_{dis(E)}$		t_{EHQZ}	0	45	0	55	0	55	0	55	ns
$t_{dis(G)}$		t_{GHQZ}	0	30	0	30	0	30	0	35	ns
$t_{h(D)}$		t_{AXQX}	0		0		0		0		ns
$t_{rec(W)}$		t_{WHGL}	6		6		6		6		μs

† Whichever occurs first

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timing requirements—write/erase/program operations

PARAMETER	ALTERNATE SYMBOL	'28F010B-90			'28F010B-10			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(W)}$	t_{AVAV}	90			100			ns
$t_{c(W)PR}$	t_{WHWH1}	10			10			μ s
$t_{c(W)ER}$	t_{WHWH2}	9.5			9.5	10		ms
$t_h(A)$	t_{WLAX}	40			55			ns
$t_h(E)$	t_{WHEH}	0			0			ns
$t_h(WHD)$	t_{WHDX}	10			10			ns
$t_{su(A)}$	t_{AVWL}	0			0			ns
$t_{su(D)}$	t_{DVWH}	40			50			ns
$t_{su(E)}$	t_{ELWL}	15			20			ns
$t_{su(VPPEL)}$	t_{VPEL}	1			1			μ s
$t_{rec(W)}$	t_{WHGL}	6			6			μ s
$t_{rec(R)}$	t_{GHWL}	0			0			μ s
$t_w(W)$	t_{WLWH}	40			60			ns
$t_w(WH)$	t_{WHWL}	20			20			ns
$t_r(VPP)$	t_{VPPR}	1			1			μ s
$t_f(VPP)$	t_{VPPF}	1			1			μ s

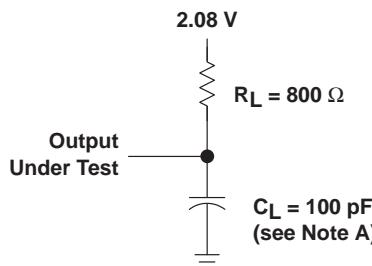
PARAMETER	ALTERNATE SYMBOL	'28F010B-12			'28F010B-15			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$t_{c(W)}$	t_{AVAV}	120			150			ns
$t_{c(W)PR}$	t_{WHWH1}	10			10			μ s
$t_{c(W)ER}$	t_{WHWH2}	9.5	10		9.5	10		ms
$t_h(A)$	t_{WLAX}	60			60			ns
$t_h(E)$	t_{WHEH}	0			0			ns
$t_h(WHD)$	t_{WHDX}	10			10			ns
$t_{su(A)}$	t_{AVWL}	0			0			ns
$t_{su(D)}$	t_{DVWH}	50			50			ns
$t_{su(E)}$	t_{ELWL}	20			20			ns
$t_{su(VPPEL)}$	t_{VPEL}	1			1			μ s
$t_{rec(W)}$	t_{WHGL}	6			6			μ s
$t_{rec(R)}$	t_{GHWL}	0			0			μ s
$t_w(W)$	t_{WLWH}	60			60			ns
$t_w(WH)$	t_{WHWL}	20			20			ns
$t_r(VPP)$	t_{VPPR}	1			1			μ s
$t_f(VPP)$	t_{VPPF}	1			1			μ s

NOTE 5: Rise/fall time \leq 10 ns

timing requirements — alternative \bar{E} -controlled writes

PARAMETER	ALTERNATE SYMBOL	'28F010B-90		'28F010B-10		'28F010B-12		'28F010B-15		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(W)}$	Cycle time, write using \bar{E}	tAVAV	90	100		120		150		ns
$t_{c(E)PR}$	Cycle time, programming operation	tEHEH	10	10		10		10		μ s
$t_h(EA)$	Hold time, address	tELAX	45	75		80		80		ns
$t_h(ED)$	Hold time, data	tEHDX	10	10		10		10		ns
$t_h(W)$	Hold time, \bar{W}	tEHW	0	0		0		0		ns
$t_{su(A)}$	Setup time, address	tAVEL	0	0		0		0		ns
$t_{su(D)}$	Setup time, data	tDVEH	35	50		50		50		ns
$t_{su(W)}$	Setup time, \bar{W} before \bar{E}	tWEL	0	0		0		0		ns
$t_{su(VPPEL)}$	Setup time, V _{PP} to \bar{E} low	tVPEL	1	1		1		1		μ s
$t_{rec(E)R}$	Recovery time, write using \bar{E} before read	tEHGL	6	6		6		6		μ s
$t_{rec(E)W}$	Recovery time, read before write using \bar{E}	tGHEL	0	0		0		0		μ s
$t_w(E)$	Pulse duration, write using \bar{E}	tELEH	45	70		70		70		ns
$t_w(EH)$	Pulse duration, write, \bar{E} high	tEHEL	20	20		20		20		ns

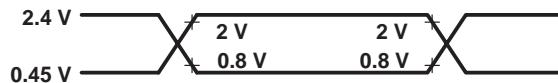
PARAMETER MEASUREMENT INFORMATION



NOTE A: C_L includes probe and fixture capacitance.

Figure 4. AC Test Output Load Circuit

AC testing input/output waveforms



AC testing inputs are driven at 2.4 V for logic high and 0.45 V for logic low. Timing measurements are made at 2 V for logic high and 0.8 V for logic low on both inputs and outputs. Each device should have a 0.1- μ F ceramic capacitor connected between V_{CC} and V_{SS} as close as possible to the device pins.

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PARAMETER MEASUREMENT INFORMATION

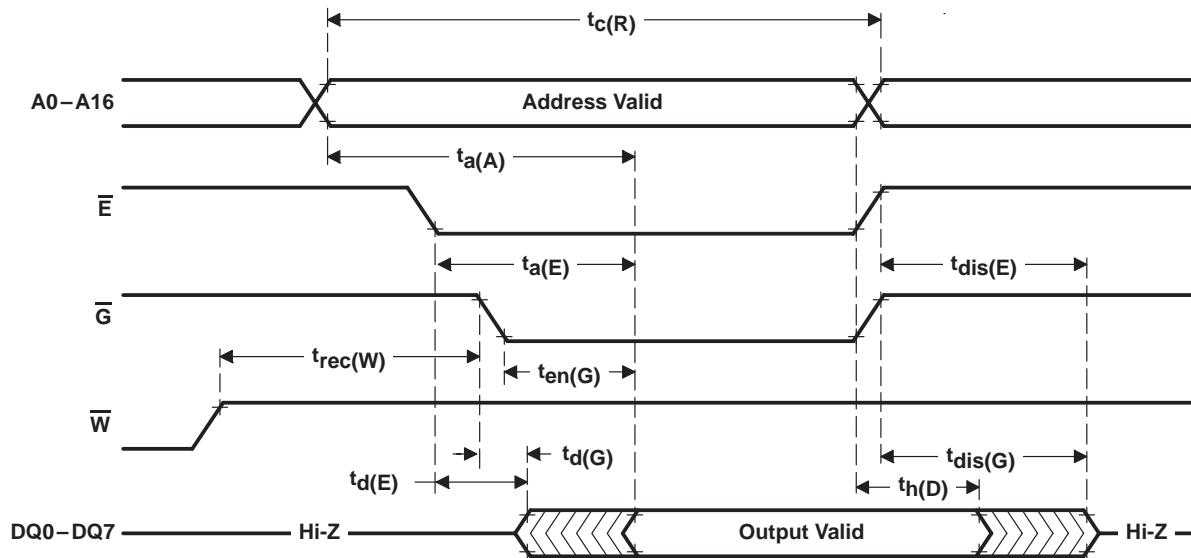


Figure 5. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

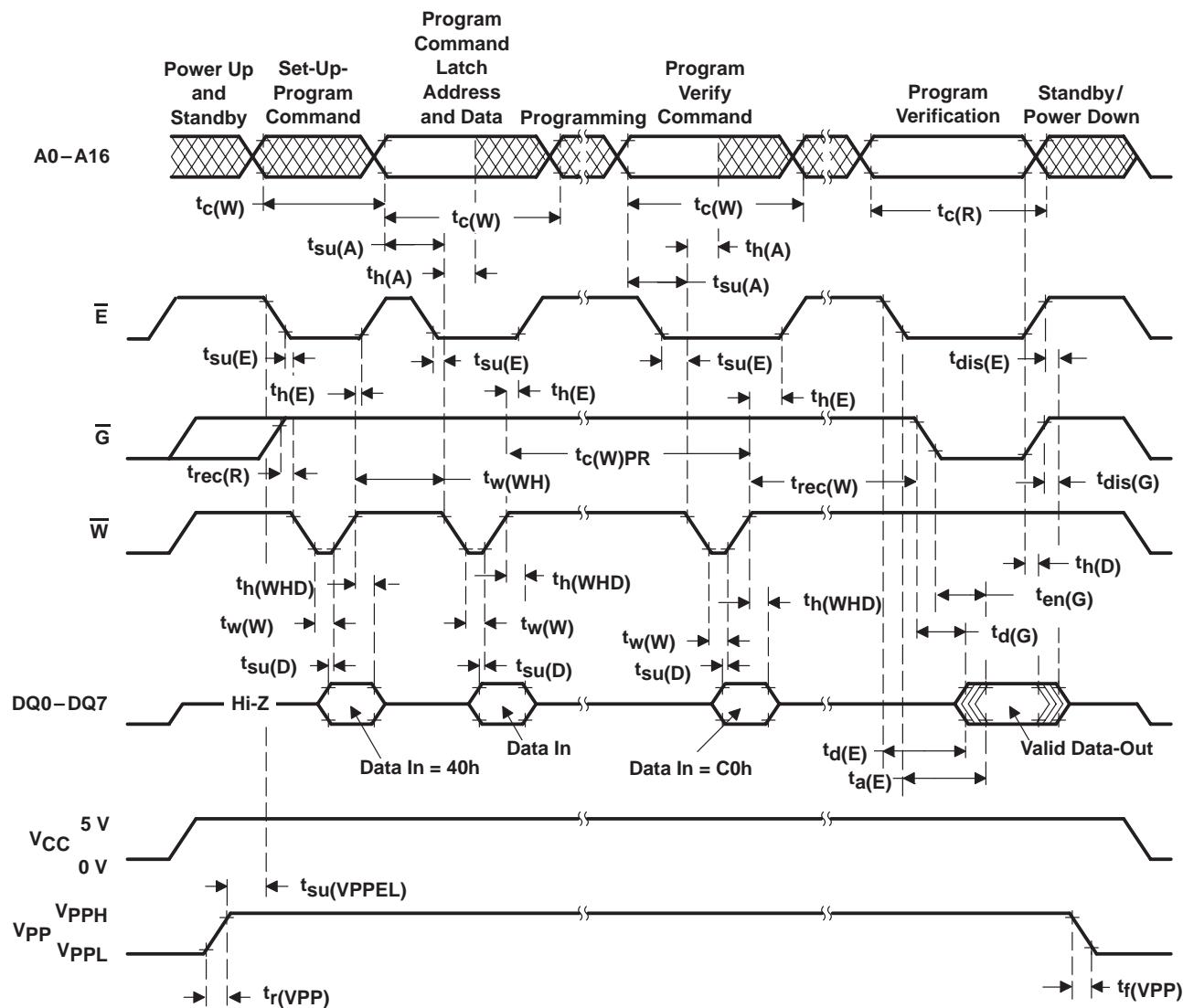


Figure 6. Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

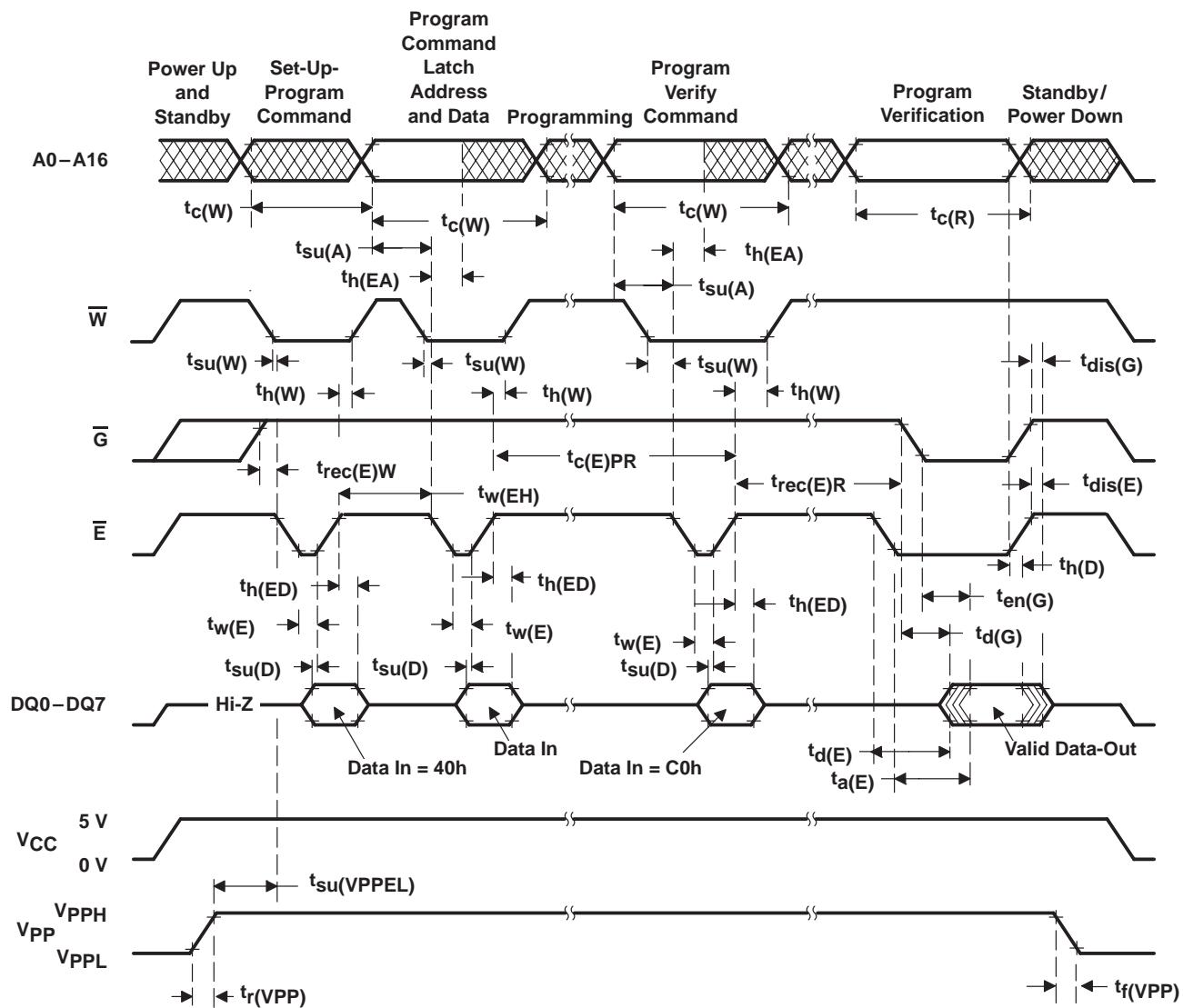


Figure 7. Write-Cycle (Alternative \overline{E} -Controlled Writes) Timing

PARAMETER MEASUREMENT INFORMATION

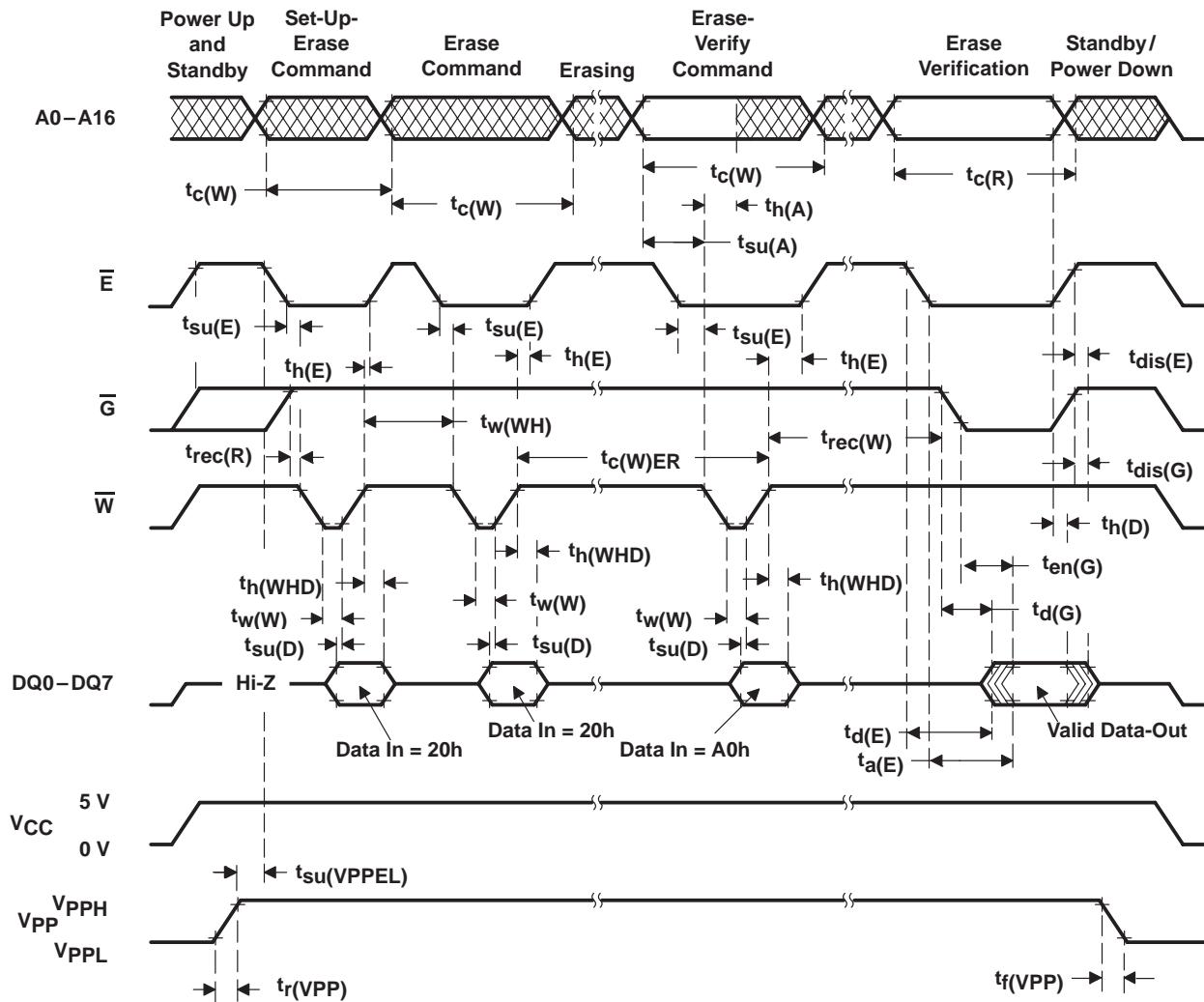


Figure 8. Flash-Erase-Cycle Timing

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