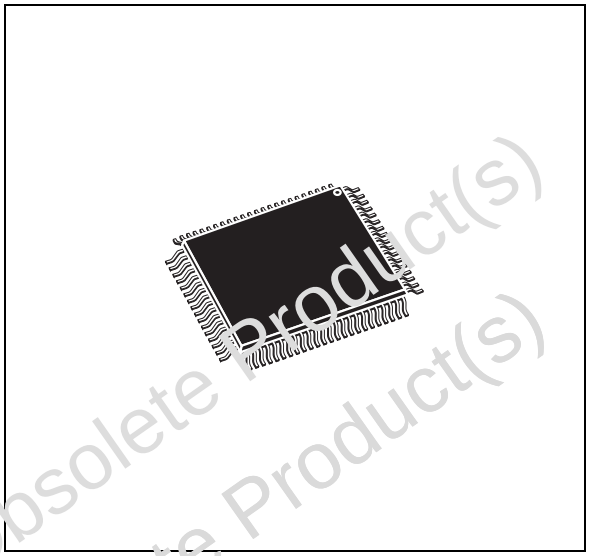
PSD4135G2
PSD4135G2V

Flash in-system programmable peripherals for 16-bit MCUs

Features

- Single supply volate
  - 3 V±10% (PSD4135G2V)
  - 5 V±10% (PSD4135G2)
- Up to 4 Mbit of primary Flash memory (8 uniform sectors)
- 256 Kbit secondary Flash memory (4 uniform sectors)
- Up to 64 Kbit SRAM
- Over 3,000 gates of PLD: DPLD and CPLD
- 52 reconfigurable I/O ports
- Enhanced JTAG serial port
- Programmable power management
- High endurance:
  - 100,000 erase/write cycles of Flash memory
  - 1,000 erase/write cycles of PLD



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1 Description

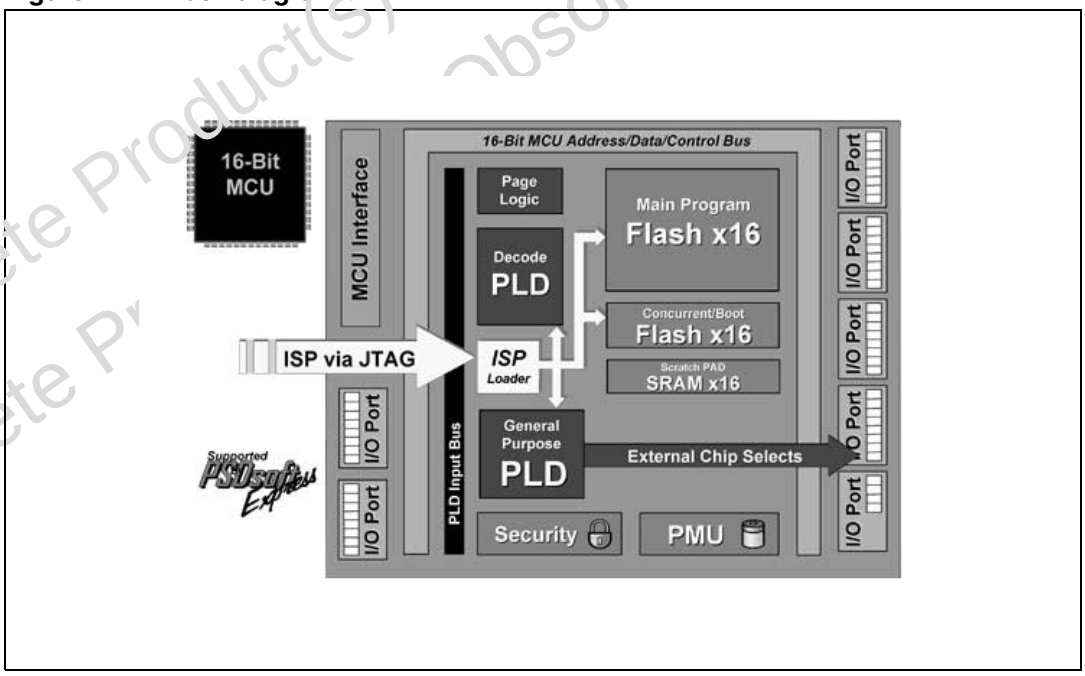
The PSD4135G2 and PSD4135G2V programmable microcontroller (MCU) peripherals bring in-system-programmability (ISP) to Flash memory and programmable logic. The result is a simple and flexible solution for embedded designs. The devices combine many of the peripheral functions found in MCU based applications (see *Figure 1*). They consist of six major types of functional blocks:

- Memory blocks
  - 4 Mbit of Flash memory
  - A secondary Flash memory for boot or data
  - Over 3,000 gates of Flash programmable logic
  - 64 Kbit SRAM
- PLD blocks
- Bus interface
- Reconfigurable I/O ports
- Power management unit
- JTAG-ISP interface

The functions of each block are described in the following sections. Many of the blocks perform multiple functions, and are user configurable.

The PSD4135G2 and PSD4135G2V devices offer two methods to program PSD Flash memory while the PSD is soldered to a circuit board.

Figure 1. Block diagram



1.1 In-system programming (ISP) via JTAG

An IEEE 1149.1 compliant JTAG-ISP interface is included on the PSD enabling the entire device (both Flash memories, the PLD, and all configuration) to be rapidly programmed while soldered to the circuit board. This requires no MCU participation, which means the PSD can be programmed anytime, even while completely blank.

The innovative JTAG interface to Flash memories is an industry first, solving key problems faced by designers and manufacturing houses, such as:

1.1.1 First time programming

How do I get firmware into the Flash the very first time? JTAG is the answer, program the PSD while blank with no MCU involvement.

1.1.2 Inventory build-up of pre-programmed devices

How do I maintain an accurate count of pre-programmed Flash memory and PLD devices based on customer demand? How many and what version? JTAG is the answer, build your hardware with blank PSDs soldered directly to the board and then custom program just before they are shipped to customer. No more labels on chips and no more wasted inventory.

1.1.3 Expensive sockets

How do I eliminate the need for expensive and unreliable sockets? JTAG is the answer. Solder the PSD directly to the circuit board. Program first time and subsequent times with JTAG. No need to handle devices and bend the fragile leads.

1.2 In-application programming (IAP)

Two independent Flash memory arrays are included so the MCU can execute code from one memory while erasing and programming the other. Robust product firmware updates in the field are possible over any communication channel (CAN, Ethernet, UART, J1850, etc) using this unique architecture. Designers are relieved of these problems:

1.2.1 Simultaneous read and write to Flash memory

How can the MCU program the same memory from which it is executing code? It cannot. The PSD allows the MCU to operate the two Flash memories concurrently, reading code from one while erasing and programming the other during IAP.

1.2.2 Complex memory mapping

How can I map these two memories efficiently? A programmable decode PLD is embedded in the PSD. The concurrent PSD memories can be mapped anywhere in MCU address space, segment by segment with extremely high address resolution. As an option, the secondary Flash memory can be swapped out of the system memory map when IAP is complete. A built-in page register breaks the MCU address limit.

1.2.3 Separate program and data space

How can I write to Flash memory while it resides in “program” space during field firmware updates? My 80C51XA won’t allow it. The Flash PSD provides means to “reclassify” Flash memory as “data” space during IAP, then back to “program” space when complete.

1.2.4 PSDsoft™ Express

PSDsoft Express, a software development tool from ST, guides you through the design process step-by-step making it possible to complete an embedded MCU design capable of ISP/IAP in just hours. Select your MCU and PSDsoft Express takes you through the remainder of the design with point and click entry, covering PSD selection, pin definitions, programmable logic inputs and outpus, MCU memory map definition, ANSI-C code generation for your MCU, and merging your MCU firmware with the PSD design. When complete, two different device programmers are supported directly from PSDsoft Express: FlashLINK (JTAG) and PSDpro.

Figure 2. Logic diagram

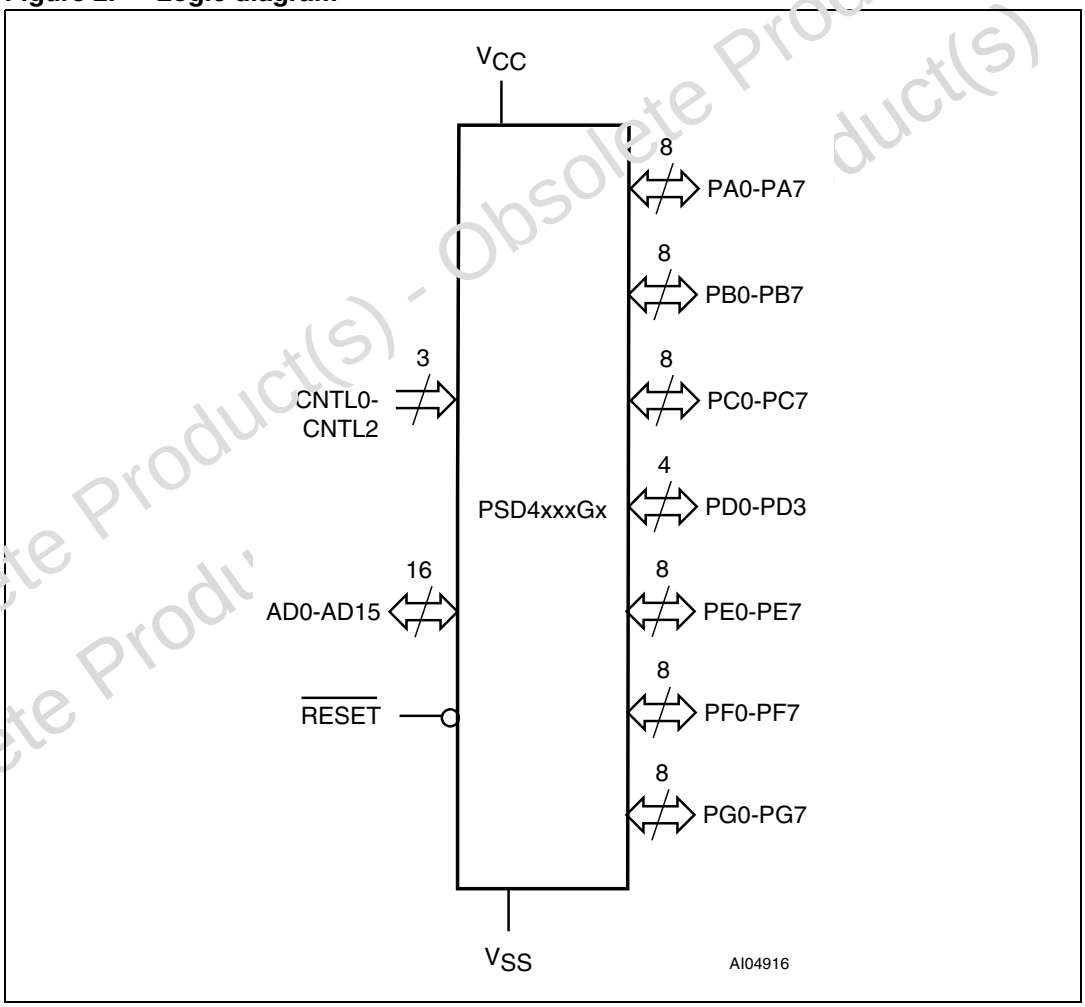
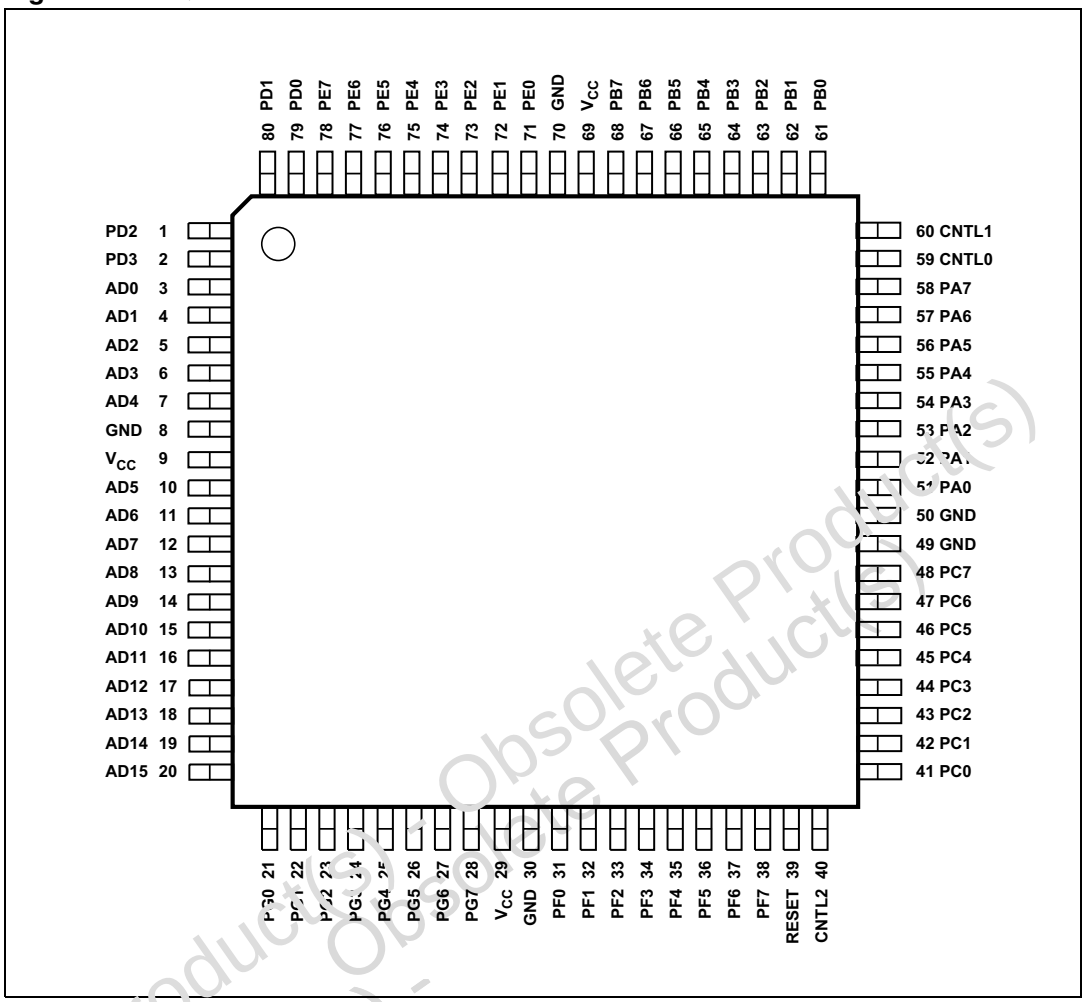


Table 1. Pin names

Pin	Description
PA0-PA7	Port-A
PB0-PB7	Port-B
PC0-PC7	Port-C
PD0-PD3	Port-D
PE0-PE7	Port-E
PF0-PF7	Port-F
PG0-PG7	Port-G
AD0-AD15	Address/Data
CNTL0-CNTL2	Control
$\overline{\text{RESET}}$	Reset
V_{CC}	Supply voltage
V_{SS}	Ground

Figure 3. LQFP connections



2 Pin description

Table 2 describes the pin names and pin functions of the PSD4135G2 and PSD4135G2V. Pins that have multiple names and/or functions are defined using PSDsoft Express.

Table 2. Pin description

Pin name	Pin	Type	Description
ADIO0-ADIO7	3-7 10-12	I/O	This is the lower Address/Data port. Connect your MCU address or address/data bus according to the following rules: 1. If your MCU has a multiplexed address/data bus where the data is multiplexed with the lower address bits, connect AD0-AD7 to this port. 2. If your MCU does not have a multiplexed address/data bus, connect A0-A7 to this port. 3. If you are using an 80C51XA in burst mode, connect A4/D0 through A11/D7 to this port. ALE or AS latches the address. The PSD drives data out only if the READ signal is active and one of the PSD functional blocks has been selected. The addresses on this port are passed to the PLDs.
ADIO8-ADIO15	13-20	I/O	This is the upper Address/Data port. Connect your MCU address or address/data bus according to the following rules: 1. If your MCU has a multiplexed address/data bus where the data is multiplexed with the upper address bits, connect A8-A15 to this port. 2. If your MCU does not have a multiplexed address/data bus, connect A8-A15 to this port. 3. If you are using an 80C51XA in burst mode, connect A12/D8 through A19/D15 to this port. ALE or AS latches the address. The PSD drives data out only if the READ signal is active and one of the PSD functional blocks has been selected. The addresses on this port are passed to the PLDs.
CNTL0	59	I	The following control signals can be connected to this pin, based on your MCU: 1. $\overline{WR}$ - active low, Write Strobe input. 2. R_$\overline{W}$ - active high, READ/active low WRITE input. 3. $\overline{WRL}$ - active low, WRITE to low-byte. This pin is connected to the PLDs. Therefore, these signals can be used in decode and other logic equations.
CNTL1	60	I	The following control signals can be connected to this pin, based on your MCU: 1. $\overline{RD}$ - active low, Read Strobe input. 2. E - E clock input. 3. $\overline{DS}$ - active low, Data Strobe input. 4. $\overline{LDS}$ - active low, Strobe for low data byte. This pin is connected to the PLDs. Therefore, these signals can be used in decode and other logic equations.

Table 2. Pin description (continued)

Pin name	Pin	Type	Description
CNTL2	40	I	READ or other Control input pin, with multiple configurations. Depending on the MCU interface selected, this pin can be: 1. $\overline{\text{PSEN}}$ - Program Select Enable, active low in code fetch bus cycle (80C51XA mode). 2. BHE - high-byte enable, 16-bit data bus. 3. $\overline{\text{UDS}}$ - active low, Strobe for high data byte, 16-bit data bus mode. 4. SIZ0 - Byte enable input. 5. $\overline{\text{LSTRB}}$ - low Strobe input. This pin is also connected to the PLDs.
$\overline{\text{RESET}}$	39	I	Active low input. Resets I/O Ports, PLD macrocells and some of the Configuration registers and JTAG registers. Must be low at Power-up. Reset also aborts any Flash memory Program or Erase cycle that is currently in progress.
PA0-PA7	51-58	I/O CMOS or Open Drain	These pins make up Port A. These port pins are configurable and can have the following functions: 1. MCU I/O - standard output or input port. 2. GPLD macrocell outputs. 3. Latched, transparent or registered PLD inputs (can also be PLD input for address A16 and above).
PB0-PB7	61-68	I/O CMOS or Open Drain	These pins make up Port B. These port pins are configurable and can have the following functions: 1. MCU I/O - standard output or input port. 2. GPLD macrocell outputs. 3. Latched, transparent or registered PLD inputs (can also be PLD input for address A16 and above).
PC0-PC7	41-48	I/O CMOS or Slew Rate	These pins make up Port C. These port pins are configurable and can have the following functions: 1. MCU I/O - standard output or input port. 2. External Chip Select (ECS0-ECS7) outputs. 3. Latched, transparent or registered PLD inputs (can also be PLD input for address A16 and above).
PD0	79	I/O CMOS or Open Drain	PD0 pin of Port D. This port pin can be configured to have the following functions: 1. ALE/AS input - latches address on ADIO0-ADIO15. 2. $\overline{\text{AS}}$ input - latches address on ADIO0-ADIO15 on the rising edge. 3. MCU I/O - standard output or input port. 4. Transparent PLD input (can also be PLD input for address A16 and above).
PD1	80	I/O CMOS or Open Drain	PD1 pin of Port D. This port pin can be configured to have the following functions: 1. MCU I/O - standard output or input port. 2. Transparent PLD input (can also be PLD input for address A16 and above). 3. CLKIN - clock input to the GPLD macrocells, the APD Unit's Power-down counter, and the GPLD AND Array.

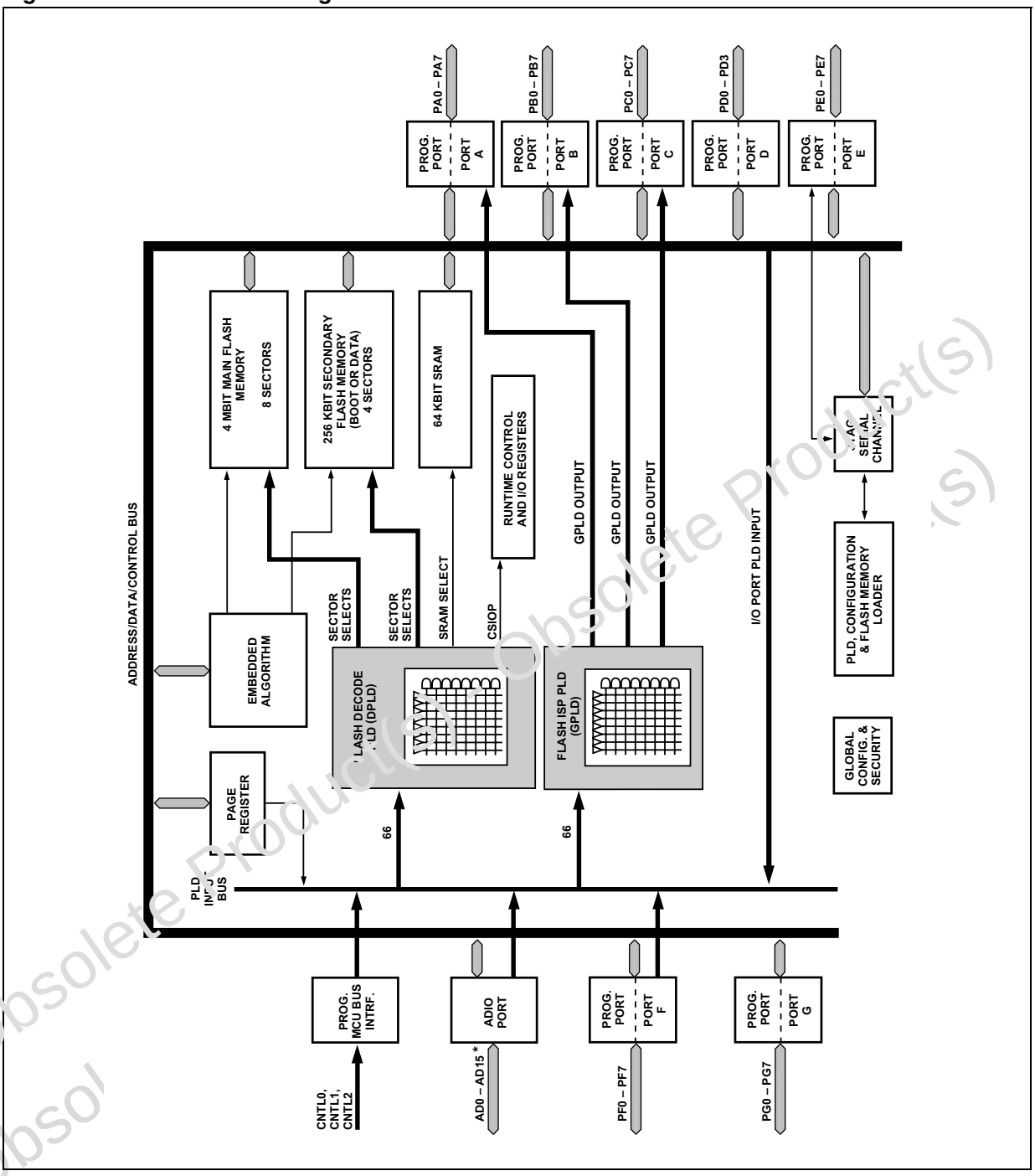
Table 2. Pin description (continued)

Pin name	Pin	Type	Description
PD2	1	I/O CMOS or Open Drain	PD2 pin of Port D. This port pin can be configured to have the following functions: 1. MCU I/O - standard output or input port. 2. Transparent PLD input (can also be PLD input for address A16 and above). 3. PSD Chip Select input ($\overline{CSI}$). When low, the MCU can access the PSD memory and I/O. When high, the PSD memory blocks are disabled to conserve power. The falling edge of this signal can be used to get the device out of Power-down mode.
PD3	2	I/O CMOS or Open Drain	PD3 pin of Port D. This port pin can be configured to have the following functions: 1. MCU I/O - standard output or input port. 2. Transparent PLD input (can also be PLD input for address A16 and above) 3. $\overline{WRH}$ - for 16-bit data bus, WRITE to high byte, active low.
PE0	71	I/O CMOS or Open Drain	PE0 pin of Port E. This port pin can be configured to have the following functions: 1. MCU I/O - standard output or input port. 2. Latched address output. 3. TMS input for the JTAG Serial Interface.
PE1	72	I/O CMOS or Open Drain	PE1 pin of Port E. This port pin can be configured to have the following functions: 1. MCU I/O - standard output or input port. 2. Latched address output. 3. TCK input for the JTAG Serial Interface.
PE2	73	I/O CMOS or Open Drain	PE2 pin of Port E. This port pin can be configured to have the following functions: 1. MCU I/O - standard output or input port. 2. Latched address output. 3. TDI input for the JTAG Serial Interface.
PE3	74	I/O CMOS or Open Drain	PE3 pin of Port E. This port pin can be configured to have the following functions: 1. MCU I/O - standard output or input port. 2. Latched address output. 3. TDO output for the JTAG Serial Interface.
PE4	75	I/O CMOS or Open Drain	PE4 pin of Port E. This port pin can be configured to have the following functions: 1. MCU I/O - standard output or input port. 2. Latched address output. 3. TSTAT output for the JTAG Serial Interface. 4. Ready/$\overline{Busy}$ output for parallel in-system programming (ISP).
PE5	76	I/O CMOS or Open Drain	PE5 pin of Port E. This port pin can be configured to have the following functions: 1. MCU I/O - standard output or input port. 2. Latched address output. 3. $\overline{TERR}$ active low output for the JTAG Serial Interface.
PE6	77	I/O CMOS or Open Drain	PE6 pin of Port E. This port pin can be configured to have the following functions: 1. MCU I/O - standard output or input port. 2. Latched address output.

Table 2. Pin description (continued)

Pin name	Pin	Type	Description
PE7	78	I/O CMOS or Open Drain	PE7 pin of Port E. This port pin can be configured to have the following functions: 1. MCU I/O - standard output or input port. 2. Latched address output.
PF0-PF7	31-38	I/O CMOS or Open Drain	These pins make up Port F. These port pins are configurable and can have the following functions: 1. MCU I/O - standard output or input port. 2. Inputs to GPLD. 3. Latched address outputs. 4. Address A1-A3 inputs in 80C51XA mode (PF0 is grounded) 5. Data bus port (D0-D7) in a non-multiplexed bus configuration. 6. MCU reset mode.
PG0-PG7	21-28	I/O CMOS or Open Drain	These pins make up Port G. These port pins are configurable and can have the following functions: 1. MCU I/O - standard output or input port. 2. Latched address outputs. 3. Data bus port (D8-D15) in a non-multiplexed bus configuration. 4. MCU reset mode.
V_{CC}	9, 29, 69		Supply voltage
GND	8, 30, 49, 50, 70		Ground pins

Figure 4. Detailed block diagram



1. Additional address lines can be brought into PSD via Port A, B, C, D, or F.

3 PSD architectural overview

PSD4135G2 and PSD4135G2V devices contain several major functional blocks. *Figure 4: Detailed block diagram* shows the architecture of the device family. The functions of each block are described briefly in the following sections. Many of the blocks perform multiple functions and are user configurable.

3.1 Memory

The devices contain the following memories:

- 4 Mbit Flash
- A secondary 256 Kbit Flash memory for boot or data
- 64 Kbit SRAM.

The 4 Mbit Flash is the main memory of the PSD4135G2/G2V. It is divided into eight equally-sized sectors that are individually selectable.

The 256 Kbit secondary Flash memory is divided into four equally-sized sectors. Each sector is individually selectable.

The 64 Kbit SRAM is intended for use as a scratchpad memory or as an extension to the microcontroller SRAM.

Each block of memory can be located in a different address space as defined by the user. The access times for all memory types includes the address latching and DPLD decoding time.

3.2 PLDs

The device contains two PLD blocks, each optimized for a different function, as shown in *Table 3*. The functional partitioning of the PLDs reduces power consumption, optimizes cost/performance, and eases design entry.

The decode PLD (DPLD) is used to decode addresses and generate chip selects for the PSD4135G2/G2V internal memory and registers. The general purpose PLD (GPLD) can implement user-defined external chip selects and logic functions. The PLDs receive their inputs from the PLD input bus and are differentiated by their output destinations, number of Product Terms.

The PLDs consume minimal power by using zero-power design techniques. The speed and power consumption of the PLD is controlled by the Turbo bit in the PMMR0 register and other bits in the PMMR2 registers. These registers are set by the microcontroller at runtime. There is a slight penalty to PLD propagation time when invoking the non-Turbo bit.

3.3 I/O ports

The PSD4135G2 and PSD4135G2V have 52 I/O pins divided among seven ports (Port A, B, C, D, E, F and G). Each I/O pin can be individually configured for different functions. Ports can be configured as standard MCU I/O ports, PLD I/O, or latched address outputs for microcontrollers using multiplexed address/data busses.

The JTAG pins can be enabled on Port E for in-system programming (ISP).

Ports F and G can also be configured as a data port for a non-multiplexed bus.

3.4 MCU bus interface

The PSD4135G2 and PSD4135G2V easily interface with most 16-bit microcontrollers that have either multiplexed or non-multiplexed address/data busses. The devices are configured to respond to the microcontroller's control signals, which are also used as inputs to the PLDs.

Table 3. PLD I/O

Name	Inputs	Outputs	Product terms
Decode PLD (DPLD)	66	14	40
General purpose PLD (GPLD)	66	24	136

3.5 ISP via JTAG port

In-system programming can be performed through the JTAG pins on Port E. This serial interface allows complete programming of the entire PSD4135G2/G2V devices. A blank device can be completely programmed. The JTAG signals (TMS, TCK, TSTAT, $\overline{\text{TERR}}$, TDI, TDO) can be multiplexed with other functions on Port E. *Table 4* indicates the JTAG signals pin assignments.

Table 4. JTAG signals on port E

Port E pins	JTAG signal
PE0	TMS
PE1	TCK
PE2	TDI
PE3	TDO
PE4	TSTAT
PE5	$\overline{\text{TERR}}$

3.6 In-system programming (ISP)

Using the JTAG signals on Port E, the entire PSD4135G2/G2V (memory, logic, configuration) devices can be programmed or erased without the use of the microcontroller.

3.7 In-application programming (IAP)

The main Flash memory can also be programmed in-system by the microcontroller executing the programming algorithms out of the secondary Flash memory, or SRAM. Since this is a sizable separate block, the application can also continue to operate. The secondary Flash boot memory can be programmed the same way by executing out of the main Flash memory. *Table 5* indicates which programming methods can program different functional blocks of the PSD4135G2/G2V.

Table 5. Methods of programming different functional blocks of the PSD

Functional block	JTAG-ISP	Device programmer	IAP
Primary Flash memory	Yes	Yes	Yes
Secondary Flash memory	Yes	Yes	Yes
PLD Array (DPLD and GPLD)	Yes	Yes	No
PSD configuration	Yes	Yes	No

3.8 Page register

The eight-bit Page Register expands the address range of the microcontroller by up to 256 times.The paged address can be used as part of the address space to access external memory and peripherals or internal memory and I/O. The Page Register can also be used to change the address mapping of blocks of Flash memory into different memory spaces for IAP.

3.9 Power management unit (PMU)

The power management unit (PMU) in the PSD4135G2/G2V gives the user control of the power consumption on selected functional blocks based on system requirements. The PMU includes an automatic power-down unit (APD) that will turn off device functions due to microcontroller inactivity. The APD unit has a Power-down mode that helps reduce power consumption.

The PSD4135G2 and PSD4135G2V also have some bits that are configured at run-time by the MCU to reduce power consumption of the GPLD. The turbo bit in the PMMR0 register can be turned off and the GPLD will latch its outputs and go to standby until the next transition on its inputs.

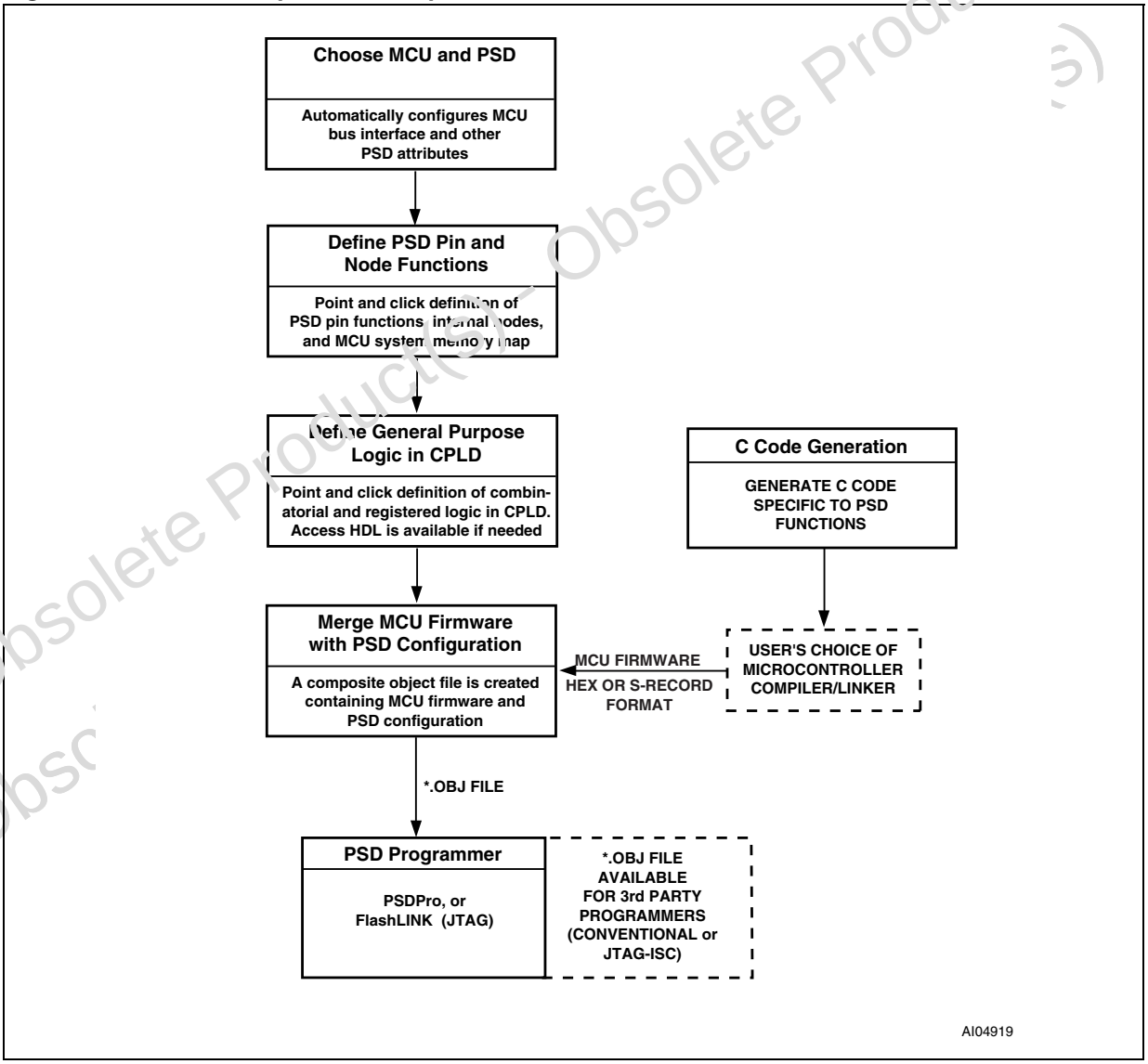
Additionally, bits in the PMMR2 register can be set by the MCU to block signals from entering the GPLD to reduce power consumption (see *Section 11: Power management*).

4 Development system

The PSD4135G2/G2V series is supported by PSDsoft a Windows-based (95, 98, NT) software development tool. A PSD design is quickly and easily produced in a point and click environment. The designer does not need to enter Hardware Definition Language (HDL) equations (unless desired) to define PSD pin functions and memory map information. The general design flow is shown in *Figure 5* below. PSDsoft is available from our web site (www.psdst.com) or other distribution channels.

PSDsoft directly supports two low cost device programmers from ST, PSDpro and FlashLINK (JTAG). Both of these programmers may be purchased through your local rep/distributor, or directly from our web site using a credit card. The PSD4135G2 and PSD4135G2V are also supported by third party device programmers, see web site for current list.

Figure 5. PSDsoft Express development tool



5 PSD register description and address offsets

Table 6 shows the offset addresses to the PSD registers relative to the CSIOP base address. The CSIOP space is the 256 bytes of address that is allocated by the user to the internal PSD registers. *Table 6* provides brief descriptions of the registers in CSIOP space.

The following sections give a more detailed description.

Table 6. Register address offset

Register name	Port A	Port B	Port C	Port D	Port E	Port F	Port G	Other(1)	Description
Data In	00	01	10	11	30	40	41		Reads Port pin as input, MCU I/O input mode
Control					32	42	43		Selects mode between MCU I/O or Address Out
Data Out	04	05	14	15	34	44	45		Stores data for output to Port pins, MCU I/O output mode
Direction	06	07	16	17	36	46	47		Configures Port pin as input or output
Drive Select	08	09	18	19	38	48	49		Configures Port pins as either CMOS or Open Drain on some pins, while selecting high slew rate on other pins.
Flash Memory Protection								C0	Read only - Primary Flash Sector Protection
Flash Boot Protection								C2	Read only - PSD Security and secondary Flash memory Sector Protection
PMMR0								B0	Power Management register 0
PMMR2								B4	Power Management register 2
Page								E0	Page register
VM								E2	Places PSD memory areas in Program and/or Data space on an individual basis.
Memory_ID0								F0	Read only - SRAM and Primary memory size
Memory_ID1								F1	Read only - Secondary memory type and size

1. Other registers that are not part of the I/O ports.

6 Register bit definition

All the registers in the PSD4135G2/G2V are included here for reference. Detail description of the registers are found in the functional block sections of the datasheet.

6.1 Data-In registers - port A, B, C, D, E, F, G

Read Port pin status when Port is in MCU I/O input mode.

Read-only registers.

Table 7. Data-In registers - Ports A, B, C, D, E, F, G

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port pin 7	Port pin 6	Port pin 5	Port pin 4	Port pin 3	Port pin 2	Port pin 1	Port pin 0

6.2 Data-out registers - port A, B, C, D, E, F, G

Latched data for output to Port pin when pin is configured in MCU I/O output mode.

Table 8. Data-Out registers - Ports A, B, C, D, E, F, G

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port pin 7	Port pin 6	Port pin 5	Port pin 4	Port pin 3	Port pin 2	Port pin 1	Port pin 0

6.3 Direction registers - ports A, B, C, D, E, F, G

Table 9. Direction registers - Ports A, B, C, D, E, F, G

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port pin 7	Port pin 6	Port pin 5	Port pin 4	Port pin 3	Port pin 2	Port pin 1	Port pin 0

Port pin <i>:

0: Port pin <i> is configured in input mode (default).

1: Port pin <i> is configured in output mode.

6.4 Control registers

Table 10. Control registers - Ports E, F, G

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port pin 7	Port pin 6	Port pin 5	Port pin 4	Port pin 3	Port pin 2	Port pin 1	Port pin 0

Port pin <i>:

0: Port pin <i> is configured in MCU I/O mode (default).

1: Port pin <i> is configured in Latched Address Out mode.

6.5 Drive registers - Ports A, B, D, E, G

Table 11. Drive registers - Ports A, B, D, E, G

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port pin 7	Port pin 6	Port pin 5	Port pin 4	Port pin 3	Port pin 2	Port pin 1	Port pin 0

Port pin <i>:

0: Port pin <i> is configured for CMOS output driver (default).

1: Port pin <i> is configured for Open Drain output driver.

6.6 Drive registers - Ports C and F

Table 12. Drive registers - Ports C, F

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port pin 7	Port pin 6	Port pin 5	Port pin 4	Port pin 3	Port pin 2	Port pin 1	Port pin 0

Port pin <i>:

0: Port pin <i> is configured for CMOS output driver (default).

1: Port pin <i> is configured in Slew Rate mode.

6.7 Flash Memory Protection register

Read-only register

Table 13. Flash Memory Protection register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Sec7_Prot	Sec6_Prot	Sec5_Prot	Sec4_Prot	Sec3_Prot	Sec2_Prot	Sec1_Prot	Sec0_Prot

Sec<i>_Prot:

1: Primary Flash memory Sector <i> is write protected.

0: Primary Flash memory Sector <i> is not write protected.

6.8 Flash Boot Protection register

Table 14. Flash Boot Protection register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Security_ Bit	not used	not used	not used	Sec3_Prot	Sec2_Prot	Sec1_Prot	Sec0_Prot

Sec<i>_Prot:

1: Secondary Flash memory Sector <i> is write protected.

0: Secondary Flash memory Sector <i> is not write protected.

Security_Bit:

0: Security bit in device has not been set.

1: Security bit in device has been set.

6.9 Page register

This register configures the page input to PLD.

Default value is PGR7-PGR0=0.

Table 15. Page register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PGR 7	PGR 6	PGR 5	PGR 4	PGR 3	PGR 2	PGR 1	PGR 0

6.10 PMMR0 register

The bits of this register are cleared to zero following Power-up. Subsequent Reset ($\overline{\text{RESET}}$) pulses do not clear the registers.

Table 16. PMMR0 register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
not used (set to '0')	not used (set to '0')	not used (set to '0')	PLD Array CLK	PLD Turbo	not used (set to '0')	APD Enable	not used (set to '0')

APD Enable:

0: Automatic power-down (APD) is disabled.

1: Automatic power-down (APD) is enabled.

PLD Turbo:

0: PLD Turbo is on.

1: PLD Turbo is off, saving power.

PLD Array CLK:

0: CLKIN to the PLD AND array is connected. Every CLKIN change powers up the PLD when Turbo bit is off.

1: CLKIN to the PLD AND array is disconnected, saving power.

6.11 PMMR2 register

Table 17. PMMR2 register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
not used (set to '0')	PLD Array $\overline{WRH}$	PLD Array ALE	PLD Array CNTL2	PLD Array CNTL1	PLD Array CNTL0	not used (set to '0')	PLD Array Addr

For bit 4, bit 3, bit 2: See *Table 27* for the signals that are blocked on pins CNTL0-CNTL2.

PLD Array Addr:

0: Address A7-A0 are connected to the PLD array.

1 Address A7-A0 are blocked from the PLD array, saving power.

Note: In XA mode, A3-A0 come from PF3-PF0, and A7-A4 come from ADIO7-ADIO4).

PLD Array CNTL2:

0: CNTL2 input to the PLD AND array is connected.

1: CNTL2 input to the PLD AND array is disconnected, saving power.

PLD Array CNTL1

0: CNTL1 input to the PLD AND array is connected.

1: CNTL1 input to the PLD AND array is disconnected, saving power.

PLD Array CNTL0

0: CNTL0 input to the PLD AND array is connected.

1: CNTL0 input to the PLD AND array is disconnected, saving power.

PLD Array ALE

0: ALE input to the PLD AND array is connected.

1: ALE input to the PLD AND array is disconnected, saving power.

PLD Array $\overline{WRH}$

0: $\overline{WRH}$/$\overline{DBE}$ input to the PLD AND array is connected.

1: $\overline{WRH}$/$\overline{DBE}$ input to the PLD AND array is disconnected, saving power.

6.12 VM register

Table 18. VM register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Peripheral mode	not used (set to '0')	not used (set to '0')	FL_data	Boot_data	FL_code	Boot_code	SR_code

On reset, bit1-Bit4 are loaded to configurations that are selected by the user in PSDsoft Express. bit0 and bit7 are always cleared on reset. bit0-Bit4 are active only when the device is configured in Philips 80C51XA mode.

SR_code

0 = $\overline{\text{PSEN}}$ cannot access SRAM in 80C51XA modes.

1 = $\overline{\text{PSEN}}$ can access SRAM in 80C51XA modes.

Boot_code

0 = $\overline{\text{PSEN}}$ cannot access Secondary NVM in 80C51XA modes.

1 = $\overline{\text{PSEN}}$ can access Secondary NVM in 80C51XA modes.

FL_code

0 = $\overline{\text{PSEN}}$ cannot access primary Flash memory in 80C51XA modes.

1 = $\overline{\text{PSEN}}$ can access primary Flash memory in 80C51XA modes.

Boot_data

0 = $\overline{\text{RD}}$ cannot access Secondary NVM in 80C51XA modes.

1 = $\overline{\text{RD}}$ can access Secondary NVM in 80C51XA modes.

FL_data

0 = $\overline{\text{RD}}$ cannot access primary Flash memory in 80C51XA modes.

1 = $\overline{\text{RD}}$ can access primary Flash memory in 80C51XA modes.

Peripheral mode

0 = Peripheral mode of Port F is disabled.

1 = Peripheral mode of Port F is enabled.

6.13 Memory_ID0 registers

Table 19. Memory_ID0 register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
S_size 3	S_size 2	S_size 1	S_size 0	F_size 3	F_size 2	F_size 1	F_size 0

F_size[3:0]

0h = There is no primary Flash memory
1h: Primary Flash memory size is 256 Kbit
2h: Primary Flash memory size is 512 Kbit
3h = Primary Flash memory size is 1 Mbit
4h = Primary Flash memory size is 2 Mbit
5h = Primary Flash memory size is 4 Mbit
6h = Primary Flash memory size is 8 Mbit

S_size[3:0]

0h = There is no SRAM
1h = SRAM size is 16 Kbit
2h = SRAM size is 32 Kbit
3h = SRAM size is 64 Kbit
4h = SRAM size is 128 Kbit
5h = SRAM size is 256 Kbit

6.14 Memory_ID1 register

Table 20. Memory_ID1 register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
not used (set to '0')	not used (set to '0')	B_type 1	B_type 0	B_size 3	B_size 2	B_size 1	B_size 0

B_size[3:0]

0h = There is no secondary NVM
1h = Secondary NVM size is 128 Kbit
2h = Secondary NVM size is 256 Kbit
3h = Secondary NVM size is 512 Kbit

B_type[1:0]

0h = Secondary NVM is Flash memory
1h = Secondary NVM is EEPROM

7 Memory blocks delailed operation

The PSD4135G2 and PSD4135G2V have the following memory blocks:

- The main Flash memory
- Secondary Flash memory
- SRAM.

The memory select signals for these blocks originate from the decode PLD (DPLD) and are user-defined in PSDsoft.

Table 21 summarizes which versions of the PSD4135G2/G2V contain which memory blocks.

Table 21. Memory block size and organization

Sector number	Primary Flash memory		Secondary Flash memory		SRAM	
	Sector size (x16, Kbytes)	Sector Select signal	Sector size (x16, Kbytes)	Sector Select signal	SRAM size (x16, Kbytes)	SRAM Select signal
0	32	FS0	4	CSBOOT0	4	RS0
1	32	FS1	4	CSBOOT1		
2	32	FS2	4	CSBOOT2		
3	32	FS3	4	CSBOOT3		
4	32	FS4				
5	32	FS5				
6	32	FS6				
7	32	FS7				
Total	**512 Kbytes**	**8 sectors**	**64 Kbytes**	**4 sectors**	**8 Kbytes**	

7.1 Primary Flash and secondary Flash memory description

The primary Flash memory block is divided evenly into eight sectors. The secondary Flash memory is divided into four sectors of eight Kbytes each. Each sector of either memory can be separately protected from program and erase operations.

Flash memory may be erased on a sector-by-sector basis and programmed word-by-word. Flash sector erasure may be suspended while data is read from other sectors of memory and then resumed after reading.

During a program or erase of Flash, the status can be output on the Rdy/Bsy pin of Port PE4. This pin is set up using PSDsoft Express.

7.1.1 Memory Block Selects signals

The decode PLD in the PSD4135G2/G2V generates the chip selects for all the internal memory blocks (refer to *Section 8: PLDs*). Each of the eight Flash memory sectors have a Flash Select signal (FS0-FS7) which can contain up to three product terms. Each of the four secondary Flash memory sectors have a Select signal (CSBOOT0-3) which can contain up to three product terms. Having three product terms for each sector select signal allows a given sector to be mapped in different areas of system memory. When using a microcontroller (80C51XA) with separate Program and Data space, these flexible select signals allow dynamic re-mapping of sectors from one space to the other before and after IAP.

7.1.2 Ready/Busy pin (PE4)

Pin PE4 can be used to output the Ready/Busy status of the PSD4135G2/G2V. The output on the pin will be a '0' (Busy) when Flash memory blocks are being written to, or when the Flash memory block is being erased. The output will be a '1' (Ready) when no write or erase operation is in progress.

7.1.3 Memory Operation

The primary Flash and secondary Flash memories are addressed through the microcontroller interface on the PSD4135G2G2V devices. The microcontroller can access these memories in one of two ways:

- The microcontroller can execute a typical bus write or read operation just as it would if accessing a RAM or ROM device using standard bus cycles.
- The microcontroller can execute a specific instruction that consists of several write and read operations. This involves writing specific data patterns to special addresses within the Flash to invoke an embedded algorithm. These instructions are summarized in *Table 22*.

Typically, Flash memory can be read by the microcontroller using read operations, just as it would read a ROM device. However, Flash memory can only be erased and programmed with specific instructions. For example, the microcontroller cannot write a single word directly to Flash memory as one would write a word to RAM. To program a word into Flash memory, the microcontroller must execute a program instruction sequence, then test the status of the programming event. This status test is achieved by a read operation or polling the Rdy/Busy pin (PE4).

The Flash memory can also be read by using special instructions to retrieve particular Flash device information (sector protect status and ID).

Instructions

An instruction is defined as a sequence of specific operations. Each received byte is sequentially decoded by the PSD and not executed as a standard write operation. The instruction is executed when the correct number of bytes are properly received and the time between two consecutive bytes is shorter than the time-out value. Some instructions are structured to include read operations after the initial write operations.

The sequencing of any instruction must be followed exactly. Any invalid combination of instruction bytes or time-out between two consecutive bytes while addressing Flash memory will reset the device logic into a read array mode (Flash memory reads like a ROM device).

The PSD4135G2/G2V main Flash and secondary Flash support these instructions (see *Table 22*):

- Erase memory by chip or sector
- Suspend or resume sector erase
- Program a word
- Reset to read array mode
- Read Main Flash Identifier value
- Read sector protection status
- Bypass Instruction

These instructions are detailed in *Table 22*. For efficient decoding of the instructions, the first two bytes of an instruction are the coded cycles and are followed by a command byte or confirmation byte. The coded cycles consist of writing the data byte AAh to address XAAAh during the first cycle and data byte 55h to address X554h during the second cycle (unless the Bypass Instruction feature is used). Address lines A15-A12 are don't care during the instruction write cycles. However, the appropriate sector select signal (FSi or CSBOOTi) must be selected.

The main Flash and the secondary Flash Block have the same set of instructions (except Read main Flash ID). The chip selects of the Flash memory will determine which Flash will receive and execute the instruction. The main Flash is selected if any one of the FS0-7 is active, and the secondary Flash Block is selected if any one of the CSBOOT0-3 is active.

Table 22. Instructions(1)(2)(3)

Instruction(4)	FS0-FS7 or CSBOOT0-CSBOOT3(5)	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7
READ(6)	1	"Read" RD @ RA						
Read Main Flash ID(7)	1	AAh@ XAAAh	55h@ X554h	90h@ XAAAh	Read ID @ XX02h			
Read Sector Protection(7)(8)(9)	1	AAh@ XAAAh	55h@ X554h	90h@ XAAAh	Read 00h or 01h @ XX04h			
Program a Flash Word(9)	1	AAh@ XAAAh	55h@ X554h	A0h@ XAAAh	PD@ PA			
Flash Sector Erase(10)(9)	1	AAh@ XAAAh	55h@ X554h	80h@ XAAAh	AAh@ XAAAh	55h@ X554h	30h@ SA	30h(10) @ next SA
Flash Bulk Erase(9)	1	AAh@ XAAAh	55h@ X554h	80h@ XAAAh	AAh@ XAAAh	55h@ X554h	10h@ XAAAh	
Suspend Sector Erase(11)	1	B0h@ XXXXh						
Resume Sector Erase(12)	1	30h@ XXXXh						
Reset(7)	1	F0h@ XXXXh						

Table 22. Instructions(1)(2)(3) (continued)

Instruction(4)	FS0-FS7 or CSBOOT0-CSBOOT3(5)	Cycle 1	Cycle 2	Cycle 3	Cycle 4	Cycle 5	Cycle 6	Cycle 7
Unlock Bypass	1	AAh@ XAAAh	55h@ X554h	20h@ XAAAh				
Unlock Bypass Program(13)	1	A0h@ XXXXh	PD@ PA					
Unlock Bypass Reset(14)	1	90h@ XXXXh	00h@ XXXXh					

1. All bus cycles are WRITE bus cycles, except the ones with the “Read” label
2. All values are in hexadecimal:
   X = Don’t Care. Addresses of the form XXXXh, in this table, must be even addresses, RA = Address of the memory location to be read
   RD = Data read from location RA during the READ cycle
   PA = Address of the memory location to be programmed. Addresses are latched on the falling edge of Write Strobe ($\overline{WR}$, CNTL0). PA is an even address for PSD in word programming mode.
   PD = Data word to be programmed at location PA. Data is latched on the rising edge of Write Strobe ($\overline{WR}$, CNTL0)
   SA = Address of the sector to be erased or verified. The Sector Select (FS0-FS7 or CSBOOT0-CSBOOT3) of the sector to be erased, or verified, must be Active (High).
3. Only address bits A11-A0 are used in instruction decoding.
4. All WRITE bus cycles in an instruction are byte WRITE to an even address (XAAAh or X554h). A Flash memory Program bus cycle writes a word to an even address.
5. Sector Select (FS0 to FS7 or CSBOOT0 to CSBOOT3) signals are active high, and are defined in PSDsoft Express.
6. No Unlock or instruction cycles are required when the device is in the READ mode.
7. The Reset instruction is required to return to the READ mode after reading the Flash ID, or after reading the Sector Protection Status, or if the Error Flag bit (DQ5/DQ13) goes high.
8. The data is 00h for an unprotected sector, and 01h for a protected sector. In the fourth cycle, the Sector Select is active, and (A1,A0)=(1,0)
9. The MCU cannot invoke these instructions while executing code from the same Flash memory as that for which the instruction is intended. The MCU must fetch, for example, the code from the secondary Flash memory when reading the Sector Protection Status of the primary Flash memory.
10. Additional sectors to be erased must be written at the end of the Sector Erase instruction within 80µs.
11. The system may perform READ and Program cycles in non-erasing sectors, read the Flash ID or read the Sector Protection Status when in the Suspend Sector Erase mode. The Suspend Sector Erase instruction is valid only during a Sector Erase cycle.
12. The Resume Sector Erase instruction is valid only during the Suspend Sector Erase mode.
13. The Unlock Bypass instruction is required prior to the Unlock Bypass Program instruction.
14. The Unlock Bypass Reset Flash instruction is required to return to reading memory data when the device is in the Unlock Bypass mode.

7.1.4 Power-up condition

The PSD4135G2/G2V internal logic is reset upon power-up to the read array mode. The FSi and CSBOOTi select signals, along with the write strobe signal, must be in the false state during power-up for maximum security of the data contents and to remove the possibility of data being written on the first edge of a write strobe signal. Any write cycle initiation is locked when Vcc is below V_{LKO}.

7.1.5 Reading Flash memory

Under typical conditions, the microcontroller may read the Flash, or secondary Flash memories using read operations just as it would a ROM or RAM device. Alternately, the microcontoller may use read operations to obtain status information about a program or erase operation in progress. Lastly, the microcontroller may use instructions to read special data from these memories. The following sections describe these read functions.

Reading Memory content

Primary Flash and secondary Flash memories are placed in the read array mode after power-up, chip reset, or a Reset Flash instruction (see *Table 22*). The microcontroller can read the memory contents of primary Flash or secondary Flash by using read operations any time the read operation is not part of an instruction.

Reading Primary Flash Identifier

The primary Flash identifier is read with an instruction composed of 4 operations: 3 specific write operations and a read operation (see *Table 22*). The PSD4135G2/G2V primary Flash memory ID is E8h. The secondary Flash does not support this instruction.

Reading Memory Sector Protection status

The Flash memory sector protection status is read with an instruction composed of 4 operations: 3 specific write operations and a read operation (see *Table 22*). The read operation will produce 01h if the Flash sector is protected, or 00h if the sector is not protected.

The sector protection status for all NVM blocks (primary Flash or secondary Flash) can also be read by the microcontroller accessing the Flash Protection and Flash Boot Protection registers in PSD I/O space. See *Section 6.7: Flash Memory Protection register* and *Section 6.8: Flash Boot Protection register*.

Reading the Erase/Program Status bits

The PSD4135G2 and PSD4135G2V provide several status bits to be used by the microcontroller to confirm the completion of an erase or programming instruction of Flash memory. These status bits minimize the time that the microcontroller spends performing these tasks and are defined in *Table 23*. The status byte resides in even location and can be read as many times as needed. Please note DQ15-8 is even byte for Motorola MCUs with 16 bit data bus.

For Flash memory, the microcontroller can perform a read operation to obtain these status bits while an erase or program instruction is being executed by the embedded algorithm. Refer to *Section 7.1.6: Programming Flash memory* for details.

Table 23. Status bits

DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Data Polling	Toggle Flag	Error Flag	X	Erase timeout	X	X	X

Table 24. Status bits for Motorola(1)(2)(3)

DQ15	DQ14	DQ13	DQ12	DQ11	DQ10	DQ9	DQ8
Data Polling	Toggle Flag	Error Flag	X	Erase timeout	X	X	X

1. X = Not guaranteed value, can be read either 1 or 0.
2. DQ15-DQ0 represent the Data Bus bits, D15-D0.
3. FS0-FS7/CSBOOT0-CSBOOT3 are active high.

Data Polling flag DQ7 (DQ15 for Motorola)

When Erasing or Programming the Flash memory bit DQ7 (DQ15) outputs the complement of the bit being entered for Programming/Writing on DQ7 (DQ15). Once the Program instruction or the Write operation is completed, the true logic value is read on DQ7 (DQ15) (in a Read operation). Flash memory specific features:

- Data Polling is effective after the fourth Write pulse (for programming) or after the sixth Write pulse (for Erase). It must be performed at the address being programmed or at an address within the Flash sector being erased.
- During an Erase instruction, DQ7 (DQ15) outputs a '0'. After completion of the instruction, DQ7 (DQ15) will output the last bit programmed (it is a '1' after erasing).
- If the location to be programmed is in a protected Flash sector, the instruction is ignored.
- If all the Flash sectors to be erased are protected, DQ7 (DQ15) will be set to '0' for about 100 µs, and then return to the previous addressed location. No erasure will be performed.

Toggle flag DQ6 (DQ14 for Motorola)

The PSD4135G2 and PSD4135G2V offer another way for determining when the Flash memory Program instruction is completed. During the internal Write operation and when either the FSi or CSBOOTi is true, the DQ6 (DQ14) will toggle from '0' to '1' and '1' to '0' on subsequent attempts to read any word of the memory.

When the internal cycle is complete, the toggling will stop and the data read on the Data Bus is the addressed memory location. The device is now accessible for a new Read or Write operation. The operation is finished when two successive reads yield the same output data. Flash memory specific features:

- The Toggle bit is effective after the fourth Write pulse (for programming) or after the sixth Write pulse (for Erase).
- If the location to be programmed belongs to a protected Flash sector, the instruction is ignored.
- If all the Flash sectors selected for erasure are protected, DQ6 (DQ14) will toggle to '0' for about 100 µs and then return to the previous addressed location.

Error flag DQ5 (DQ14 for Motorola)

During a normal Program or Erase cycle, the Error bit will set to ‘0’. This bit is set to ‘1’ when there is a failure during Flash programming, Sector erase, or Bulk Erase.

In the case of Flash programming, the Error Bit indicates the attempt to program a Flash bit(s) from the programmed state (0) to the erased state (1), which is not a valid operation. The Error bit may also indicate a timeout condition while attempting to program a word.

In case of an error in Flash sector erase or word program, the Flash sector in which the error occurred or to which the programmed location belongs must no longer be used. Other Flash sectors may still be used. The Error bit resets after the Reset instruction. A reset instruction is required after detecting the error bit.

Erase Timeout flag DQ3 (DQ11 for Motorola)

The Erase Timer bit reflects the timeout period allowed between two consecutive Sector Erase instructions. The Erase timer bit is set to ‘0’ after a Sector Erase instruction for a time period of 100 µs + 20% unless an additional Sector Erase instruction is decoded.

After this time period or when the additional Sector Erase instruction is decoded, DQ3 (DQ11) is set to ‘1’. A reset instruction is required after detecting the erase timer bit.

7.1.6 Programming Flash memory

Flash memory must be erased prior to being programmed. The MCU may erase Flash memory all at once or by-sector. Flash memory sector erases to all logic ones, and its bits are programmed to logic zeros. Although erasing Flash memory occurs on a sector or chip basis, programming Flash memory occurs on a word basis.

The PSD4135G2/G2V primary Flash and secondary Flash memories require the MCU to send an instruction to program a word or perform an erase function (see *Table 22*).

Once the MCU issues a Flash memory program or erase instruction, it must check for the status of completion. The embedded algorithms that are invoked inside the PSD4135G2/G2V support several means to provide status to the MCU. Status may be checked using any of three methods: Data Polling, Data Toggle, or the Ready/Busy output pin.

Data polling

Polling on DQ7 (DQ15) is a method of checking whether a Program or Erase instruction is in progress or has completed. *Figure 6* shows the Data Polling algorithm.

When the MCU issues a programming instruction, the embedded algorithm within the PSD4135G2/G2V begins. The MCU then reads the location of the word to be programmed in Flash to check status. Data bit DQ7 (DQ15) of this location becomes the compliment of data bit 7of the original data word to be programmed. The MCU continues to poll this location, comparing DQ7 (DQ15) and monitoring the Error bit on DQ5 (DQ13). When the DQ7 (DQ15) matches data bit 7 of the original data, and the Error bit at DQ5 (DQ13) remains ‘0’, then the embedded algorithm is complete. If the Error bit at DQ5 is ‘1’, the MCU should test DQ7 (DQ15) again since DQ7 (DQ15) may have changed simultaneously with DQ5 (DQ13) (see *Figure 6*).

The Error bit at DQ5 (DQ13) will be set if either an internal timeout occurred while the embedded algorithm attempted to program the location or if the MCU attempted to program a ‘1’ to a bit that was not erased (not erased is logic ‘0’).

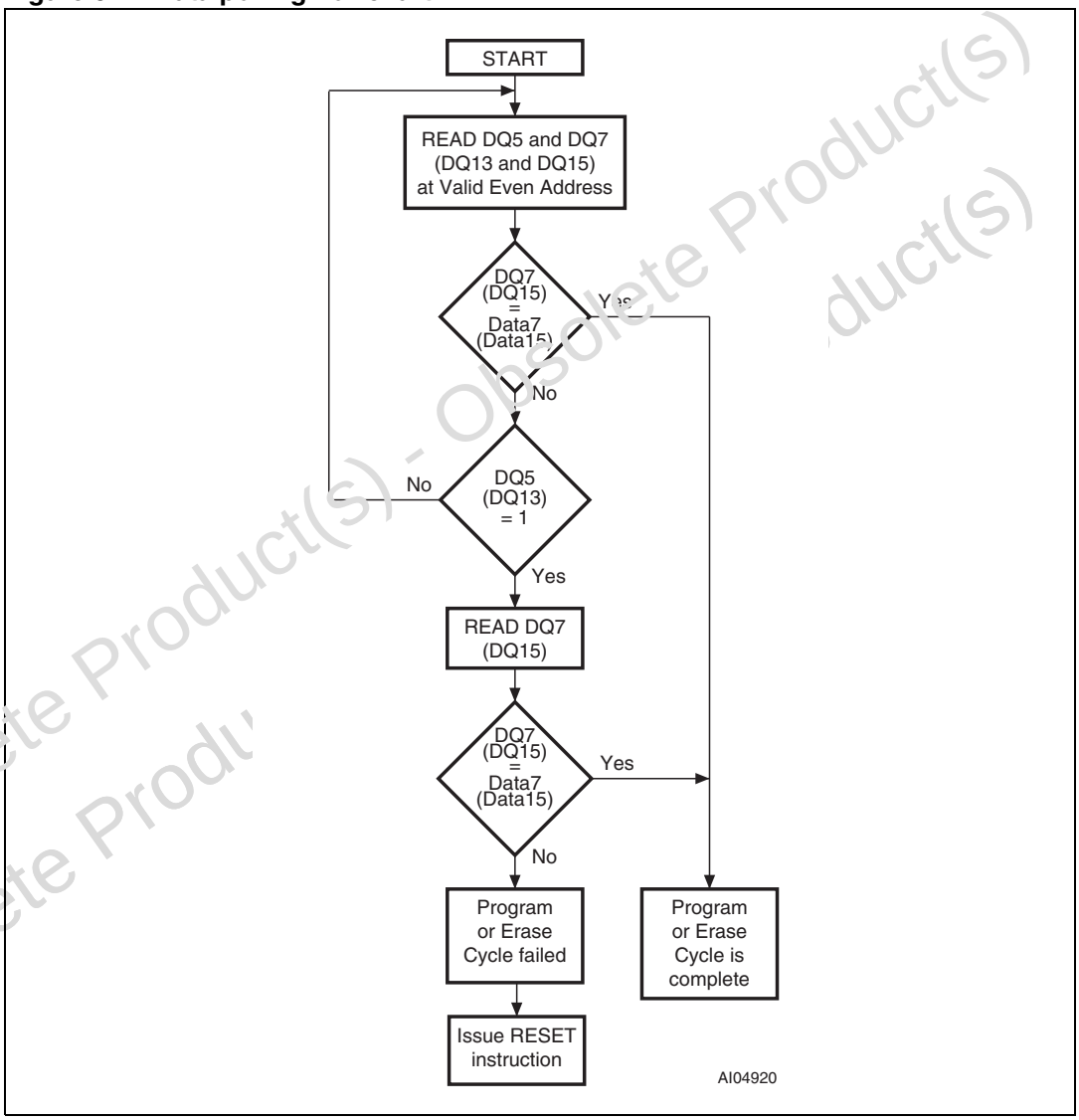
It is suggested (as with all Flash memories) to read the location again after the embedded programming algorithm has completed to compare the word that was written to Flash with the word that was intended to be written.

When using the Data Polling method after an erase instruction, *Figure 6* still applies. However, DQ7 (DQ15) will be '0' until the erase operation is complete. A '1' on DQ5 (DQ13) will indicate a timeout failure of the erase operation, a '0' indicates no error.

The MCU can read any location within the sector being erased to get DQ7 (DQ15) and DQ5 (DQ13) .

PSDsoft generates ANSI C code functions which implement these Data Polling algorithms.

Figure 6. Data polling flowchart



Data toggle

Checking the Data Toggle bit on DQ6 (DQ14) is a method of determining whether a Program or Erase instruction is in progress or has completed. *Figure 7* shows the Data Toggle algorithm.

When the MCU issues a programming instruction, the embedded algorithm within the PSD4135G2G2V begins. The MCU then reads the location to be programmed in Flash to check status. Data bit DQ6 (DQ14) of this location will toggle each time the MCU reads this location until the embedded algorithm is complete. The MCU continues to read this location, checking DQ6 (DQ14) and monitoring the Error bit on DQ5 (DQ13) . When DQ6 (DQ14) stops toggling (two consecutive reads yield the same value), and the Error bit on DQ5 (DQ13) remains '0', then the embedded algorithm is complete. If the Error bit on DQ5 (DQ13) is '1', the MCU should test DQ6 (DQ14) again, since DQ6 (DQ14) may have changed simultaneously with DQ5 (DQ13) (see *Figure 7*).

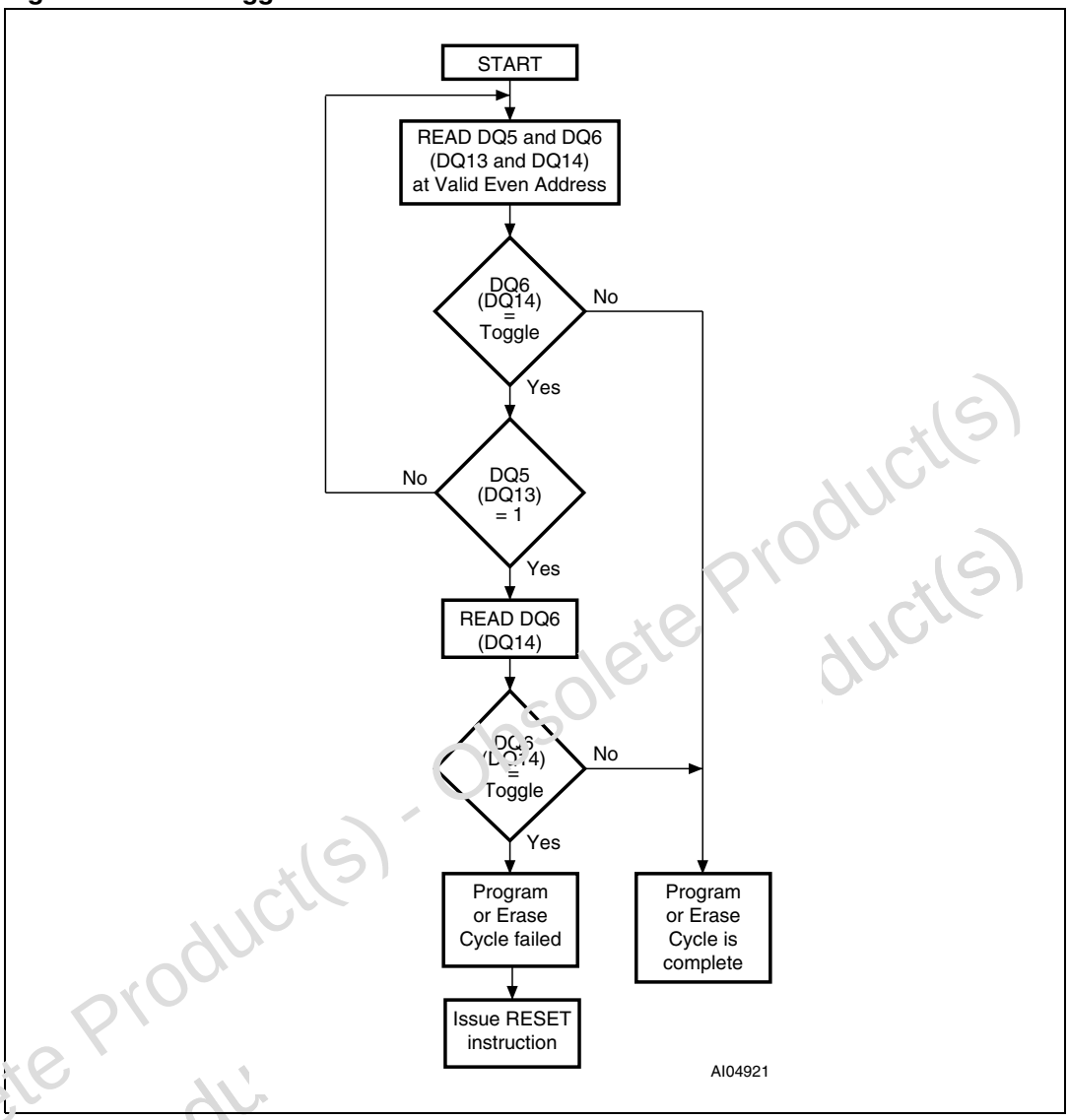
The Error bit at DQ5 (DQ13) will be set if either an internal timeout occurred while the embedded algorithm attempted to program, or if the MCU attempted to program a '1' to a bit that was not erased (not erased is logic '0').

It is suggested (as with all Flash memories) to read the location again after the embedded programming algorithm has completed to compare the word that was written to Flash with the word that was intended to be written.

When using the Data Toggle method after an erase instructin, *Figure 7* still applies. DQ6 (DQ14) will toggle until the erase operation is complete. A '1' on DQ5 (DQ13) will indicate a timeout failure of the erase operation, a '0' indicates no error. The MCU can read any even location within the sector being erased to get DQ6 (DQ14) and DQ5 (DQ13) .

PSDsoft generates ANSI C code functions which implement these Data Toggling algorithms.

Figure 7. Data toggle flowchart



7.1.7 Unlock Bypass

The unlock bypass feature allows the system to program words to the Flash memories faster than using the standard program instruction. The unlock bypass instruction is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h (see *Table 22*). The Flash memory then enters the unlock bypass mode. A two-cycle Unlock Bypass Program instruction is all that is required to program in this mode. The first cycle in this instruction contains the unlock bypass programm command, A0h; the second cycle contains the program address and data.

Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program instruction, resulting in faster total programming time. During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset instructions are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset instruction. The first cycle must contain the

data 90h; the second cycle the data 00h. Addresses are don't care for both cycles. The Flash memory then returns to reading array data mode.

7.1.8 Erasing Flash memory

Flash Bulk Erase

The Flash Bulk Erase instruction uses six write operations followed by a Read operation of the status register, as described in *Table 22*. If any byte of the Bulk Erase instruction is wrong, the Bulk Erase instruction aborts and the device is reset to the Read Flash memory status.

During a Bulk Erase, the memory status may be checked by reading status bits DQ5, DQ6, and DQ7 (DQ13, DQ14, DQ15), as detailed in *Section 7.1.6: Programming Flash memory*. The Error bit (returns a '1' if there has been an Erase Failure (maximum number of erase cycles have been executed).

It is not necessary to program the array with 00h because the PSD4135G2/G2V will automatically do this before erasing to 0FFh.

During execution of the Bulk Erase instruction, the Flash memory will not accept any instructions.

Flash Sector Erase

The Sector Erase instruction uses six write operations, as described in *Table 22*. Additional Flash Sector Erase confirm commands and Flash sector addresses can be written subsequently to erase other Flash sectors in parallel, without further coded cycles, if the additional instruction is transmitted in a shorter time than the timeout period of about 100 µs. The input of a new Sector Erase instruction will restart the timeout period.

The status of the internal timer can be monitored through the level of DQ3 (DQ11) (Erase timeout bit). If DQ3 (DQ11) is '0', the Sector Erase instruction has been received and the timeout is counting. If DQ3 (DQ11) is '1', the timeout has expired and the PSD4135G2/G2V is busy erasing the Flash sector(s). Before and during Erase timeout, any instruction other than Erase suspend and Erase Resume will abort the instruction and reset the device to Read Array mode. It is not necessary to program the Flash sector with 00h as the PSD4135G2/G2V will do this automatically before erasing.

During a Sector Erase, the memory status may be checked by reading status bits DQ5, DQ6, and DQ7 (DQ13, DQ14, DQ15), as detailed in *Section 7.1.6: Programming Flash memory*.

During execution of the erase instruction, the Flash block logic accepts only Reset and Erase Suspend instructions. Erasure of one Flash sector may be suspended, in order to read data from another Flash sector, and then resumed.

Suspend Sector Erase

When a Sector Erase operation is in progress, the Erase Suspend instruction will suspend the operation by writing 0B0h to any even address when an appropriate Chip Select (FSi or CSBOOTi) is true. (See *Table 22*). This allows reading of data from another Flash sector after the Erase operation has been suspended. Erase suspend is accepted only during the Flash Sector Erase instruction execution and defaults to read array mode. An Erase Suspend instruction executed during an Erase timeout will, in addition to suspending the erase, terminate the time out.

The Toggle Bit DQ6 stops toggling when the PSD4135G2/G2V internal logic is suspended. The toggle Bit status must be monitored at an address within the Flash sector being erased. The Toggle Bit will stop toggling between 0.1 µs and 15 µs after the Erase Suspend instruction has been executed. The PSD4135G2/G2V will then automatically be set to Read Flash block Memory Array mode.

If an Erase Suspend instruction was executed, the following rules apply:

- Attempting to read from a Flash sector that was being erased will output invalid data.
- Reading from a Flash sector that was not being erased is valid.
- The Flash memory cannot be programmed, and will only respond to Erase Resume and Reset instructions (read is an operation and is OK).
- If a Reset instruction is received, data in the Flash sector that was being erased will be invalid.

Resume Sector Erase

If an Erase Suspend instruction was previously executed, the erase operation may be resumed by this instruction. The Erase Resume instruction consists of writing 030h to any even address while an appropriate Chip Select (FSi or CSBOOT) is true (see *Table 22*)

7.1.9 Specific features

Primary and secondary Flash Sector Protect

Each sector of primary Flash and secondary Flash memory can be separately protected against Program and Erase functions. Sector Protection provides additional data security because it disables all program or erase operations. This mode can be activated (or deactivated) through the JTAG-ISP Port or a Device Programmer.

Sector protection can be selected for each sector using the PSDsoft program. This will automatically protect selected sectors when the device is programmed through the JTAG Port or a Device Programmer. Flash sectors can be unprotected to allow updating of their contents using the JTAG Port or a Device Programmer. The microcontroller can read (but cannot change) the sector protection bits.

Any attempt to program or erase a protected Flash sector will be ignored by the device.

The Verify operation will result in a read of the protected data. This allows a guarantee of the retention of the Protection status.

The sector protection status can either be read by the MCU through the Flash protection and secondary Flash protection registers (CSIOP), or use the Read Sector Protection instruction (see *Table 22*).

7.1.10 Reset

The Reset instruction consists of one write cycle (see *Table 22*). It can also be optionally preceded by the standard two write decoding cycles (writing AAh to AAAh and 55h to 554h). The Reset instruction must be executed after:

- Reading the Flash Protection status or Flash ID using the Flash instruction.
- When an error condition occurs (DQ5 (DQ13) goes high) during a Flash programming or erase cycle.

The Reset instruction will reset the Flash to normal Read mode immediately. However, if there is an error condition (DQ5 (DQ13) goes high), the Flash memory will return to the Read mode in 25 µs after the Reset instruction is issued.

The Reset instruction is ignored when it is issued during a Flash programming or Bulk Erase cycle. The Reset instruction will abort the on going sector erase cycle and return the Flash memory to normal Read mode in 25 µs.

7.1.11 Reset ($\overline{\text{RESET}}$) pin input

The reset pulse input from the pin will abort any operation in progress and reset the Flash memory to Read mode. When the reset occurs during a programming or erase cycle, the Flash memory will take up to 25 µs to return to Read mode. It is recommended that the reset pulse (except Power-on reset, see *Section 7.1.10: Reset*) be at least 25 µSeconds such that the Flash memory will always be ready for the MCU to fetch the boot code after reset is over.

7.2 SRAM

The SRAM is enabled when RS0—the SRAM chip select output from the DPLD—is high. RS0 can contain up to three product terms, allowing flexible memory mapping.

The Chip Select signal (RS0) for the SRAM is configured using PSDsoft.

7.3 Memory Select signals

The primary Flash (FSi), secondary Flash (CSBOOTi), and SRAM (RS0) memory select signals are all outputs of the DPLD. They are defined using PSDsoft. The following rules apply to the equations for the internal chip select signals:

- Primary Flash memory and secondary Flash memory sector select signals must not be larger than the physical sector size.
- Any primary Flash memory sector must not be mapped in the same memory space as another primary Flash sector.
- A secondary Flash memory sector must not be mapped in the same memory space as another Flash Boot sector.
- SRAM and I/O spaces must not overlap.
- A secondary Flash memory sector may overlap a primary Flash memory sector. In case of overlap, priority will be given to the Flash Boot sector.
- SRAM, I/O, and Peripheral I/O spaces may overlap any other memory sector. Priority will be given to the SRAM, and I/O.

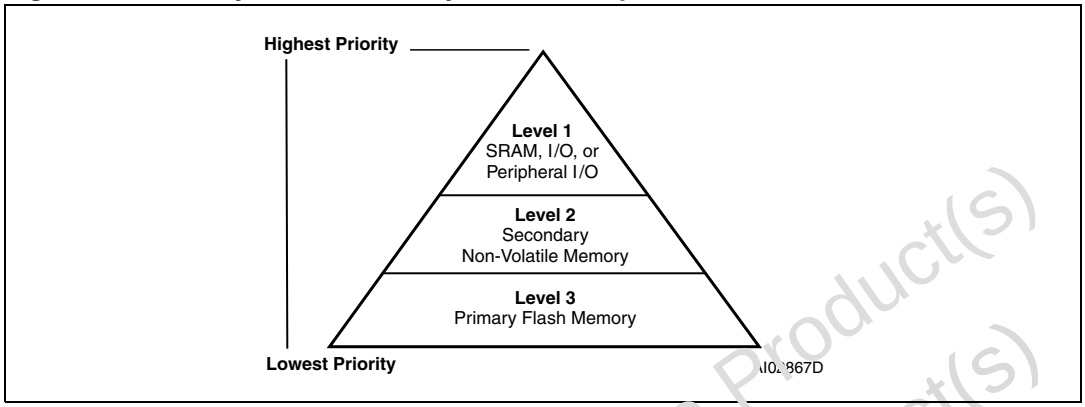
Example

FS0 is valid when the address is in the range of 8000h to BFFFh, CSBOOT0 is valid from 8000h to 9FFFh, and RS0 is valid from 8000h to 87FFh. Any address in the range of RS0 will always access the SRAM. Any address in the range of CSBOOT0 greater than 87FFh (and less than 9FFFh) will automatically address Boot memory segment 0. Any address greater than 9FFFh will access the Flash memory segment 0. You can see that half of the Flash memory segment 0 and one-fourth of Boot segment 0 can not be accessed in this

example. Also note that an equation that defined FS1 to anywhere in the range of 8000h to BFFFh would **not** be valid.

Figure 8 shows the priority levels for all memory components. Any component on a higher level can overlap and has priority over any component on a lower level. Components on the same level must **not** overlap. Level one has the highest priority and level 3 has the lowest.

Figure 8. Priority level of memory and I/O components



7.3.1 Memory select configuration for MCUs with separate program and data spaces

The 80C51XA and compatible family of micro controllers, can be configured to have separate address spaces for code memory (selected using $\overline{PSEN}$) and data memory (selected using $\overline{RD}$). Any of the memories within the PSD4135G2/G2V can reside in either space or both spaces. This is controlled through manipulation of the VM register that resides in the PSD's CSIOP space.

The VM register is set using PSDsoft to have an initial value. It can subsequently be changed by the microcontroller so that memory mapping can be changed on-the-fly. For example, you may wish to have SRAM and primary Flash in Data Space at boot, and secondary Flash memory in Program Space at boot, and later swap main and secondary Flash memory. This is easily done with the VM register by using PSDsoft to configure it for boot up and having the microcontroller change it when desired.

Table 18 describes the VM register.

7.3.2 Configuration modes for MCUs with separate program and data spaces

Separate space modes

Code memory space is separated from data memory space. For example, the $\overline{PSEN}$ signal is used to access the program code from the primary Flash memory, while the $\overline{RD}$ signal is used to access data from the secondary Flash memory, SRAM and I/O Ports.

This configuration requires the VM register to be set to 0Ch.

Combined space modes

The program and data memory spaces are combined into one space that allows the main Flash memory, secondary Flash memory, and SRAM to be accessed by either $\overline{PSEN}$ or $\overline{RD}$. For example, to configure the primary Flash memory in combined space mode, bits 2 and 4 of the VM register are set to "1".

80C51XA memory map example

See Application Notes for examples.

Figure 9. 80C51XA memory modules - separate space

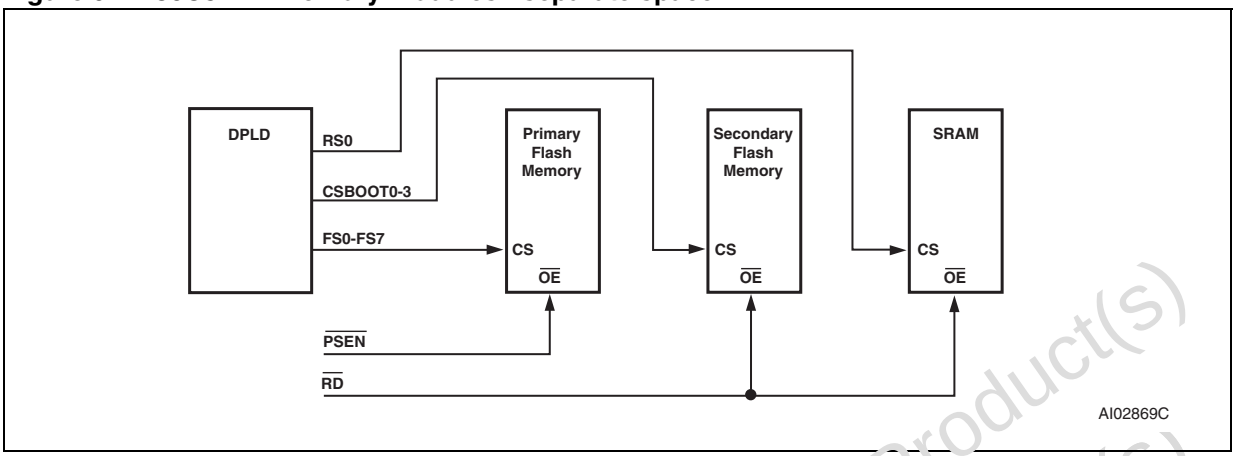
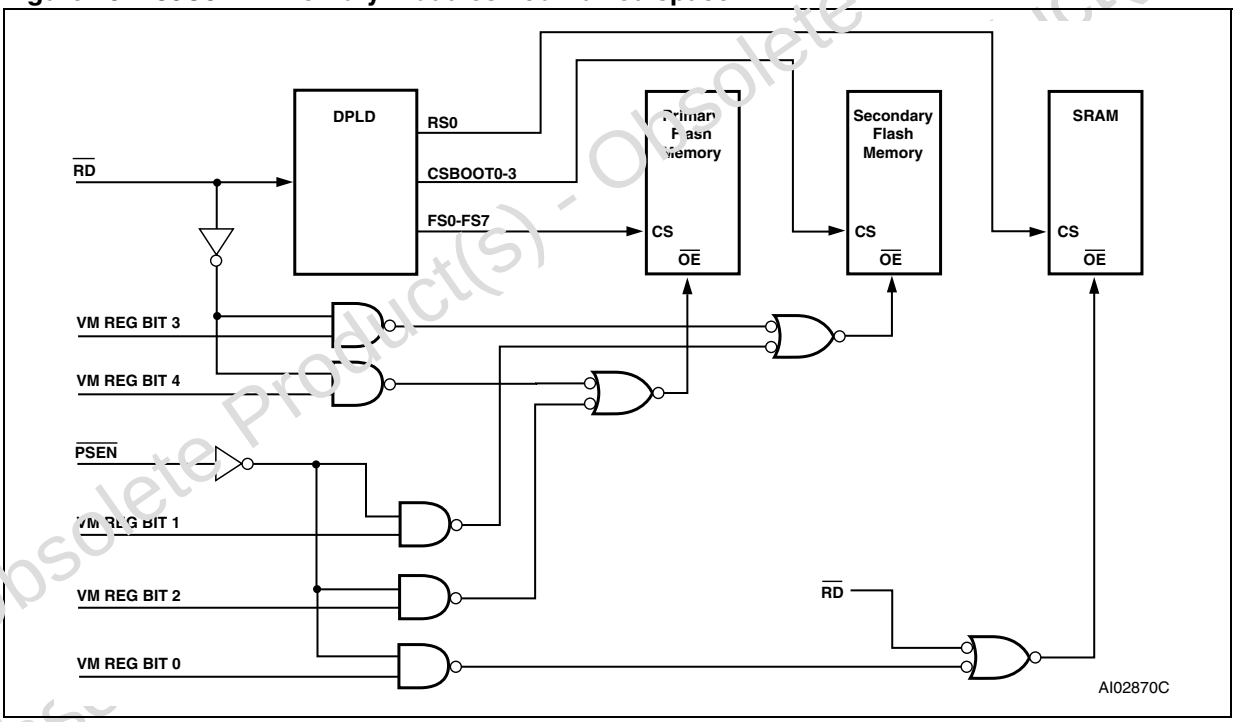


Figure 10. 80C51XA memory modules - combined space

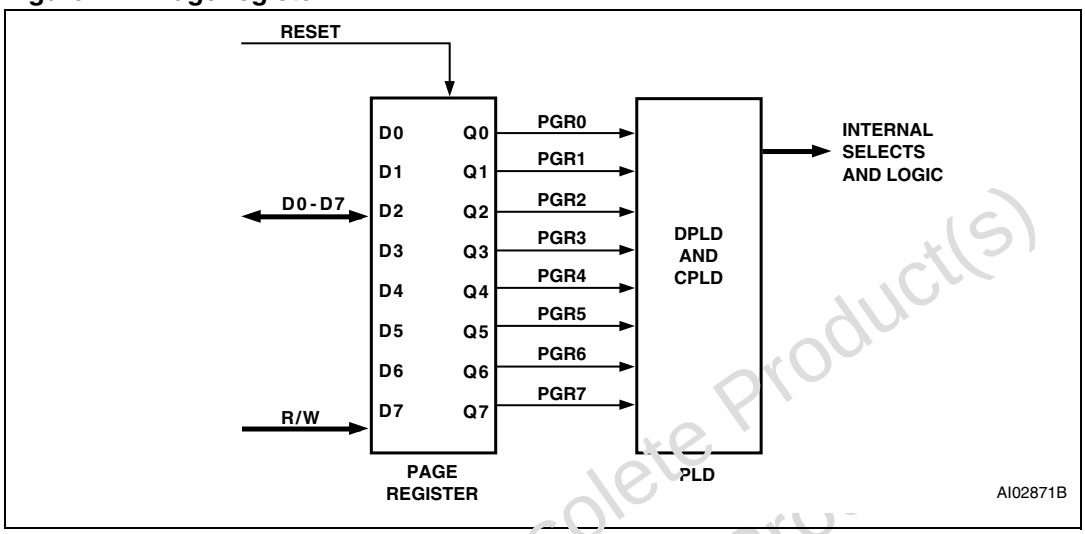


7.4 Page register

The eight bit Page Register increases the addressing capability of the microcontroller by a factor of up to 256. The contents of the register can also be read by the microcontroller. The outputs of the Page Register (PGR0-PGR7) are inputs to the PLD decoder and can be included in the Flash memory, secondary Flash memory, and SRAM chip select equations.

If memory paging is not needed, or if not all 8 page register bits are needed for memory paging, then these bits may be used in the PLD for general logic. See Application Notes. *Figure 11* shows the Page Register. The eight flip flops in the register are connected to the internal data bus. The microcontroller can write to or read from the Page Register. The Page Register can be accessed at address location CSIOP + E0h.

Figure 11. Page register



7.5 Memory ID registers

The 8-bit read only memory status registers are included in the CSIOP space. The user can determine the memory configuration of the PSD device by reading the Memory ID0 and Memory ID1 registers. The content of the registers is defined as shown in *Table 19* and *Table 20*.

8 PLDs

The PLDs bring programmable logic functionality to the PSD4135G2/G2V. After specifying the logic for the PLDs in PSDsoft, the logic is programmed into the device and available upon power-up.

The PSD4135G2 and PSD4135G2V contain two PLDs: the Decode PLD (DPLD), and the general purpose PLD (GPLD). The PLDs are briefly discussed in the next few paragraphs, and in more detail in *Section 8.1: Decode PLD (DPLD)* and *Section 8.2: General purpose PLD (GPLD)*. *Figure 11* shows the configuration of the PLDs.

The DPLD performs address decoding for internal components, such as memory, registers, and I/O port selects.

The GPLD can be used to generate external chip selects, control signals or logic functions. The GPLD has 24 outputs that are connected to Port A, B and C.

The AND array is used to form product terms. These product terms are specified using PSDsoft. An input bus consisting of 66 signals is connected to the PLDs. The signals are shown in *Table 25*. The complement of the 66 signals are also available as inputs to the AND array.

PSD Turbo bit

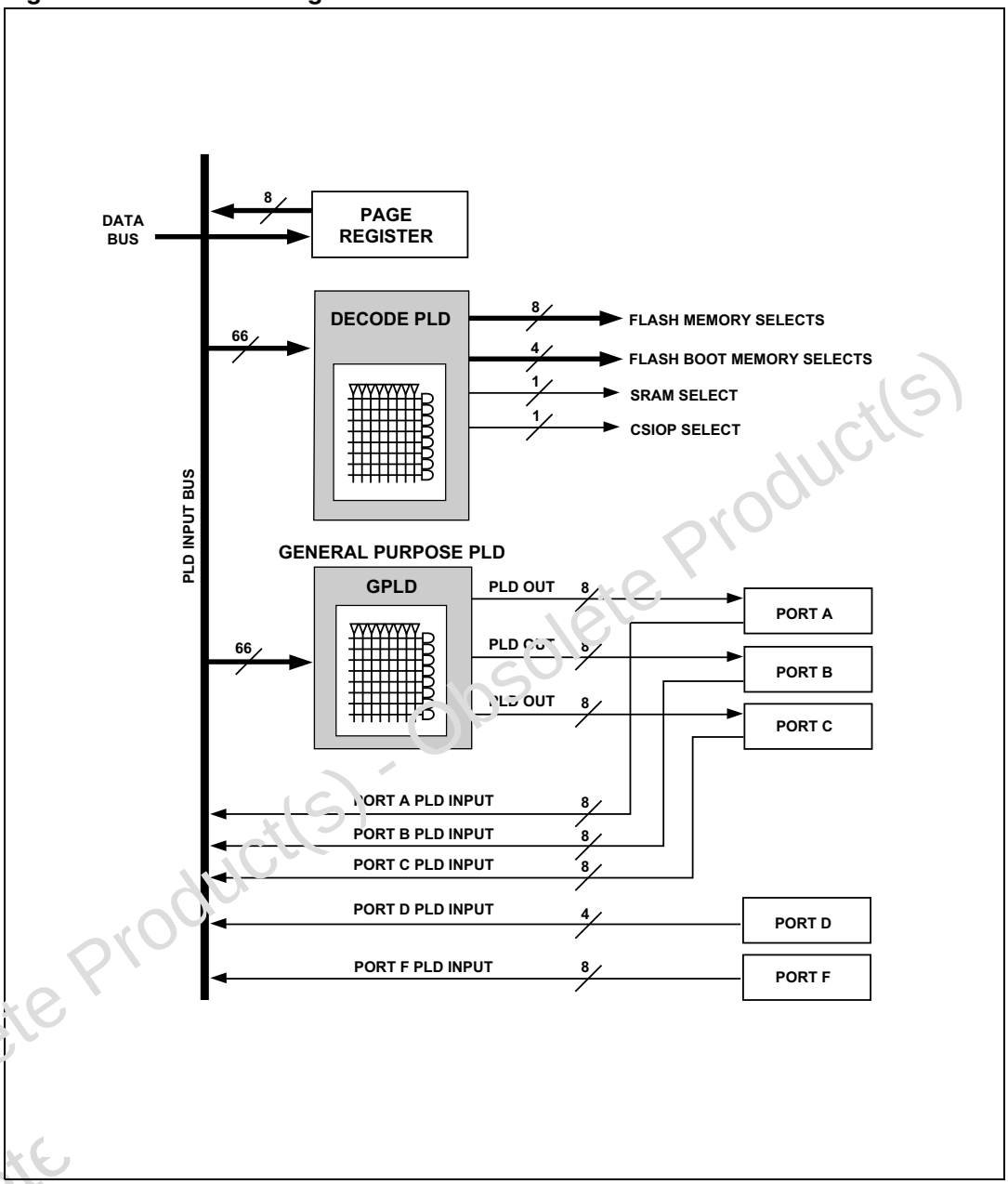
The PLDs in the PSD4135G2/G2V can minimize power consumption by switching to standby when inputs remain unchanged for an extended time of about 70 ns. Setting the Turbo mode bit to off (Bit 3 of the PMMR0 register) automatically places the PLDs into standby if no inputs are changing. Turbo-off mode increases propagation delays while reducing power consumption. Refer to the *Section 3.9: Power management unit (PMU)* on how to set the Turbo Bit. Additionally, five bits are available in the PMMR2 register to block MCU control signals from entering the PLDs. This reduces power consumption and can be used only when these MCU control signals are not used in PLD logic equations.

Table 25. DPLD and GPLD inputs

Input source	Input name	Number of signals
MCU address bus(1)	A15-A0	16
MCU control signals	CNTL0-CNTL2	3
Reset	$\overline{\text{RST}}$	1
Power-down	PDN	1
Port A input macrocells	PA7-PA0	8
Port B input macrocells	PB7-PB0	8
Port C input macrocells	PC7-PC0	8
Port D inputs	PD3-PD0	4
Port F inputs	PF7-PF0	8
Page register	PGR7-PGR0	8
Flash memory Program Status bit	Ready/$\overline{\text{Busy}}$	1

1. The address inputs are A19-A4 in 80C51XA mode.

Figure 12. PLD block diagram



8.1 Decode PLD (DPLD)

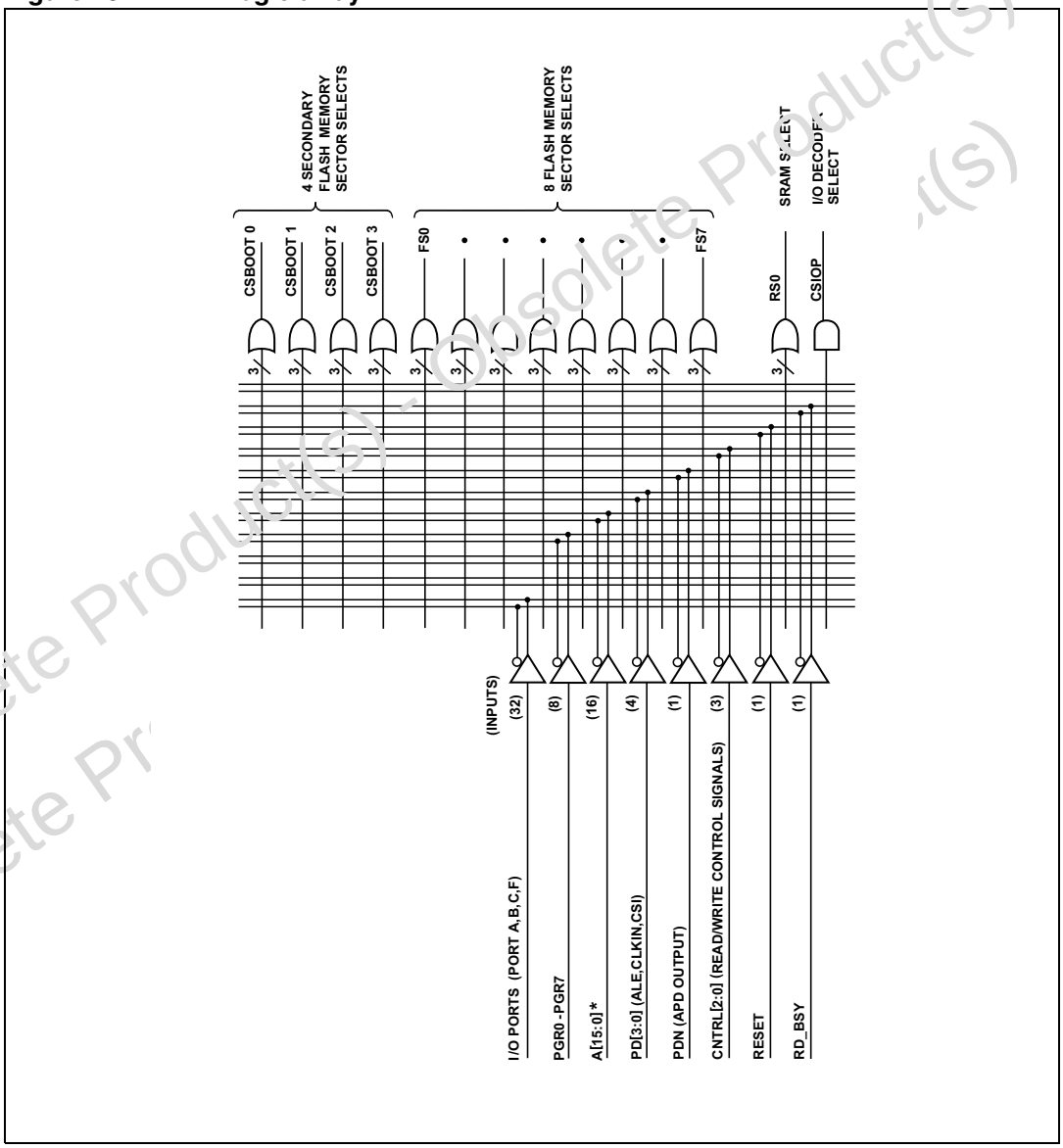
The DPLD, shown in *Figure 11*, is used for decoding the address for internal components.

The DPLD can generate the following decode signals:

- 8 sector selects for the primary Flash memory (three product terms each)
- 4 sector selects for the secondary Flash memory (three product terms each)
- 1 internal SRAM select (three product terms)
- 1 internal CSIOP select (select PSD registers, one product term)

Inputs to the DPLD chip selects may include address inputs, Page Register inputs and other user defined external inputs from Ports A, B, C, D or F.

Figure 13. DPLD logic array



1. *The address inputs are A[19:4] in 80C51XA mode.
2. Additional address lines can be brought into PSD via Port A, B, C, C or F.

8.2 General purpose PLD (GPLD)

The general purpose PLD implements user defined system combinatorial logic function or chip selects for external devices. *Figure 14* shows how the GPLD is connected to the I/O Ports. The GPLD has 24 outputs and each are routed to a port pin. The port pin can also be configured as input to the GPLD. When it is not used as GPLD output or input, the pin can be configured to perform other I/O functions.

All GPLD outputs are identical except in the number of available product terms (PTs) for logic implementation. Select the pin that can best meet the PT requirement of your logic function or chip select. In general, a PT is consumed for each logic “OR” function that you specify in PSDsoft. However, certain logic functions can consume more than one PT even if no logic “OR” is specified (such as specifying an address range with boundaries of high granularity).

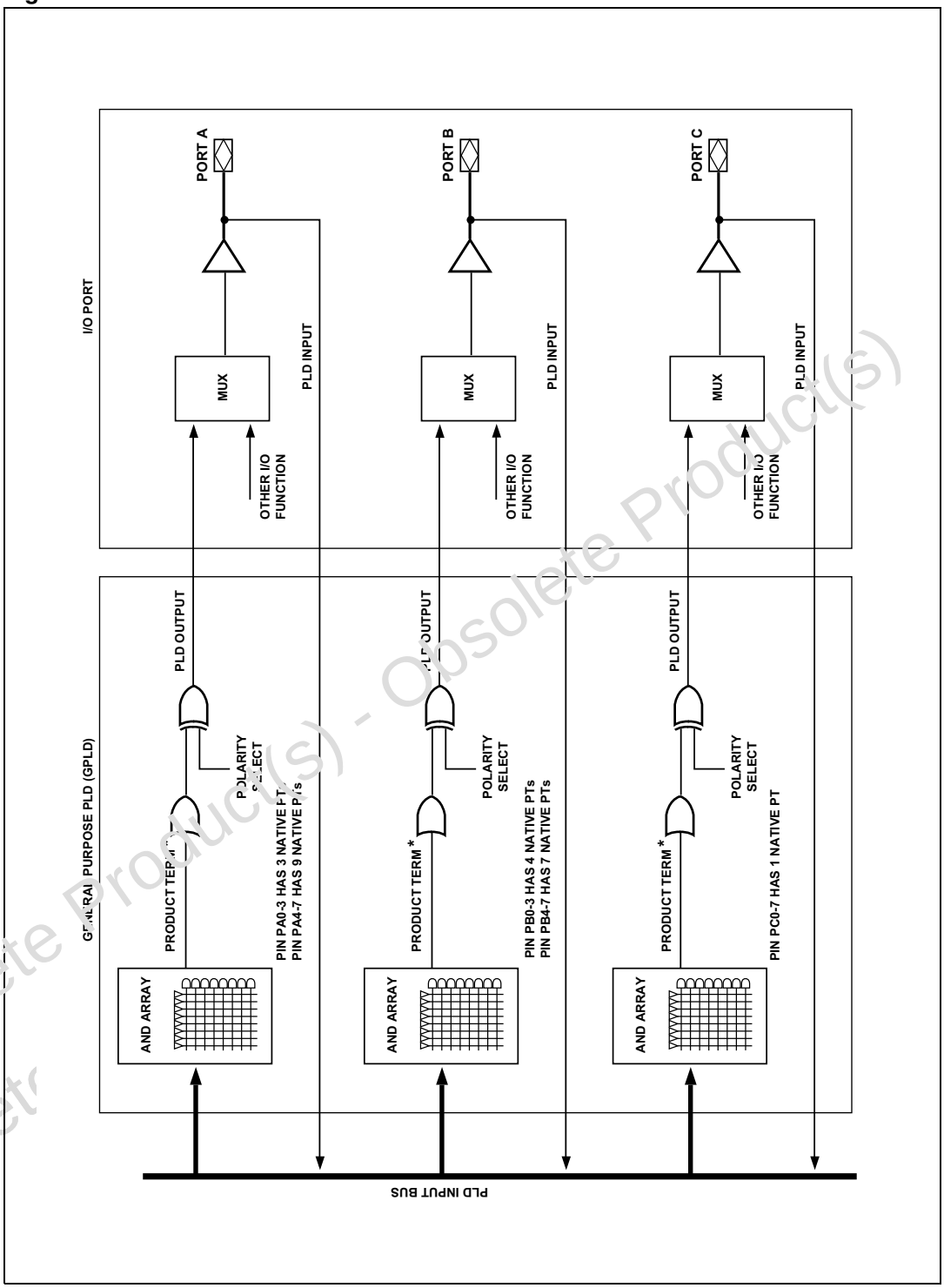
Table 26 shows the number of “native” PTs for each GPLD output pin. A native PT means that a particular PT is dedicated to an output pin. For example, *Table 26* shows that PSD Port A pin PA0 has 3 native product terms. This means a guaranteed minimum of 3 PTs is available to implement logic for that pin.

PSD silicon and PSDsoft can include additional PTs beyond the native PTs to implement logic. This is a transparent operation that occurs as needed through PT expansion (internal feedback) or PT allocation (internal borrowing). You may notice in the fitter report generated by PSDsoft that for a given GPLD output pin, more PTs were used to implement logic than the number of native PTs available for that pin. This is because PSDsoft has called on unused PTs from other GPLD output pins to make your logic design fit (PT allocation or PT expansion). For optimum results, choose a GPLD output pin with a large number of native PTs for complicated logic.

Table 26. GPLD Product Term Availability

GPLD output on port pin	Number of native product terms
Port A, pins PA0-3	3
Port A, pins PA4-7	9
Port B, pins PB0-3 4	4
Port B, pins PB4-7 7	7
Port C, pins PC0-7	1

Figure 14. The MicroCell and I/O Port



9 MCU bus interface

The “no-glue logic” PSD4135G2/G2V microcontroller bus interface can be directly connected to most popular microcontrollers and their control signals. Key 16-bit microcontrollers with their bus types and control signals are shown in *Table 27*. The MCU interface type is specified using the PSDsoft.

Table 27. MCUs and their control signals

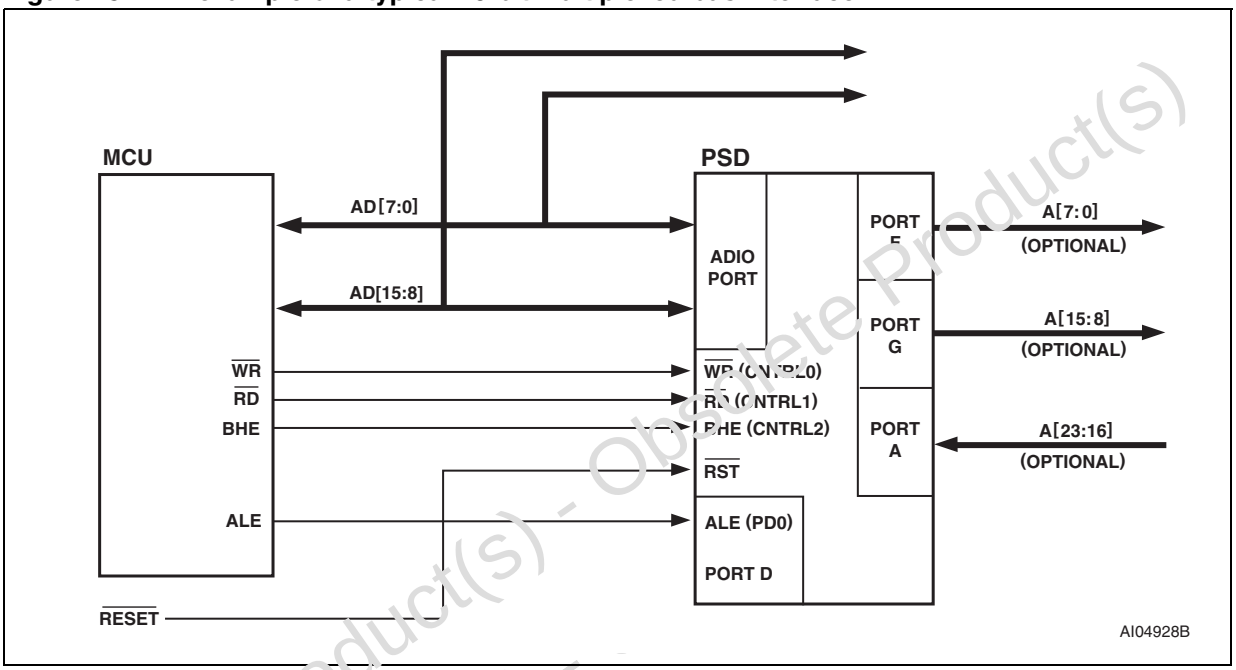
MCU	CNTL0	CNTL1	CNTL2	PD3	PD0(1)	ADIO0	PF3-PF0
68302, 68306, MMC2001	R/$\overline{W}$	$\overline{LDS}$	$\overline{UDS}$	(2)	AS	—	(2)
68330, 68331, 68332, 68340	R/$\overline{W}$	$\overline{DS}$	SIZ0	(2)	AS	A0	(2)
68LC302, MMC2001	$\overline{WEL}$	$\overline{OE}$	—	$\overline{WEH}$	AS	—	(2)
68HC16	R/$\overline{W}$	$\overline{DS}$	SIZ0	(2)	AS	A0	(2)
68HC912	R/$\overline{W}$	E	$\overline{LSTRB}$	$\overline{DBE}$	E	A0	(2)
68HC812(3)	R/$\overline{W}$	E	$\overline{LSTRB}$	(2)	(2)	A0	(2)
80196	$\overline{WR}$	$\overline{RD}$	BHE	(2)	ALE	A0	(2)
80196SP	$\overline{WRL}$	$\overline{RD}$	(2)	$\overline{WRH}$	ALE	A0	(2)
80186	$\overline{WR}$	$\overline{RD}$	$\overline{BHE}$	(2)	ALE	A0	(2)
80C161, 80C164-80C167	$\overline{WR}$	$\overline{RD}$	$\overline{BHE}$	(2)	ALE	A0	(2)
80C51XA	$\overline{WRL}$	$\overline{RD}$	$\overline{PSEN}$	$\overline{WRH}$	ALE	A4/D0	A3-A1
H8/300	$\overline{WRL}$	$\overline{RD}$	(2)	$\overline{WRH}$	AS	A0	—
M37702M2	R/$\overline{W}$	E	$\overline{BHE}$	(2)	ALE	A0	(2)

1. ALE/AS input is optional for MCUs with a non-multiplexed bus
2. Unused CNTL2 pin can be configured as PLD input. Other unused pins (PD3-PD0, PF3-PF0) can be configured for other I/O functions.
3. This configuration is for 68C812A4_EC at 5MHz, 3V only.

9.1 PSD interface to a multiplexed bus

Figure 19 shows an example of a system using a microcontroller with a 16-bit multiplexed bus and a PSD4135G2/G2V. The ADIO port on the PSD4135G2/G2V is connected directly to the microcontroller address/data bus. ALE latches the address lines internally. Latched addresses can be brought out to Port E, F or G. The PSD4135G2 and PSD4135G2V drive the ADIO data bus only when one of its internal resources is accessed and the $\overline{RD}$ input is active. Should the system address bus exceed sixteen bits, Ports A, B, C, or F may be used as additional address inputs.

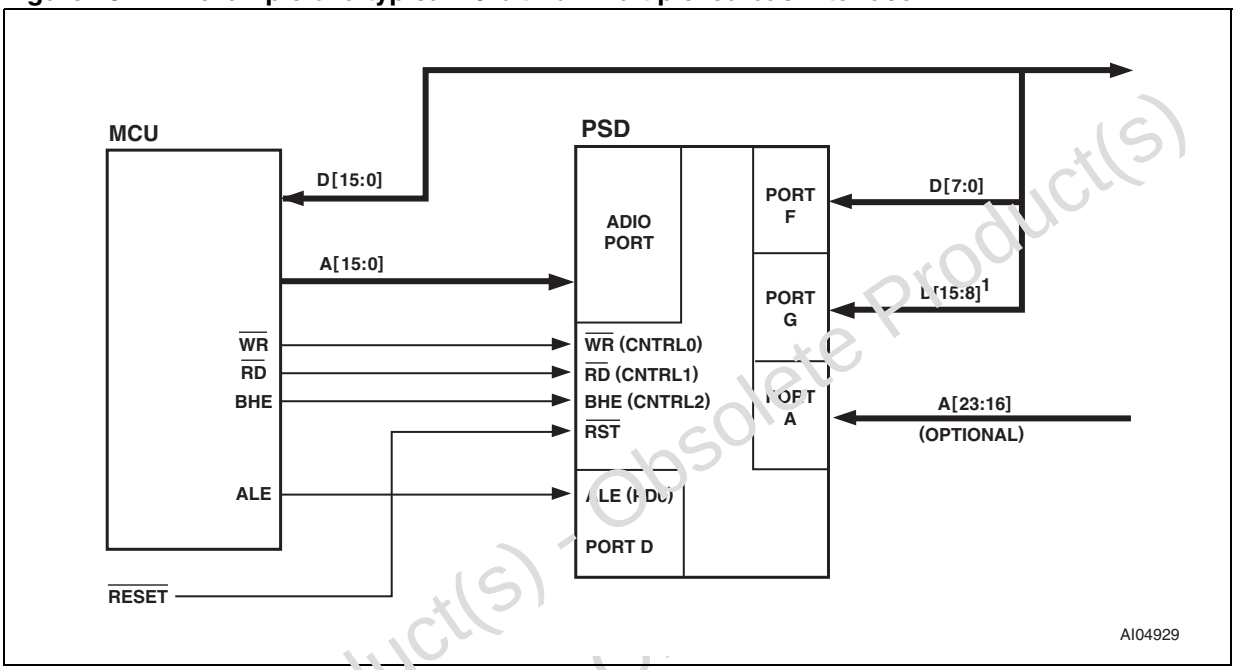
Figure 15. An example of a typical 16-bit multiplexed bus interface



9.2 PSD interface to a non-multiplexed bus

Figure 20: Interfacing a PSD4135G2 with a H83/2350 shows an example of a system using a microcontroller with a 16-bit non-multiplexed bus and a PSD4135G2/G2V. The address bus is connected to the ADIO Port, and the data bus is connected to Port F and G. Port F and G are in tri-state mode when the PSD4135G2G2V is not accessed by the microcontroller. Should the system address bus exceed sixteen bits, Ports A, B or C may be used for additional address inputs.

Figure 16. An example of a typical 16-bit non-multiplexed bus interface



9.3 Data Byte Enable reference

Microcontrollers have different data byte orientations. The following tables show how the PSD4135G2/G2V interprets byte/word operation in different bus write configurations. Even-byte refers to locations with address A0 equal to zero and odd byte as locations with A0 equal to one.

9.4 MCU interface examples

Figure 17, *Figure 18*, *Figure 19*, and *Figure 20* show examples of the basic connections between the PSD4135G2/G2V and some popular microcontrollers. The PSD4135G2 Control input pins are labeled as the microcontroller function for which they are configured. The MCU interface is specified using PSDsoft.

9.4.1 80C196 and 80C186

In *Figure 17*, the Intel 80C196 microcontroller, which has a multiplexed sixteen-bit bus, is shown connected to a PSD4135G2. The $\overline{WR}$ and $\overline{RD}$ signals are connected to the CNTL0-1 pins. The BHE signal is used for high data byte selection. If BHE is not used, the PSD can be configured to receive the $\overline{WRL}$ and $\overline{WRH}$ from the MCU. Higher address inputs (A16-A19) can be routed to Port A, B or C as inputs to the PLD.

The AMD 80186 family has the same bus connection to the PSD as the 80C196, MC683XX and 68HC16

Figure 18 shows a Motorola MC68331 with non-multiplexed sixteen-bit data bus and 24-bit address bus. The data bus from the MC68331 is connected to Port F (D0-7) and Port G (D8-D15). The SIZ0 and A0 inputs determine the high/low byte selection. The R/$\overline{W}$, $\overline{DS}$ and SIZ0 are connected to the CNTL0-2 pins. The 68HC16 and other members of the 683XX family have the same connection as the 68331 shown in *Figure 18*.

Table 28. 16-bit data bus with $\overline{BHE}$

$\overline{BHE}$	A0	D15-D8	D7-D0
0	0	Odd Byte	Even Byte
0	1	Odd Byte	—
1	0	—	Even Byte

Table 29. 16-bit data bus with $\overline{WRH}$ and $\overline{WRL}$

$\overline{WRH}$	$\overline{WRL}$	D15-D8	D7-D0
0	0	Odd Byte	Even Byte
0	1	Odd Byte	—
1	0	—	Even Byte

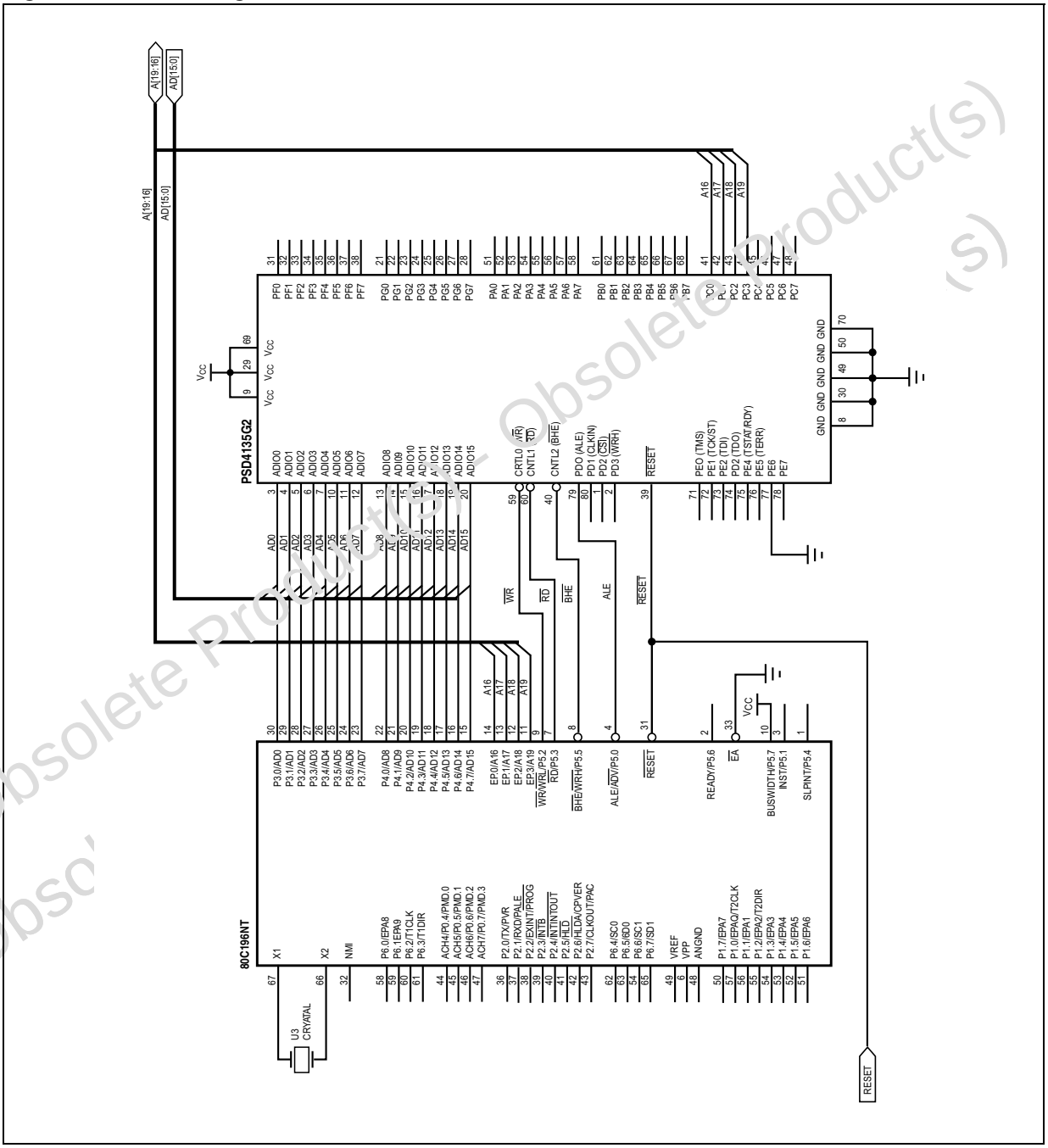
Table 30. 16-bit data bus with SIZ0, A0 (Motorola MCU)

SIZ0	A0	D15-D8	D7-D0
0	0	Even Byte	Odd Byte
1	0	Even Byte	—
1	1	—	Odd Byte

Table 31. 16-bit data bus with $\overline{LDS}$, $\overline{UDS}$ (Motorola MCU)

$\overline{LDS}$	$\overline{UDS}$	D15-D8	D7-D0
0	0	Even Byte	Odd Byte
1	0	Even Byte	—
0	1	—	Odd Byte

Figure 17. Interfacing the PSD4135G2 with an 80C196

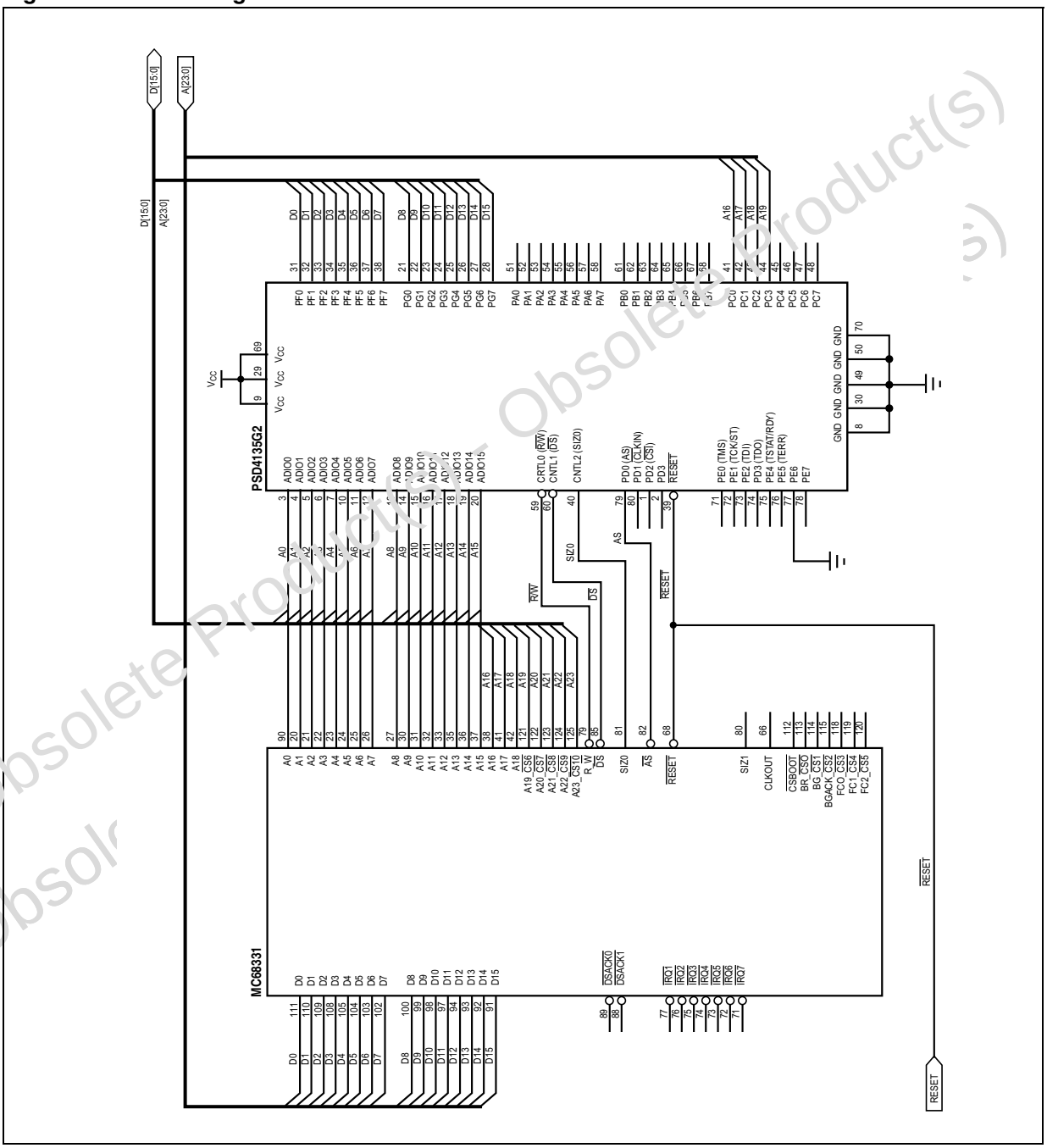


9.4.2 MC683XX and 68HC16

Figure 18 shows a Motorola MC68331 with non-multiplexed sixteen-bit data bus and 24-bit address bus. The data bus from the MC68331 is connected to Port F (D0-7) and Port G (D8-D15). The SIZ0 and A0 inputs determine the high/low byte selection. The R/$\overline{W}$, $\overline{DS}$ and SIZ0 are connected to the CNTL0-2 pins.

The 68HC16 and other members of the 683XX family have the same connection as the 68331 shown in *Figure 18*.

Figure 18. Interfacing the PSD with an MC68331



9.4.3 80C51XA

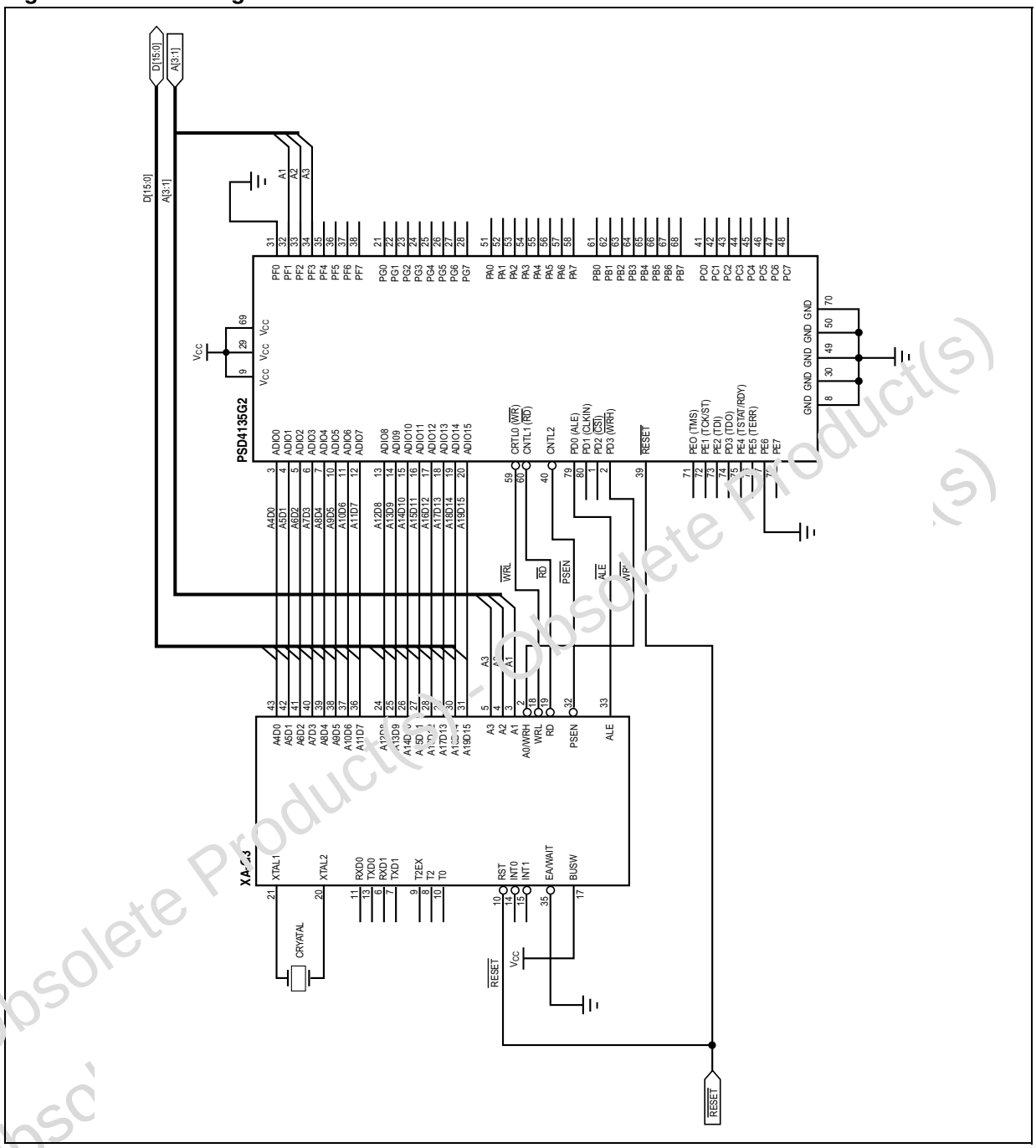
The Philips 80C51XA microcontroller has a 16-bit multiplexed bus with burst cycles.

Address bits A[3:1] are not multiplexed while A[19:4] are multiplexed with data bits D[15:0].

The PSD4135G2 supports the 80C51XA burst mode. The $\overline{WRH}$ signal is connected to the PD3 and the $\overline{WRL}$ is connected to CNTL0 pin. The $\overline{RD}$ and $\overline{PSEN}$ signal is connected to CNTL1-2 pins. *Figure 19* shows the XA schematic.

The 80C51XA improves bus throughput and performance by issuing Burst cycles to fetch codes from memory. In Burst cycles, addresses A19-4 are latched internally by the PSD, while the 80C51XA drives the A3-1 lines to sequentially fetch up to 16 bytes of code. The PSD access time is then measured from address A3-A1 valid to data in valid. The PSD bus timing requirement in Burst cycle is identical to the normal bus cycle except the address set up or hold time with respect to ALE is not required.

Figure 19. Interfacing the PSD with an 80C51XA-G3

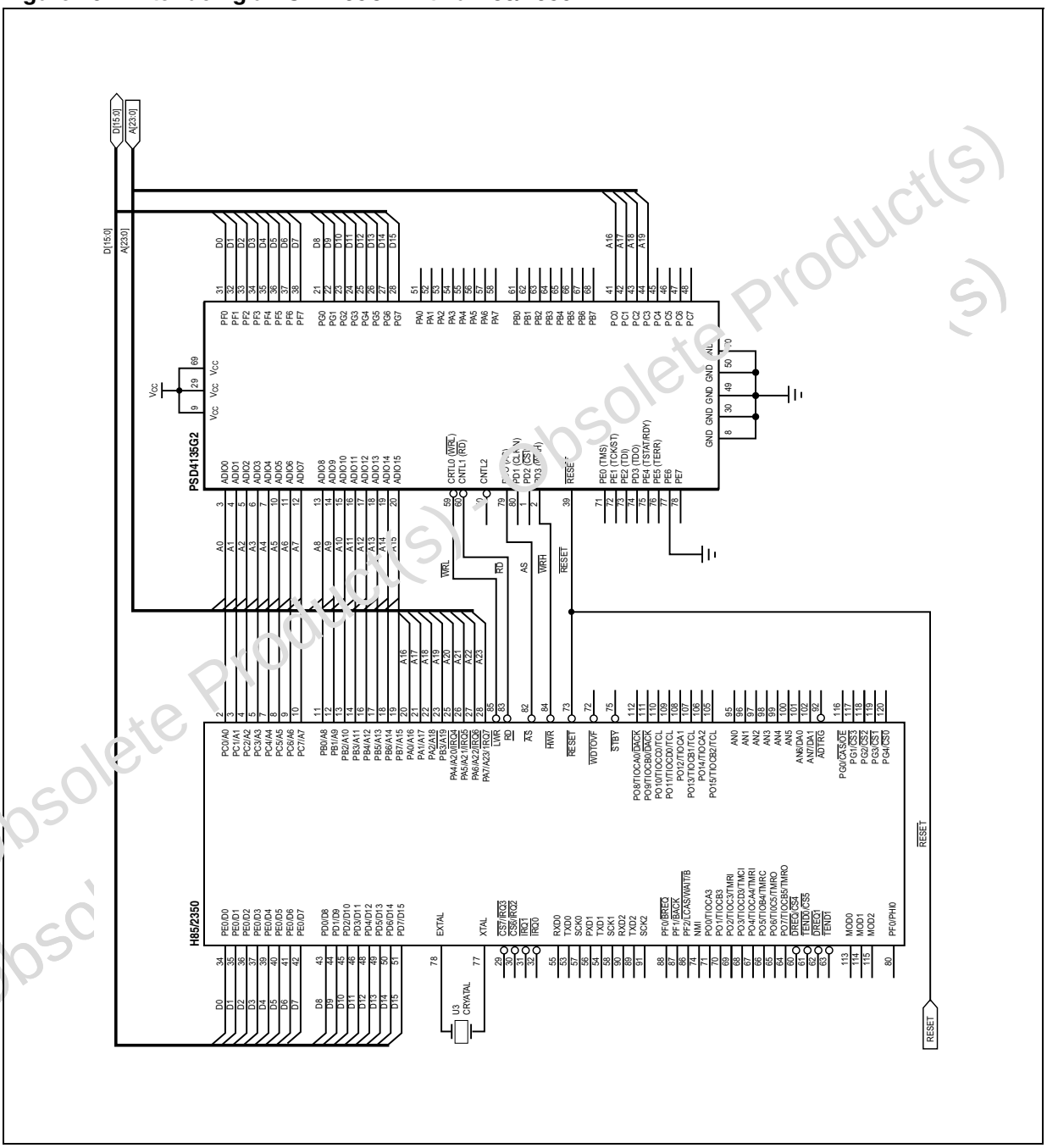


9.4.4 H8/300

Figure 20 shows a Hitachi H8/2350 with non-multiplexed sixteen-bit data bus and 24-bit address bus. The H8 data bus is connected to Port F (D0-7) and Port G (D8-15).

The $\overline{WRL}$, $\overline{WRH}$ and $\overline{RD}$ signals are connected to the CNTL0, PD3 and CNTL1 pins respectively. The AS connection is optional and is required if the address are to be latched.

Figure 20. Interfacing a PSD4135G2 with a H83/2350



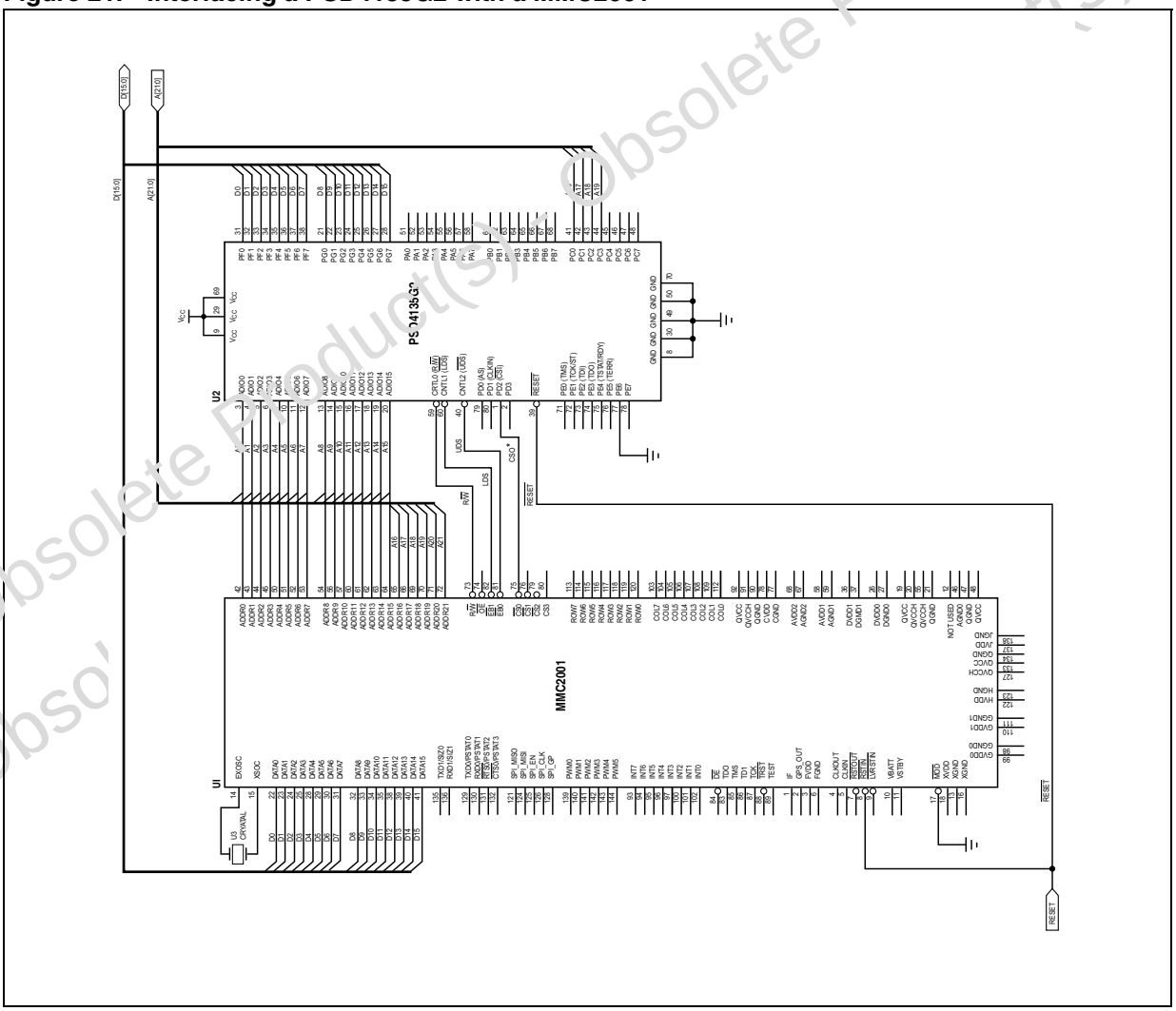
9.4.5 MMC2001

The Motorola MCORE MMC2001 microcontroller has a MOD input pin that selects internal or external boot ROM. The PSD4135G2 can be configured as the external Flash boot ROM or as extension to the internal ROM.

The MMC2001 has a 16-bit external data bus and 20 address lines with external Chip Select signals. The Chip Select Control Registers allow the user to customize the bus interface and timing to fit the individual system requirement. A typical interface configuration to the PSD4135G2 is shown in *Figure 21*. The MMC2001's R/$\overline{W}$ signal is connected to the cntl0 pin, while EB0 and EB1 (enable byte0 and byte1) are connected to the cntl1 ($\overline{UDS}$) and cntl2 ($\overline{LDS}$) pins. The WEN bit in the Chip Select Control Register should set to 1 to terminate the EB[0:1] earlier to provide the write data hold time for the PSD. The WSC and WWS bits in the Control Register are set to wait states that meet the PSD access time requirement.

Another option is to configure the EB0 and EB1 as $\overline{WRL}$ and $\overline{WRH}$ signals. In this case the PSD4135G2 control setting will be: $\overline{OE}$, $\overline{WRL}$, $\overline{WRH}$ where $\overline{OE}$ is the read signal from the MMC2001.

Figure 21. Interfacing a PSD4135G2 with a MMC2001

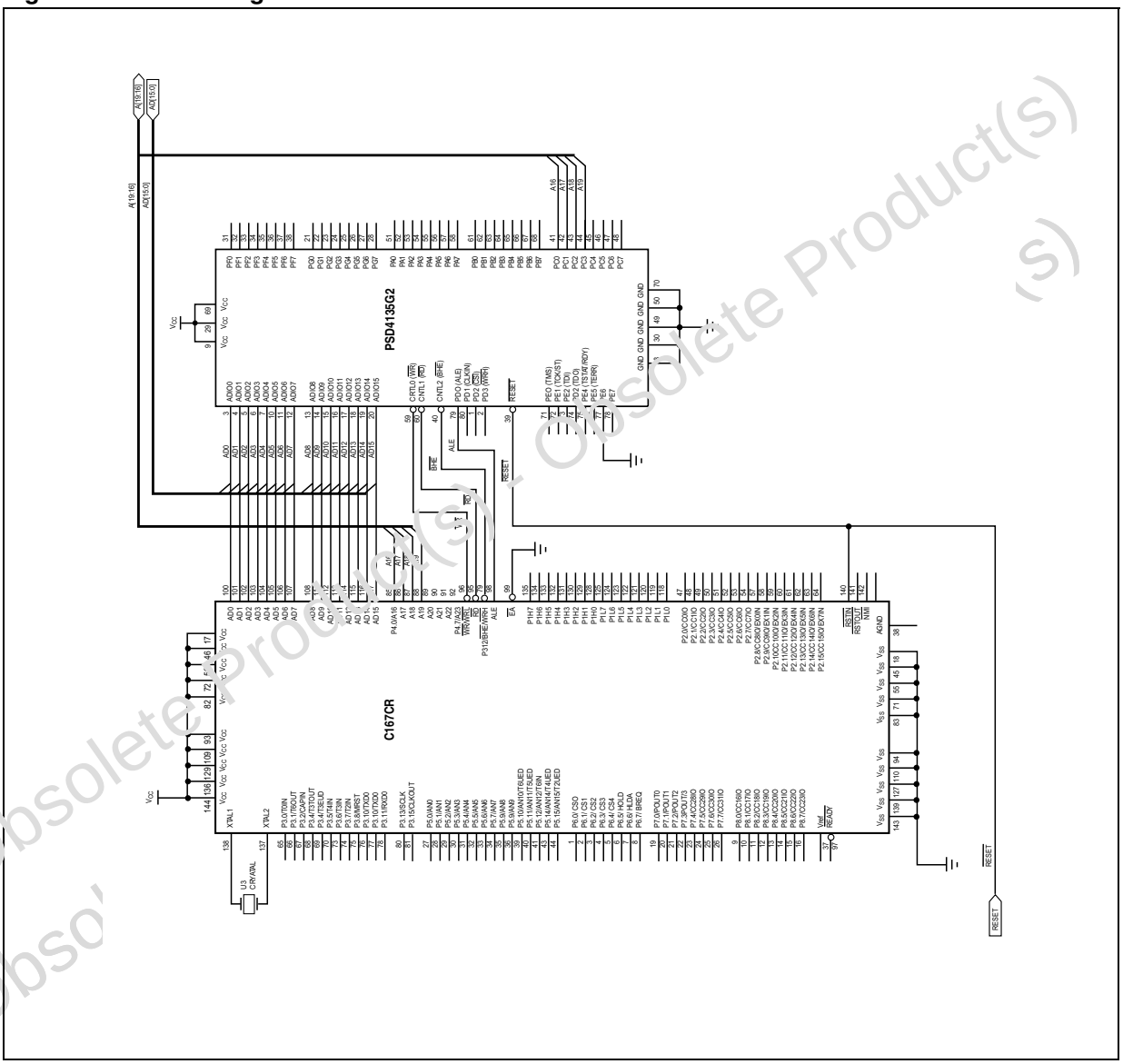


9.4.6 C16X family

The PSD4135G2 supports Infineon's C16X family of microcontrollers (C161-C167) in both the multiplexed and non-multiplexed bus configuration. In *Figure 22* the C167CR is shown connected to the PSD4135G2 in a multiplexed bus configuration. The control signals from the MCU are $\overline{WR}$, $\overline{RD}$, BHE and ALE and are routed to the corresponding PSD pins.

The C167 has another control signal setting ($\overline{RD}$, $\overline{WRL}$, $\overline{WRH}$, ALE) which is also supported by the PSD4135G2.

Figure 22. Interfacing a PSD4135G2 with a C167R



10 I/O ports

There are seven programmable I/O ports: Ports A, B, C, D, E, F and G. Each of the ports is eight bits except Port D, which is 4 bits. Each port pin is individually user configurable, thus allowing multiple functions per port. The ports are configured using PSDsoft or by the microcontroller writing to on-chip registers in the CSIOP address space.

The topics discussed in this section are:

- General Port Architecture
- Port operating modes
- Port Configuration Registers
- Port Data Registers
- Individual Port Functionality

10.1 General port architecture

The general architecture of the I/O Port is shown in *Figure 23*. Individual Port architectures are shown in *Figure 24*, *Figure 25*, and *Figure 26*. In general, once the purpose for a port pin has been defined, that pin will no longer be available for other purposes. Exceptions will be noted. As shown in *Figure 23*, the ports contain an output multiplexer whose selects are driven by the configuration bits in the Control Registers (Ports E, F and G only) and PSDsoft Configuration. Inputs to the multiplexer include the following:

- Output data from the Data Out Register
- Latched address outputs
- GPLD outputs (External Chip Selects)

The Port Data Buffer (PDB) is a tri-state buffer that allows only one source at a time to be read. The PDB is connected to the Internal Data Bus for feedback and can be read by the microcontroller. The Data Out and MicroCell outputs, Direction and Control Registers, and port pin input are all connected to the PDB.

The contents of these registers can be altered by the microcontroller. The PDB feedback path allows the microcontroller to check the contents of the registers.

10.2 Port operating modes

The I/O Ports have several modes of operation. Some modes can be defined using PSDsoft, some by the microcontroller writing to the Registers in CSIOP space, and some by both. The modes that can only be defined using PSDsoft must be programmed into the device and cannot be changed unless the device is reprogrammed. The modes that can be changed by the microcontroller can be done so dynamically at run-time. The PLD I/O, Data Port, Address input, and MCU Reset modes are the only modes that must be defined before programming the device. All other modes can be changed by the microcontroller at run-time.

Table 32 summarizes which modes are available on each port. *Table 35* shows how and where the different modes are configured. Each of the port operating modes are described in the following subsections.

Figure 23. General I/O port architecture

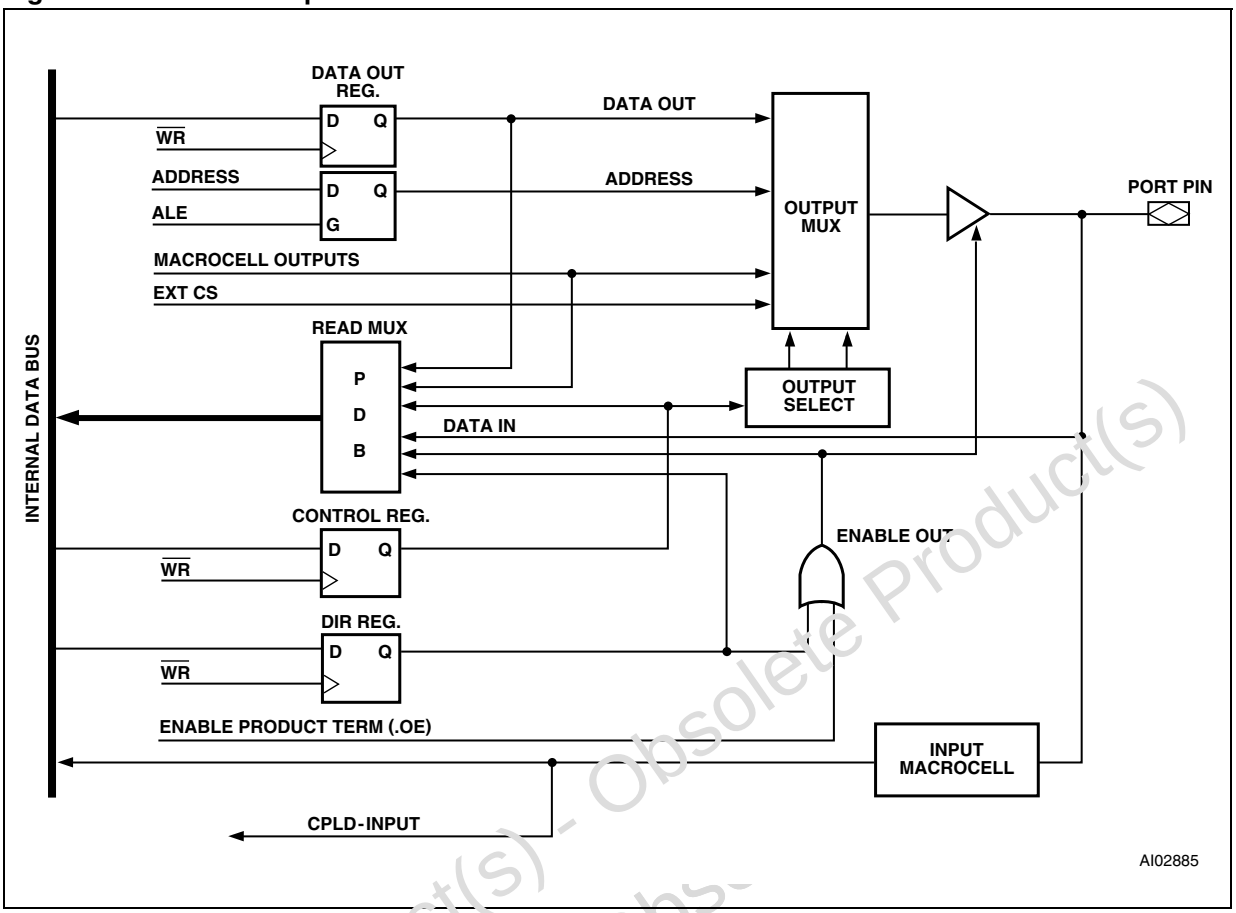


Table 32. Port operating modes

Port mode	Port A	Port B	Port C	Port D	Port E	Port F	Port G
MCU I/O	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PLD outputs	Yes	Yes	Yes	No	No	No	No
PLD inputs	Yes	Yes	Yes	Yes	No	Yes	No
Address Out	No	No	No	No	Yes (A7 - 0)	Yes (A7 - 0)	Yes (A7 - 0) or (A15 - 8)
Address In	Yes	Yes	Yes	Yes	No	Yes	No
Data Port	No	No	No	No	No	Yes	Yes
JTAG ISP	No	No	No	No	Yes	No	No
MCU Reset mode(1)	No	No	No	No	No	Yes	Yes

1. Available to Motorola 16-bit 683xx and HC16 families of MCUs.

Table 33. Port operating mode settings(1)

Mode	Defined in PSDsoft Express	Control register setting	Direction register setting	VM register setting
MCU I/O	Declare pins only	0(2)	1 = output, 0 = input	N/A
PLD I/O	Declare pins and Logic equations	N/A		N/A
Data Port (Port F, G)	Selected for MCU with non-multiplexed bus	N/A	N/A	N/A
Address Out (Port E, F, G)	Declare pins only	1	1	N/A
Address In (Port A, B, C, D, F)	Declare pins	N/A	N/A	N/A
JTAG ISP	Declare pins only	N/A	N/A	N/A
MCU Reset mode	Specific pin logic level	N/A	N/A	N/A

1. N/A = Not Applicable
2. Control register setting is not applicable to Ports A, B and C.

10.2.1 MCU I/O mode

In the MCU I/O mode, the microcontroller uses the PSD4135G2/G2V ports to expand its own I/O ports. By setting up the CSIOP space, the ports on the PSD4135G2/G2V are mapped into the microcontroller address space. The addresses of the ports are listed in *Table 6*.

A port pin can be put into MCU I/O mode by writing a '0' to the corresponding bit in the Control Register (Port E, F and G). The MCU I/O direction may be changed by writing to the corresponding bit in the Direction Register (see *Section 10.3.2: Direction register*). When the pin is configured as an output, the content of the Data Out Register drives the pin. When configured as an input, the microcontroller can read the port input through the Data In buffer (see *Figure 23*).

Ports A, B and C do not have Control Registers, and are in MCU I/O mode by default. They can be used for PLD I/O if they are specified in PSDsoft.

10.2.2 PLD I/O mode

The PLD I/O mode uses a port as an input to the GPLD's input microcells, and/or as an output from the GPLD. The corresponding bit in the Direction Register must not be set to '1' if the pin is defined as a PLD input pin in PSDsoft. The PLD I/O mode is specified in PSDsoft by declaring the port pins, and then specifying an equation in PSDsoft.

10.2.3 Address In mode

For microcontrollers that have more than 16 address lines, the higher addresses can beconnected to Ports A, B, C, D or F and are routed as inputs to the PLDs. The address input can be latched by the address strobe (ALE/AS). Any input that is included in the DPLD equations for the primary Flash, Boot Flash, or SRAM is considered to be an address input.

10.2.4 Data Port mode

Port F and G can be used as a data bus port for a microcontroller with a non-multiplexed address/data bus. The Data Port is connected to the data bus of the microcontroller. The general I/O functions are disabled in Port F and G if the ports are configured as Data Port. Data Port mode is automatically configured in PSDsoft when a non-multiplexed bus MCU is selected.

10.2.5 JTAG ISP

Port E is JTAG compliant, and can be used for in-system programming (ISP).

10.2.6 MCU Reset mode

Port F and G can be configured to operate in “MCU Reset” mode. This mode is available when PSD is configured for the Motorola 16-bit 683XX and HC16 family and is active only during reset.

At the rising edge of the Reset input, the MCU reads the logic level on the Data Bus D15-0 pins. The MCU then configures some of its I/O pin functions according to the logic level input on the data bus lines. Two dedicated buffers are usually enabled during reset to drive the data bus lines to the desired logic level.

The PSD4135G2/G2V can replace the two buffers by configuring Port F and G to operate in MCU Reset mode. In this mode, the PSD will drive the pre-defined logic level or data pattern onto the MCU Data Bus when reset is active and there is no ongoing bus cycle.

After reset, Port F and G return to the normal Data Port mode.

The MCU Reset mode is enabled and configured in PSDsoft. The user defines the logic level (data pattern) that will be driven out from Port F and G during reset.

10.2.7 Address Out mode

For microcontrollers with a multiplexed address/data bus, Address Out mode can be used to drive latched addresses onto the port pins. These port pins can, in turn, drive external devices. Either the output enable or the corresponding bits of both the Direction Register and Control Register must be set to a ‘1’ for pins to use Address Out mode. This must be done by the MCU at run-time. See *Table 31* for the address output pin assignments on Ports E, F and F for various MCUs.

Note: Do not drive address lines with Address Out mode to an external memory device if it is intended for the MCU to boot from the external device. The MCU must first boot from PSD memory so the Direction and Control register bits can be set.

Table 34. I/O port latched address output assignments(1)

MCU	Port E (PE3-PE0)	Port E (PE7-PE4)	Port F (PF3-PF0)	Port F (PF7-PF4)	Port G (PG3-PG0)	Port G (PG7-PG4)
80C51XA	N/A	Address a7-a4	N/A	Address a7-a4	Address a11-a8	Address a15-a12
All other MCU with multiplexed bus	Address a3-a0	Address a7-a4	Address a3-a0	Address a7-a4	Address a11-a8	Address a15-a12

1. N/A = Not Applicable.

10.3 Port Configuration registers (PCRs)

Each port has a set of PCRs used for configuration. The contents of the registers can be accessed by the microcontroller through normal read/write bus cycles at the addresses given in *Table 6*. The addresses in *Table 6* are the offsets in hex from the base of the CSIOP register.

The pins of a port are individually configurable and each bit in the register controls its respective pin. For example, Bit 0 in a register refers to Bit 0 of its port. The three PCRs, shown in *Table 35*, are used for setting the port configurations. The default power-up state for each register in *Table 38* is 00h.

Table 35. Port Configuration registers (PCR)

Register name	Port	MCU access
Control	E, F, G	WRITE/READ
Direction	A, B, C, D, E, F, G	WRITE/READ
Drive Select(1)	A, B, C, D, E, F, G	WRITE/READ

1. See *Table 38* for Drive register bit definition.

10.3.1 Control register

Any bit set to '0' in the Control Register sets the corresponding Port pin to MCU I/O mode, and a '1' sets it to Address Out mode. The default mode is MCU I/O. Only Ports E, F and G have an associated Control Register.

10.3.2 Direction register

The Direction Register controls the direction of data flow in the I/O Ports. Any bit set to '1' in the Direction Register will cause the corresponding pin to be an output, and any bit set to '0' will cause it to be an input. The default mode for all port pins is input.

Figure 24, *Figure 25*, and *Figure 26* show the Port Architecture diagrams for Ports A/B/C and E/F/G respectively. The direction of data flow for Ports A, B, C and F are controlled by the direction register.

An example of a configuration for a port with the three least significant bits set to output and the remainder set to input is shown in *Table 37*. Since Port D only contains four pins, the Direction Register for Port D has only the four least significant bits active.

Table 36. Port Pin Direction Control

Direction register bit	Port pin mode
0	Input
1	Output

Table 37. Port direction assignment example

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	1	1	1

10.3.3 Drive select register

The Drive Select Register configures the pin driver as Open Drain or CMOS for some port pins, and controls the slew rate for the other port pins. An external pull-up resistor should be used for pins configured as Open Drain.

A pin can be configured as Open Drain if its corresponding bit in the Drive Select Register is set to a '1'. The default pin drive is CMOS.

Note: The slew rate is a measurement of the rise and fall times of an output. A higher slew rate means a faster output response and may create more electrical noise. A pin operates in a high slew rate when the corresponding bit in the Drive Register is set to '1'. The default rate is slow slew.

Table 38 shows the Drive Register for Ports A, B, C, D, E, F and G. It summarizes which pins can be configured as Open Drain outputs and which pins the slew rate can be set for.

Table 38. Drive register pin assignment(1)

Drive register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Port A	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain
Port B	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain
Port C	Slew Rate	Slew Rate	Slew Rate	Slew Rate	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port D	NA	NA	NA	NA	Open Drain	Open Drain	Open Drain	Open Drain
Port E	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain
Port F	Slew Rate	Slew Rate	Slew Rate	Slew Rate	Slew Rate	Slew Rate	Slew Rate	Slew Rate
Port G	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain	Open Drain

1. NA = Not Applicable.

10.4 Port Data registers

The Port Data Registers, shown in *Table 39*, are used by the microcontroller to write data to or read data from the ports. *Table 39* shows the register name, the ports having each register type, and microcontroller access for each register type. The registers are described below.

10.4.1 Data In

Port pins are connected directly to the Data In buffer. In MCU I/O input mode, the pin input is read through the Data In buffer.

10.4.2 Data Out register

Stores output data written by the MCU in the MCU I/O output mode. The contents of the Register are driven out to the pins if the Direction Register or the output enable product term is set to “1”. The contents of the register can also be read back by the microcontroller.

Table 39. Port Data registers

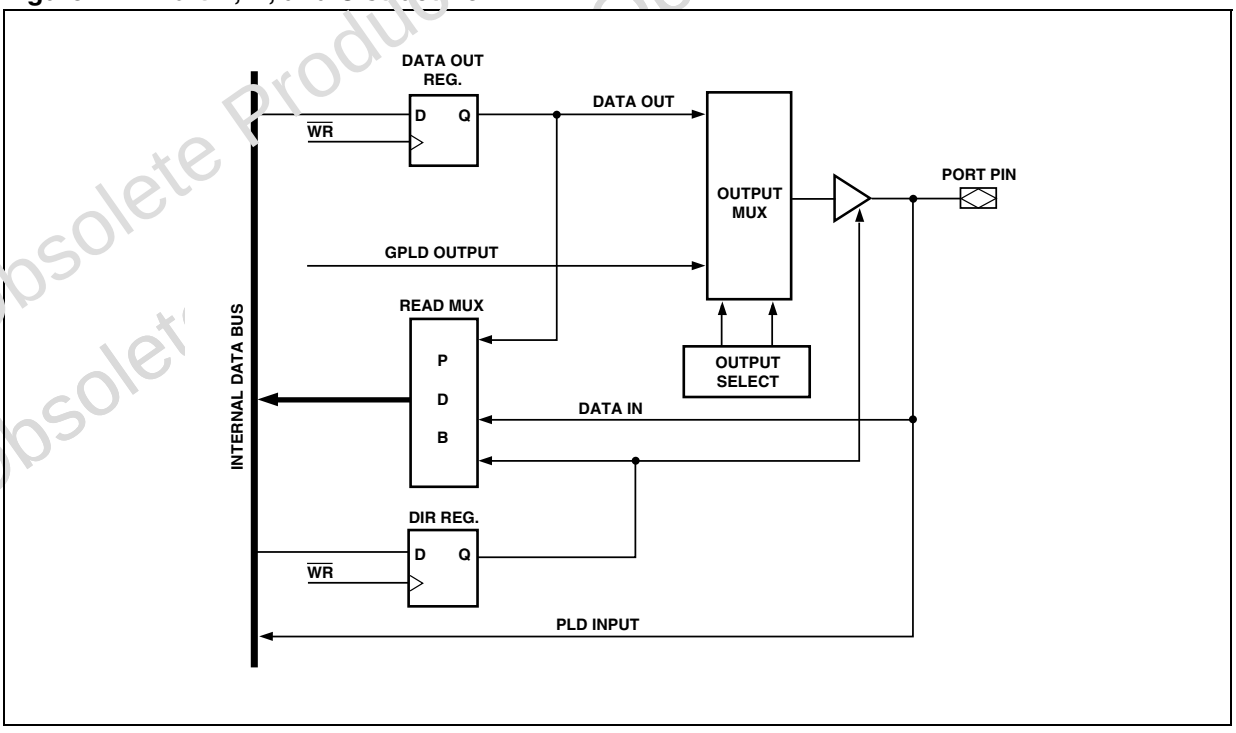
Register Name	Port	MCU Access
Data In	A, B, C, D, E, F, G	READ - input on pin
Data Out	A, B, C, D, E, F, G	WRITE/READ

10.5 Port A, B, and C registers

Ports A and B have similar functionality and structure, as shown in *Figure 24*. The two ports can be configured to perform one or more of the following functions:

- MCU I/O mode
- GPLD Output – Combinatorial PLD outputs.
- PLD input – Input to the PLDs.
- Address In – Additional high address inputs may be latched by ALE.
- Open Drain/Slew Rate
  - pins PC[7:0]can be configured to fast slew rate,
  - pins PA[7:0] and PB[7:0] can be configured to Open Drain mode.

Figure 24. Port A, B, and C structure



10.6 Port D – functionality and structure

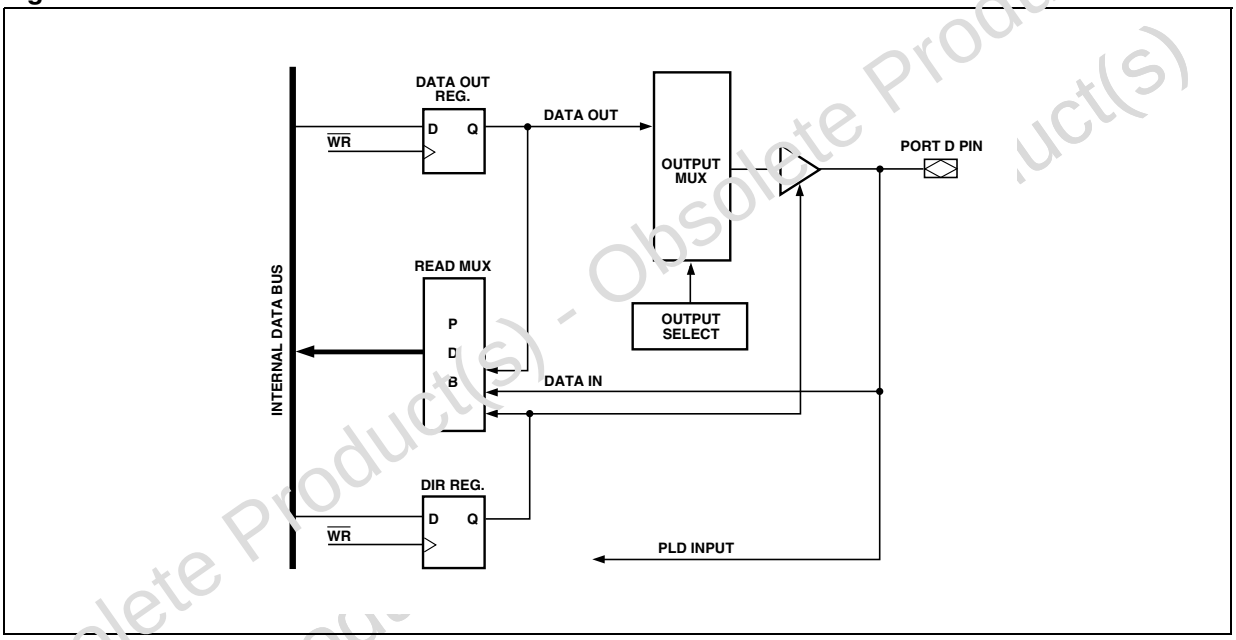
Port D has four I/O pins (see *Figure 25*). Port D can be configured to program one or more of the following functions:

- MCU I/O mode
- PLD input – direct input to PLD

Port D pins can be configured in PSDsoft as input pins for other dedicated functions:

- PD0 – ALE, as address strobe input
- PD1 – CLKIN, as clock input to the PLD and APD counter
- PD2 – CSI, as active low chip select input. A high input will disable the Flash/SRAM and CSIOP.
- PD3 – $\overline{WRH}$, as active low Write Enable (high byte) input or as $\overline{DBE}$ input from 68HC912

Figure 25. Port D structure



10.7 Port E – functionality and structure

Port E can be configured to perform one or more of the following functions (see *Figure 26*):

- MCU I/O mode
- In-system programming – JTAG port can be enabled for programming/erase of the PSD4135G2/G2V device (see *Section 12: In-circuit programming using the JTAG-ISP Interface*).Pins that are configured as JTAG pins in PSDsoft will not be available for other I/O functions.
- Open Drain – Port E pins can be configured in Open Drain mode
- Latched Address Output – Provided latched address (A7-0) output

10.8 Port F – functionality and structure

Port F can be configured to perform one or more of the following functions:

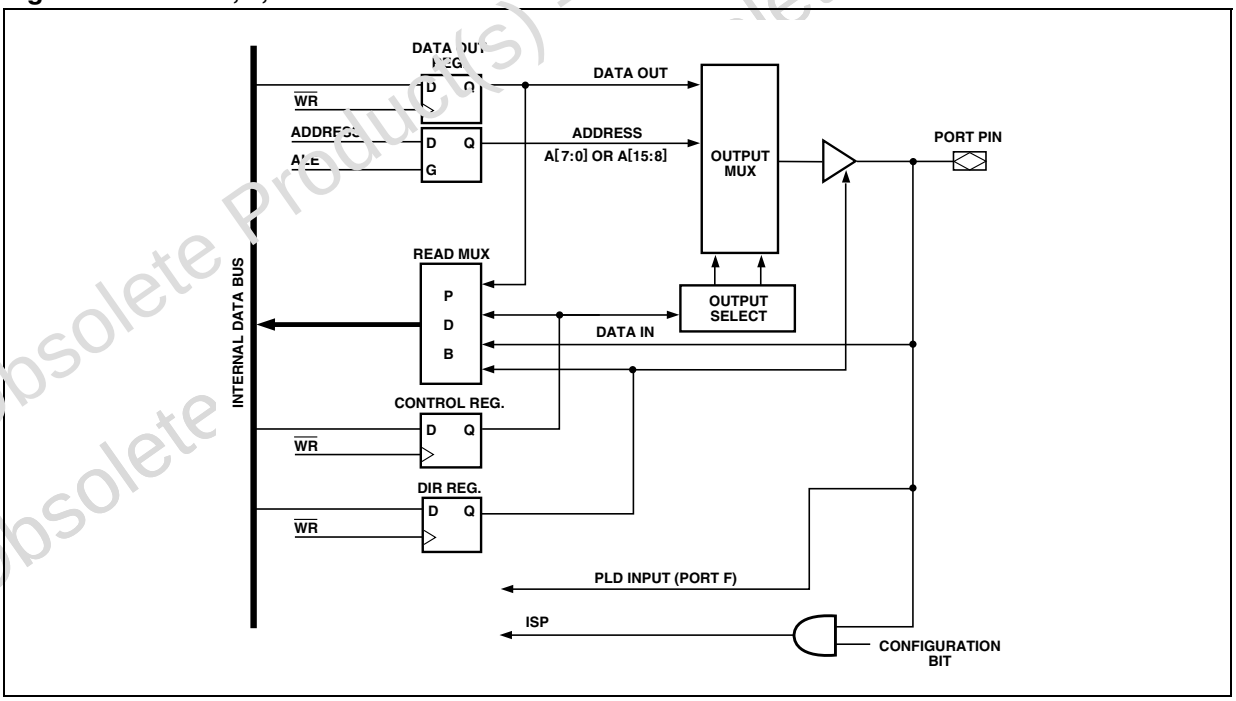
- MCU I/O mode
- PLD input – as direct input ot the PLD array.
- Address In – additional high address inputs. Direct input to the PLD array.
- Latched Address Out – Provide latched address out per *Table 43*.
- Slew Rate – pins can be set up for fast slew rate.
- Data Port – connected to D[7:0] when Port F is configured as Data Port for a non-multiplexed bus.
- MCU Reset mode – for 16-bit Motorola 683XX and HC16 microcontrollers.

10.9 Port G – functionality and structure

Port G can be configured to perform one or more of the following functions.

- MCU I/O mode
- Latched Address Out – provide latched address out per *Table 43*.
- Open Drain – pins can be configured in Open Drain mode
- Data Port – connected to D[15:8] when Port G is configured as Data Port for a non-multiplexed bus.
- MCU Reset mode – for 16-bit Motorola 683XX and HC16 microcontrollers

Figure 26. Port E, F, and G structure



11 Power management

The PSD4135G2 and PSD4135G2V offer configurable power saving options. These options may be used individually or in combinations, as follows:

- All memory types in a PSD (Flash, secondary Flash, and SRAM) are built with Zero-Power technology. In addition to using special silicon design methodology, Zero-Power technology puts the memories into standby mode when address/data inputs are not changing (zero DC current). As soon as a transition occurs on an input, the affected memory “wakes up”, changes and latches its outputs, then goes back to standby. The designer does not have to do anything special to achieve memory standby mode when no inputs are changing—it happens automatically.
  The PLD sections can also achieve standby mode when its inputs are not changing, see PMMR registers below.
- Like the Zero-Power feature, the Automatic power-down (APD) logic allows the PSD to reduce to standby current automatically. The APD will block MCU address/data signals from reaching the memories and PLDs. This feature is available on all PSD4135G2/G2V device. The APD unit is described in more detail in *Section 11.1: Automatic power-down (APD) unit and Power-down mode*.
  Built in logic will monitor the address strobe of the MCU for activity. If there is no activity for a certain time period (MCU is asleep), the APD logic initiates Power-down mode (if enabled). Once in Power-down mode, all address/data signals are blocked from reaching PSD memories and PLDs, and the memories are deselected internally. This allows the memories and PLDs to remain in standby mode even if the address/data lines are changing state externally (noise, other devices on the MCU bus, etc.). Keep in mind that any unblocked PLD input signals that are changing states keeps the PLD out of standby mode, but not the memories.
- The PSD Chip Select input (CSI) can be used to disable the internal memories, placing them in standby mode even if inputs are changing. This feature does not block any internal signals or disable the PLDs. This is a good alternative to using the APD logic, especially if your MCU has a chip select output. There is a slight penalty in memory access time when the CSI signal makes its initial transition from deselected to selected.
- The PMMR registers can be written by the MCU at run-time to manage power. All PSD devices support “blocking bits” in these registers that are set to block designated signals from reaching both PLDs. Current consumption of the PLDs is directly related to the composite frequency of the changes on their inputs (see *Figure 30* and *Figure 31*).

Significant power savings can be achieved by blocking signals that are not used in PLD logic equations at run time. PSDsoft creates a fuse map that automatically blocks the low address byte (A7-A0) or the control signals (CNTL0-2, ALE and $\overline{WRH}$/$\overline{DBE}$) if none of these signals are used in PLD logic equations.

The PSD4135G2 and PSD4135G2V devices have a Turbo bit in the PMMR0 register. This bit can be set to disable the Turbo mode feature (default is Turbo mode on). While Turbo mode is disabled, the PLDs can achieve standby current when no PLD inputs are changing (zero DC current). Even when inputs do change, significant power can be saved at lower frequencies (AC current), compared to when Turbo mode is enabled. Conversely, when the Turbo mode is enabled, there is a significant DC current component and the AC component is higher.

11.1 Automatic power-down (APD) unit and Power-down mode

The APD Unit, shown in *Figure 27*, puts the PSD into Power-down mode by monitoring the activity of the address strobe (ALE/AS). If the APD unit is enabled, as soon as activity on the address strobe stops, a four bit counter starts counting. If the address strobe remains inactive for fifteen clock periods of the CLKIN signal, the Power-down (PDN) signal becomes active, and the PSD will enter into Power-down mode, discussed next.

11.1.1 Power-down mode

By default, if you enable the PSD APD unit, Power-down mode is automatically enabled.

The device will enter Power-down mode if the address strobe (ALE/AS) remains inactive for fifteen CLKIN (pin PD1) clock periods.

The following should be kept in mind when the PSD is in Power-down mode:

- If the address strobe starts pulsing again, the PSD will return to normal operation. The PSD will also return to normal operation if either the CSI input returns low or the Reset input returns high.
- The MCU address/data bus is blocked from all memories and PLDs.
- Various signals can be blocked (prior to Power-down mode) from entering the PLDs by setting the appropriate bits in the PMMR registers. The blocked signals include MCU control signals and the common clock (CLKIN). Note that blocking CLKIN from the PLDs will not block CLKIN from the APD unit.
- All PSD memories enter Standby mode and are drawing standby current. However, the PLDs and I/O ports do not go into Standby mode because you don't want to have to wait for the logic and I/O to "wake-up" before their outputs can change. See *Table 40* for Power-down mode effects on PSD ports.
- Typical standby current is 50 µA for 5 V parts. This standby current value assumes that there are no transitions on any PLD input.

Table 40. Effect of Power-down mode on ports

Port function	Pin level
MCU I/O	No Change
PLD Out	No Change
Address Out	Undefined
Data port	Tri-State
Peripheral I/O	Tri-State

Table 41. PSD timing and standby current during Power-down mode(1)

Mode	PLD propagation delay	Memory access time	Access recovery time to normal access	Typical standby current
Power-down	Normal t_{PD}	No Access	t_{LVDV}	I_{SB}(2)

1. Power-down does not affect the operation of the PLD. The PLD operation in this mode is based only on the Turbo bit.
2. Typical current consumption, see *Table 52*, assuming no PLD inputs are changing state and the PLD Turbo bit is 0.

Figure 27. APD unit

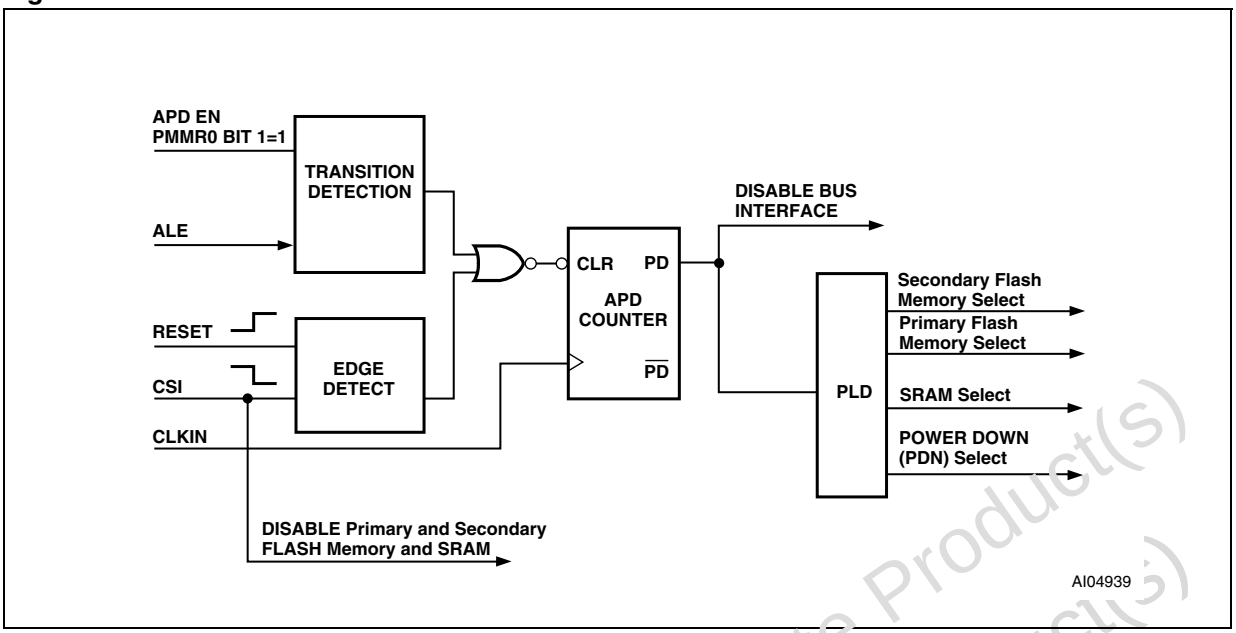
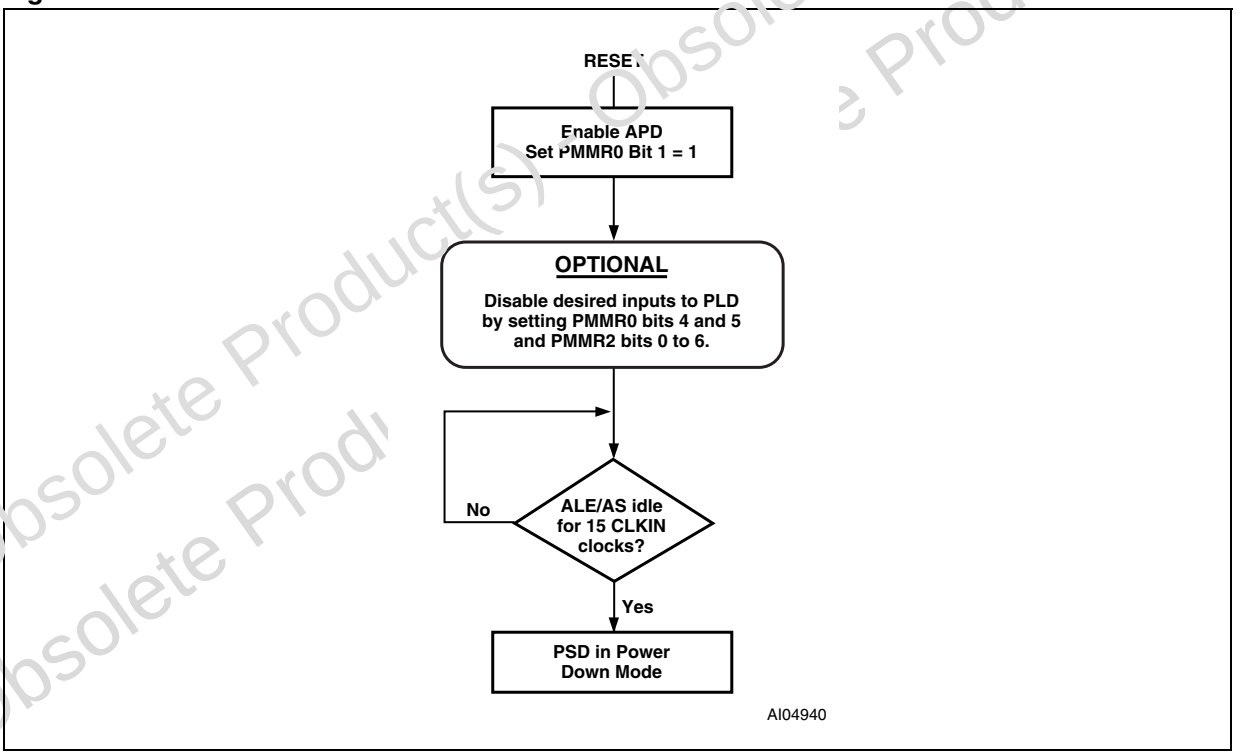


Figure 28. Enable Power-down flowchart



11.1.2 Other power saving options

The PSD4135G2 and PSD4135G2V offer other reduced power saving options that are independent of the Power-down mode. Except for the SRAM Standby and CSI input features, they are enabled by setting bits in the PMMR0 and PMMR2 registers.

Zero Power PLD

The power and speed of the PLDs are controlled by the Turbo bit (bit 3) in the PMMR0.

By setting the bit to “1”, the Turbo mode is disabled and the PLDs consume Zero Power current when the inputs are not switching for an extended time of 70 ns. The propagation delay time will be increased after the Turbo bit is set to “1” (turned off) when the inputs change at a composite frequency of less than 15 MHz. When the Turbo bit is set to a “0” (turned on), the PLDs run at full power and speed. The Turbo bit affects the PLD’s D.C. power, AC power, and propagation delay. Refer to AC/DC spec for PLD timings.

Note: Blocking MCU control signals with PMMR2 bits can further reduce PLD AC power consumption.

The CSI input

Pin PD2 of Port D can be configured in PSDsoft as the CSI input. When low, the signal selects and enables the internal Flash, Boot Block, SRAM, and I/O for read or write operations involving the PSD4135G2/G2V. A high on the CSI pin will disable the Flash memory, Boot Block, and SRAM, and reduce the PSD power consumption. However, the PLD and I/O pins remain operational when CSI is high.

Note: There may be a timing penalty when using the CSI pin depending on the speed grade of the PSD that you are using. See the timing parameter t_{SLQV} in the AC/DC specs.

Input clock

The PSD4135G2 and PSD4135G2V provide the option to turn off the CLKIN input to the PLD AND array to save AC power consumption. During Power-down mode, or, if the CLKIN input is not being used as part of the PLD logic equation, the clock should be disabled to save AC power. The CLKIN will be disconnected from the PLD AND array by setting bit 4 to a “1” in PMMR0.

MCU control signals

The PSD4135G2 PSD4135G2V provide the option to turn off the address input (A7-0) and input control signals (CNTL0-2, ALE, and $\overline{WRH}$/$\overline{DBE}$) to the PLD to save AC power consumption. These signals are inputs to the PLD AND array. During Power-down mode, or, if any of them are not being used as part of the PLD logic equation, these control signals should be disabled to save AC power. They will be disconnected from the PLD AND array by setting bits 0, 2, 3, 4, 5, and 6 to a “1” in the PMMR2.

11.1.3 Reset and power-on requirement

Power-on reset

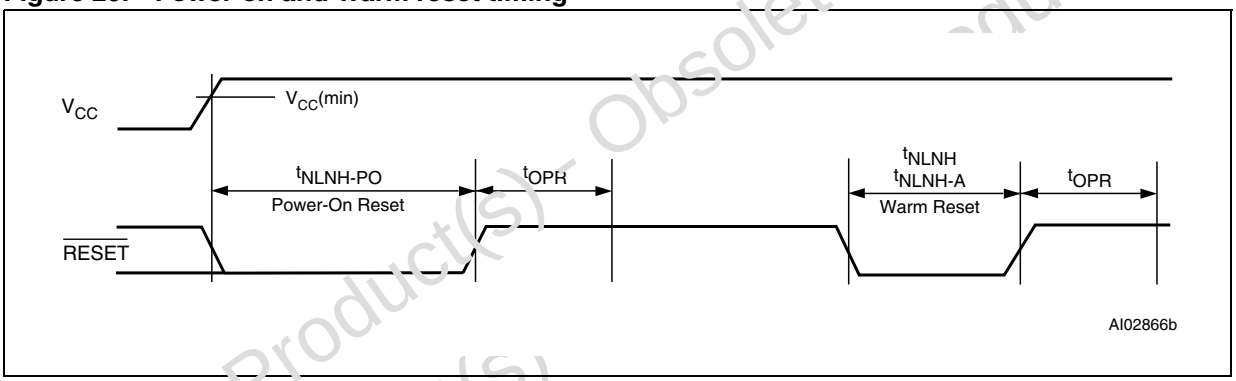
Upon power up the PSD4135G2 and PSD4135G2V require a reset pulse of $t_{NLNH-PO}$ (minimum 1 ms) after VCC is steady. During this time period the device loads internal configurations, clears some of the registers and sets the Flash into operating mode. After the rising edge of reset, the PSD4135G2/G2V remains in the reset state for an additional tOPR (maximum 120 ns) nanoseconds before the first memory access is allowed.

The PSD4135G2/G2V Flash memory is reset to the read array mode upon power up. The FSi and CSBOOTi select signals along with the write strobe signal must be in the false state during power-up reset for maximum security of the data contents and to remove the possibility of data being written on the first edge of a write strobe signal. Any Flash memory write cycle initiation is prevented automatically when VCC is below V_{LKO}.

Warm reset

Once the device is up and running, the device can be reset with a much shorter pulse of t_{NLNH} (minimum 150 ns). The same t_{OPR} time is needed before the device is operational after Warm reset. *Figure 29* shows the timing of the Power-on and Warm reset.

Figure 29. Power-on and Warm reset timing



I/O pin, register and PLD status at Reset

Table 42 shows the I/O pin, register and PLD status during Power-on reset, Warm reset and Power-down mode. PLD outputs are always valid during Warm reset, and they are valid in Power-on reset once the internal PSD configuration bits are loaded. This loading of PSD is completed typically long before the VCC ramps up to operating level. Once the PLD is active, the state of the outputs are determined by the equations specified in PSDsoft.

Reset of Flash Erase and programming cycles

An external reset on the $\overline{RESET}$ pin will also reset the internal Flash memory state machine. When the Flash is in programming or erase mode, the $\overline{RESET}$ pin will terminate the programming or erase operation and return the Flash back to read mode in t_{NLNH-A} (minimum 25 µs) time.

Table 42. Status during Power-on reset, Warm reset and Power-down mode

Port configuration	Power-on reset	Warm reset	Power-down mode
MCU I/O	Input mode	Input mode	Unchanged
PLD output	Valid after internal PSD configuration bits are loaded	Valid	Depends on inputs to PLD (addresses are blocked in PD mode)
Address Out	Tri-stated	Tri-stated	Not defined
Data Port	Tri-stated	Tri-stated	Tri-stated
PMMR0 and PMMR2	Cleared to '0'	Unchanged	Unchanged
VM register(1)	Initialized, based on the selection in PSDsoft Express Configuration menu	Initialized, based on the selection in PSDsoft Express Configuration menu	Unchanged
All other registers	Cleared to '0'	Cleared to '0'	Unchanged

1. The SR_code and Peripheral mode bits in the VM register are always cleared to '0' on Power-on reset or Warm reset.

12 In-circuit programming using the JTAG-ISP Interface

The JTAG-ISP interface on the PSD4135G2/G2V can be enabled on Port E (see *Table 43*). All memory (Flash and Flash Boot Block), PLD logic, and PSD configuration bits may be programmed through the JTAG-ISC interface. A blank part can be mounted on a printed circuit board and programmed using JTAG-ISP.

The standard JTAG signals (IEEE 1149.1) are TMS, TCK, TDI, and TDO. Two additional signals, TSTAT and $\overline{\text{TERR}}$, are optional JTAG extensions used to speed up program and erase operations.

Note: By default, on a blank PSD (as shipped from the factory, or after erasure), four pins on Port E are enabled for the basic JTAG signals TMS, TCK, TDI, and TDO.

See Application Note *AN1153* for more details on JTAG in-system programming (ISP).

Table 43. JTAG port signals

Port E pin	JTAG signals	Description
PE0	TMS	Mode Select
PE1	TCK	Clock
PE2	TDI	Serial Data In
PE3	TDO	Serial Data Out
PE4	TSTAT	Status
PE5	$\overline{\text{TERR}}$	Error Flag

12.1 Standard JTAG signals

The JTAG configuration bit (non-volatile) inside the PSD can be set by the user in the PSDsoft. Once this bit is set and programmed in the PSD, the JTAG pins are dedicated to JTAG at all times and is in compliance with IEEE 1149.1. After power up the standard JTAG signals (TDI, TDO TCK and TMS) are inputs, waiting for a serial command from an external JTAG controller device (such as FlashLink or Automated Test Equipment). When the enabling command is received from the external JTAG controller, TDO becomes an output and the JTAG channel is fully functional inside the PSD. The same command that enables the JTAG channel may optionally enable the two additional JTAG pins, TSTAT and $\overline{\text{TERR}}$.

The PSD4135G2 and PSD4135G2V support JTAG ISP commands, but not Boundary Scan. ST's PSDsoft software tool and FlashLink JTAG programming cable implement these JTAG-ISP commands.

12.2 JTAG extensions

TSTAT and $\overline{\text{TERR}}$ are two JTAG extension signals enabled by a JTAG command received over the four standard JTAG pins (TMS, TCK, TDI, and TDO). They are used to speed programming and erase functions by indicating status on PSD pins instead of having to scan the status out serially using the standard JTAG channel. See Application Note 54.

$\overline{\text{TERR}}$ will indicate if an error has occurred when erasing a sector or programming a byte in Flash memory. This signal will go low (active) when an error condition occurs, and stay low until a special JTAG command is executed or a chip reset pulse is received after an “ISC-DISABLE” command.

TSTAT behaves the same as the Rdy/Bsy signal described in *Section 7.1.2: Ready/Busy pin (PE4)*. TSTAT will be high when the PSD4135G2/G2V device is in read array mode (Flash memory and Boot Block contents can be read). TSTAT will be low when Flash memory programming or erase cycles are in progress, and also when data is being written to the secondary Flash block.

TSTAT and $\overline{\text{TERR}}$ can be configured as open-drain type signals with a JTAG command.

12.3 Security and Flash memories protection

When the security bit is set, the device cannot be read on a device programmer or through the JTAG Port. When using the JTAG Port, only a full chip erase command is allowed.

All other program/erase/verify commands are blocked. Full chip erase returns the part to a non-secured blank state. The Security Bit can be set in PSDsoft.

All Flash memory and Boot sectors can individually be sector protected against erasures. The sector protect bits can be set in PSDsoft.

13 Initial delivery state

When delivered from ST, the PSD device has all bits in the memory and PLDs set to '1.' The PSD Configuration register bits are set to '0.' The code, configuration, and PLD logic are loaded using the programming procedure. Information for programming the device is available directly from ST. Please contact your local sales representative.

14 Maximum rating

Stressing the device above the rating listed in *Table 44: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the *Section 15: DC and AC parameters* of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 44. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_{STG}	Storage temperature	–65	125	°C
T_{LEAD}	Lead temperature during Soldering (20 seconds max.)(1)		235	°C
V_{IO}	Input and output voltage (Q = V_{OH} or Hi-Z)	–0.6	7.0	V
V_{CC}	Supply voltage	–0.6	7.0	V
V_{PP}	Device programmer supply voltage	–0.6	14.0	V
V_{ESD}	Electrostatic discharge voltage (Human Body model)(2)	–2000	2000	V

1. IPC/JEDEC J-STD-020A
2. JEDEC Std JESD22-A114A (C1=100 pF, R1=1500 Ω, R2=500 Ω)

15 DC and AC parameters

These tables describe the AD and DC parameters of the PSD4235G2:

- DC electrical specification
- AC timing specification
  - PLD timing
    Combinatorial timing
    Synchronous clock mode
    Asynchronous clock mode
    Input macrocell timing
  - MCU timing
    READ timing
    WRITE timing
    Peripheral mode timing
    Power-down and Reset timing

The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

The following are issues concerning the parameters presented:

- In the DC specification the supply current is given for different modes of operation. Before calculating the total power consumption, determine the percentage of time that the PSD is in each mode. Also, the supply power is considerably different if the Turbo bit is 0.
- The AC power component gives the PLD, Flash memory, and SRAM mA/MHz specification. *Figure 30* show the PLD mA/MHz as a function of the number of Product Terms (PT) used.
- In the PLD timing parameters, add the required delay when Turbo bit is 0.

Figure 30. PLD I_{CC} /frequency consumption - 5 V

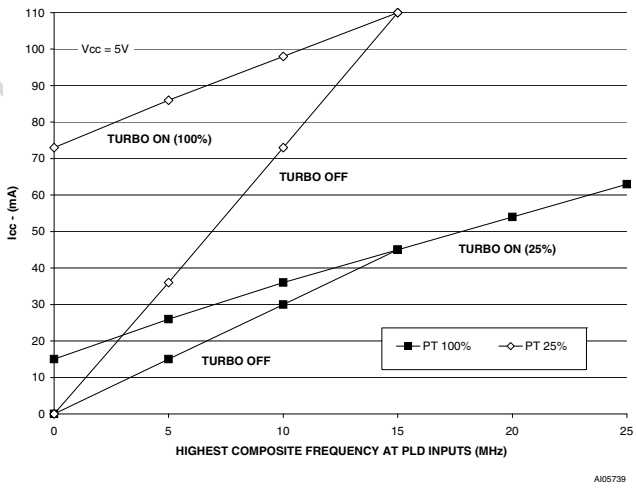


Figure 31. PLD I_{CC} /frequency consumption - 3 V

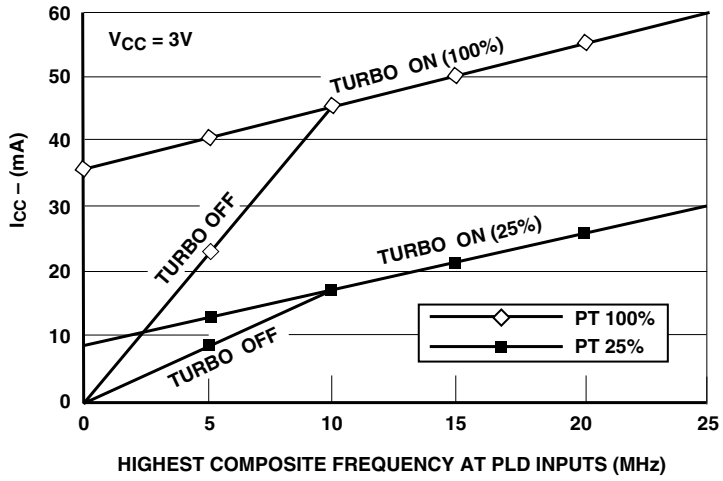


Table 45. Example of PSD typical power calculation at V_{CC} = 5.0V (with Turbo mode on)(1)

Conditions		
Highest Composite PLD input frequency		
	(Freq PLD)	= 8 MHz
MCU ALE frequency (Freq ALE)		= 4 MHz
	% Flash memory Access	= 80%
	% SRAM access	= 15%
	% I/O access	= 5% (no additional power above base)
Operational modes		
	% Normal	= 10%
	% Power-down mode	= 90%
Number of product terms used		
	(from fitter report)	= 45 PT
	% of total product terms	= 45/176 = 25.5%
	Turbo mode	= ON
Calculation (using typical values)		
I_{CC} total		= Ipwrdown x %pwrdown + %normal x (I_{CC} (ac) + I_{CC} (dc))

Table 45. Example of PSD typical power calculation at V_{CC} = 5.0V (with Turbo mode on)(1)

Conditions		
	= Ipwrdown x %pwrdown + % normal x (%flash x 2.5 mA/MHz x Freq ALE	
		+ %SRAM x 1.5 mA/MHz x Freq ALE
		+ % PLD x 2 mA/MHz x Freq PLD
		+ #PT x 400 µA/PT)
	= 50 µA x 0.90 + 0.1 x (0.8 x 2.5 mA/MHz x 4 MHz	
		+ 0.15 x 1.5 mA/MHz x 4 MHz
		+ 2 mA/MHz x 8 MHz
		+ 45 x 0.4 mA/PT)
	= 45 µA + 0.1 x (8 + 0.9 + 16 + 18 mA)	
	= 45 µA + 0.1 x 42.9	
	= 45 µA + 4.29 mA	
	= 4.34 mA	

1. This is the operating power with no Flash memory Program or Erase cycles in progress. Calculation is based on I_{OUT}=0 mA.

Table 46. Example of PSD typical power calculation at V_{CC} = 5.0V (with Turbo mode off)(1)

Conditions		
Highest Composite PLD input frequency		
	(Freq PLD)	= 8 MHz
MCU ALE frequency (Freq ALE)		= 4 MHz
	% Flash memory Access	= 80%
	% SRAM access	= 15%
	% I/O access	= 5% (no additional power above base)
Operational modes		
	% Normal	= 10%
	% Power-down mode	= 90%
Number of product terms used		
	(from fitter report)	= 45 PT
	% of total product terms	= 45/176 = 25.5%
	Turbo mode	= Off
Calculation (using typical values)		
I_{CC} total		= Ipwrdown x %pwrdown + %normal x (I_{CC} (ac) + I_{CC} (dc))
		= Ipwrdown x %pwrdown + % normal x (%flash x 2.5 mA/MHz x Freq ALE
		+ %SRAM x 1.5 mA/MHz x Freq ALE
		+ % PLD x (from graph using Freq PLD))
		= 50 µA x 0.90 + 0.1 x (0.8 x 2.5 mA/MHz x 4 MHz
		+ 0.15 x 1.5 mA/MHz x 4 MHz
		+ 24 mA)
		= 45 µA + 0.1 x (8 + 0.9 + 24)
		= 45 µA + 0.1 x 32.9
		= 45 µA + 3.29 mA
		= 3.34 mA

1. This is the operating power with no Flash memory Program or Erase cycles in progress. Calculation is based on I_{OUT} = 0 mA.

Table 47. Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage (PSD4135G2)	4.5	5.5	V
	Supply voltage (PSD4135G2V)	3.0	3.6	V
T_A	Ambient operating temperature (industrial)	–40	85	°C
	Ambient operating temperature (commercial)	0	70	°C

Table 48. AC signal letters for PLD timings(1)

Letter	Description
A	Address input
C	CEout output
D	Input data
E	E input
G	Internal WDOG_ON signal
I	Interrupt input
L	ALE input
N	Reset input or output
P	Port signal output
Q	Output data
R	$\overline{WR}$, $\overline{UDS}$, $\overline{LDS}$, $\overline{DS}$, IORD, $\overline{PSEN}$ inputs
S	Chip Select input
T	R/$\overline{W}$ input
W	Internal PDN Signal
M	Output macrocell

1. Example: t_{AVLX} - Time from Address Valid to ALE Invalid.

Table 49. AC signal behavior symbols for PLD timings

Letter	Description
t	Time
L	Logic level low or ALE
H	Logic level high
V	Valid
X	No longer a valid logic level
Z	Float

Table 50. AC measurement conditions(1)

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	30		pF

1. Output Hi-Z is defined as the point where data out is no longer driven.

Table 51. Capacitance(1)

Symbol	Parameter	Test condition	Typ(2)	Max.	Unit
C_{IN}	Input capacitance (for input pins)	V_{IN} = 0V	4	6	pF
C_{OUT}	Output capacitance (for input/output pins)	V_{OUT} = 0V	8	12	pF
C_{VPP}	Capacitance (for CNTL2/V_{PP})	V_{PP} = 0V	18	25	pF

1. Sampled only, not 100% tested.
2. Typical values are for T_A = 25°C and nominal supply voltages.

Figure 32. AC measurement I/O waveform

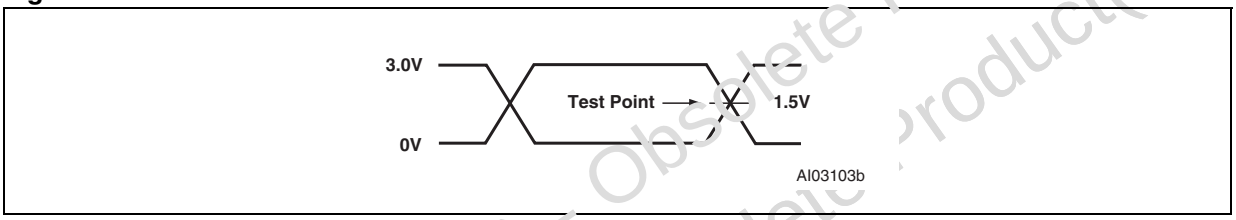


Figure 33. AC measurement load circuit

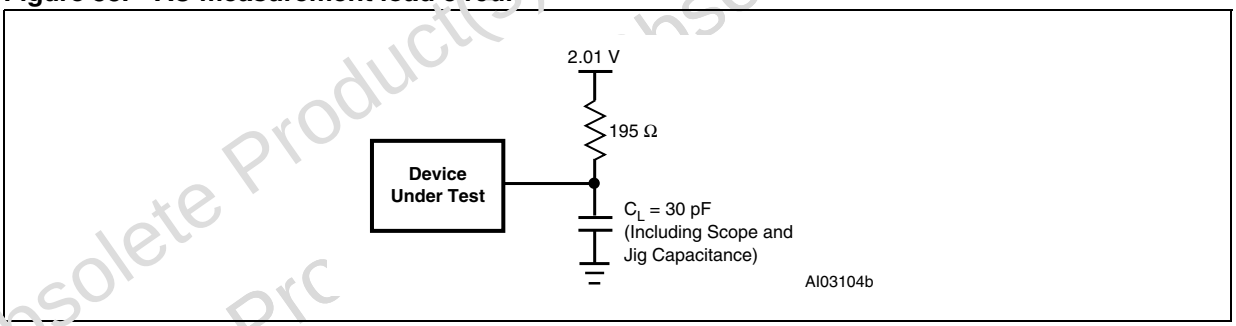


Figure 34. Switching waveforms - key

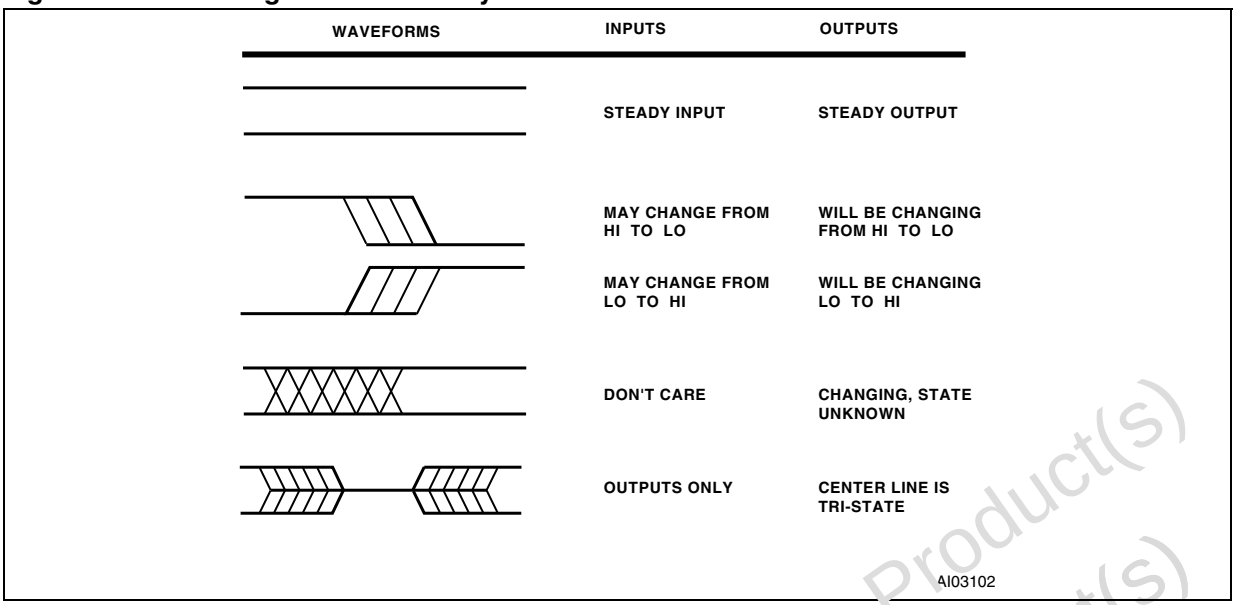


Table 52. DC characteristics 5 V

Symbol	Parameter	Test condition (in addition to those in Table 47)	Min.	Typ.	Max.	Unit
V_{IH}	input high voltage voltage	4.5 V < V_{CC} < 5.5 V	2		V_{CC} +0.5	V
V_{IL}	input low voltage	4.5 V < V_{CC} < 5.5 V	–0.5		0.8	V
V_{IH1}	$\overline{RESET}$ high level input voltage	(1)	0.8V_{CC}		V_{CC} +0.5	V
V_{IL1}	$\overline{RESET}$ low level input voltage	(1)	–0.5		0.2V_{CC} –0.1	V
V_{HYS}	$\overline{RESET}$ pin hysteresis		0.3			V
V_{LKO}	V_{CC} (min) for Flash Erase and Program		2.5		4.2	V
V_{OL}	Output low voltage	I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA, V_{CC} = 4.5 V		0.25	0.45	V
V_{OH}	Output high voltage	I_{OH} = –20 µA, V_{CC} = 4.5 V	4.4	4.49		V
		I_{OH} = –2 mA, V_{CC} = 4.5 V	2.4	3.9		V
I_{SB}	Standby supply current for Power-down mode	$\overline{CSI}$ >V_{CC} –0.3 V(2)(3)		100	200	µA
I_{LI}	Input leakage current	V_{SS} < V_{IN} < V_{CC}	–1	±0.1	1	µA
I_{LO}	Output leakage current	0.45 V < V_{OUT} < V_{CC}	–10	±5	10	µA

Table 52. DC characteristics 5 V (continued)

Symbol	Parameter		Test condition (in addition to those in *Table 47*)	Min.	Typ.	Max.	Unit
I_{CC} (DC)(4)	Operating supply current	PLD Only	PLD_TURBO = Off, f = 0 MHz (Note 5)		0		µA/PT
			PLD_TURBO = On, f = 0 MHz		400	700	µA/PT
		Flash memory	During Flash memory WRITE/Erase Only		15	30	mA
			Read Only, f = 0 MHz		0	0	mA
		SRAM	f = 0 MHz		0	0	mA
I_{CC} (AC)	PLD AC Adder					(5)	
	Flash memory AC Adder				2.5	3.5	mA/ MHz
	SRAM AC Adder				1.5	3.0	mA/ MHz

1. Reset ($\overline{RESET}$) has hysteresis. V_{IL1} is valid at or below $0.2V_{CC}-0.1$. V_{IH1} is valid at or above $0.8V_{CC}$.
2. $\overline{CSI}$ deselected or internal Power-down mode is active.
3. PLD is in non-Turbo mode, and none of the inputs are switching.
4. I_O=0 mA
5. Please see *Figure 30* for the PLD current calculation.

Table 53. DC characteristics (3 V)

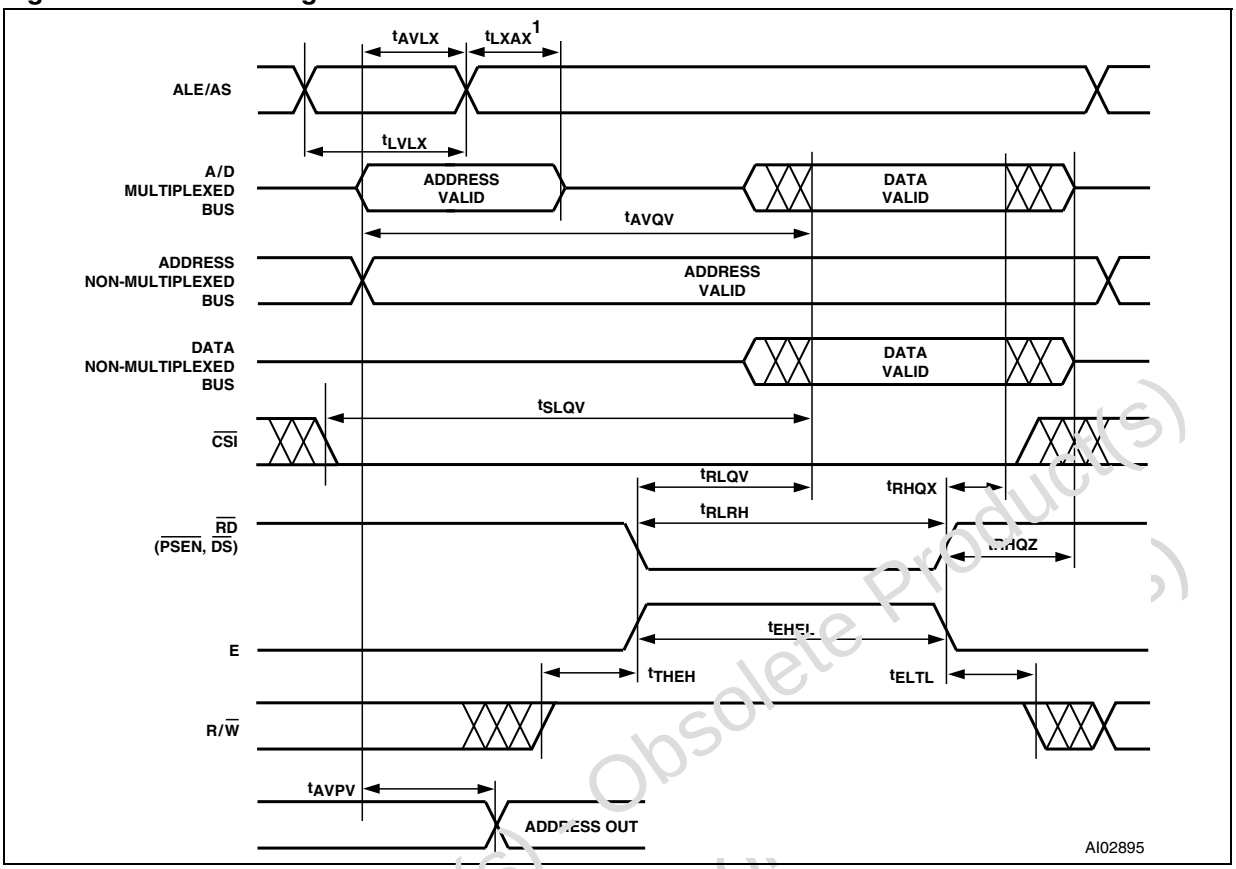
Symbol	Parameter	Test Condition (in addition to those in *Table 47*)	Min.	Typ.	Max.	Unit
V_{IH}	Input high voltage	3.0 V < V_{CC} < 3.6 V	$0.7V_{CC}$		V_{CC} +0.5	V
V_{IL}	Input low voltage	3.0 V < V_{CC} < 3.6 V	–0.5		0.8	V
V_{IH1}	$\overline{RESET}$ high level input voltage	(1)	$0.8V_{CC}$		V_{CC} +0.5	V
V_{IL1}	$\overline{RESET}$ low level input voltage	(1)	–0.5		$0.2V_{CC}-0.1$	V
V_{HYS}	$\overline{RESET}$ pin hysteresis		0.3			V
V_{LKO}	V_{CC} (min) for Flash Erase and Program		1.5		2.3	V
V_{OL}	Output low voltage	I_{OL} = 20 µA, V_{CC} = 4.5 V		0.01	0.1	V
		I_{OL} = 8 mA, V_{CC} = 4.5 V		0.15	0.45	V
V_{OH}	Output high voltage	I_{OH} = –20 µA, V_{CC} = 4.5 V	2.9	2.99		V
		I_{OH} = –2 mA, V_{CC} = 4.5 V	2.7	2.8		V
I_{SB}	Standby supply current for Power-down mode	$\overline{CSI}$ >V_{CC} –0.3 V(2)(3)		50	100	µA

Table 53. DC characteristics (3 V) (continued)

Symbol	Parameter		Test Condition (in addition to those in *Table 47*)	Min.	Typ.	Max.	Unit
I_{LI}	Input leakage current		$V_{SS} < V_{IN} < V_{CC}$	–1	±0.1	1	µA
I_{LO}	Output leakage current		$0.45 < V_{OUT} < V_{CC}$	–10	±5	10	µA
I_{CC} (DC)(4)	Operating supply current	PLD Only	PLD_TURBO = Off, f = 0 MHz (Note 5)		0		µA/PT
			PLD_TURBO = On, f = 0 MHz		200	400	µA/PT
		Flash memory	During Flash memory WRITE/Erase Only		10	25	mA
			Read Only, f = 0 MHz		0	0	mA
		SRAM	f = 0 MHz		0	0	mA
I_{CC} (AC)	PLD AC Adder				(5)		
	Flash memory AC Adder				1.5	2.0	mA/ MHz
	SRAM AC Adder				0.8	1.5	mA/ MHz

1. Reset ($\overline{RESET}$) has hysteresis. V_{IL1} is valid at or below $0.2V_{CC}$ –0.1. V_{IH1} is valid at or above $0.8V_{CC}$.
2. $\overline{CSI}$ deselected or internal Power-down mode is active.
3. PLD is in non-Turbo mode, and none of the inputs are switching.
4. I_O=0 mA
5. Please see *Figure 30* for the PLD current calculation.

Figure 35. READ timing



1. t_{AVLX} and t_{LXAX} are not required for 80C251 in Page mode or 80C51XA in Burst mode.

Table 54. READ timing (5 V)

Symbol	Parameter	Conditions	-70		-90		Turbo Off	Unit
			Min	Max	Min	Max		
t_{LVLX}	ALE or AS pulse width		15		20			ns
t_{AVLX}	Address setup time	(1)	4		6			ns
t_{LAX}	Address hold time		7		8			ns
t_{AVQV}	Address valid to data valid			70		90	+ 12	ns
t_{SLQV}	CS valid to data valid			75		100		ns
t_{RLQV}	$\overline{RD}$ to data valid 8-bit bus	(2)		24		32		ns
	$\overline{RD}$ or $\overline{PSEN}$ to data valid 8-bit Bus, 8031, 80251	(3)		31		38		ns
t_{RHQX}	$\overline{RD}$ data hold time	(4)	0		0			ns
t_{RLRH}	$\overline{RD}$ pulse width		27		32			ns
t_{RHQZ}	$\overline{RD}$ to data high-Z			20		25		ns
t_{EHEL}	E pulse width		27		32			ns
t_{THEH}	R/$\overline{W}$ setup time to Enable		6		10			ns

Table 54. READ timing (5 V) (continued)

Symbol	Parameter	Conditions	-70		-90		Turbo Off	Unit
			Min	Max	Min	Max		
t_{ELTL}	R/$\overline{W}$ Hold time after Enable		0		0			ns
t_{AVPV}	Address input valid to address output delay	(5)		20		25		ns

1. Any input used to select an internal PSD function.
2. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, and $\overline{UDS}$ signals.
3. $\overline{RD}$ and $\overline{PSEN}$ have the same timing.
4. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, and $\overline{PSEN}$ signals.
5. In multiplexed mode, latched addresses generated from ADIO delay to address output on any Port.

Table 55. READ timing (3 V)

Symbol	Parameter	Conditions	-90		-12		Turbo Off	Unit
			Min	Max	Min	Max		
t_{LVLX}	ALE or AS pulse width		22		24			ns
t_{AVLX}	Address setup time	(1)	7		9			ns
t_{LXAX}	Address hold time		3		10			ns
t_{AVQV}	Address valid to Data valid			90		120	+ 20	ns
t_{SLQV}	CS valid to Data valid			90		120		ns
t_{RLQV}	$\overline{RD}$ to Data valid 8-bit bus	(2)		35		35		ns
	$\overline{RD}$ or $\overline{PSEN}$ to Data valid 8-bit bus, 8031, 80251	(3)		45		48		ns
t_{RHQX}	$\overline{RD}$ Data hold time	(4)	0		0			ns
t_{RLRH}	$\overline{RD}$ pulse width		36		40			ns
t_{RHQZ}	$\overline{RD}$ to Data high-Z			38		40		ns
t_{EHEL}	E pulse width		38		42			ns
t_{RHEH}	R/$\overline{W}$ setup time to enable		10		16			ns
t_{ELTL}	R/$\overline{W}$ hold time after enable		0		0			ns
t_{AVPV}	Address input valid to Address output delay	(5)		30		35		ns

1. Any input used to select an internal PSD function.
2. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, and $\overline{UDS}$ signals.
3. $\overline{RD}$ and $\overline{PSEN}$ have the same timing.
4. $\overline{RD}$ timing has the same timing as $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, and $\overline{PSEN}$ signals.
5. In multiplexed mode, latched addresses generated from ADIO delay to address output on any Port.

Figure 36. WRITE timing

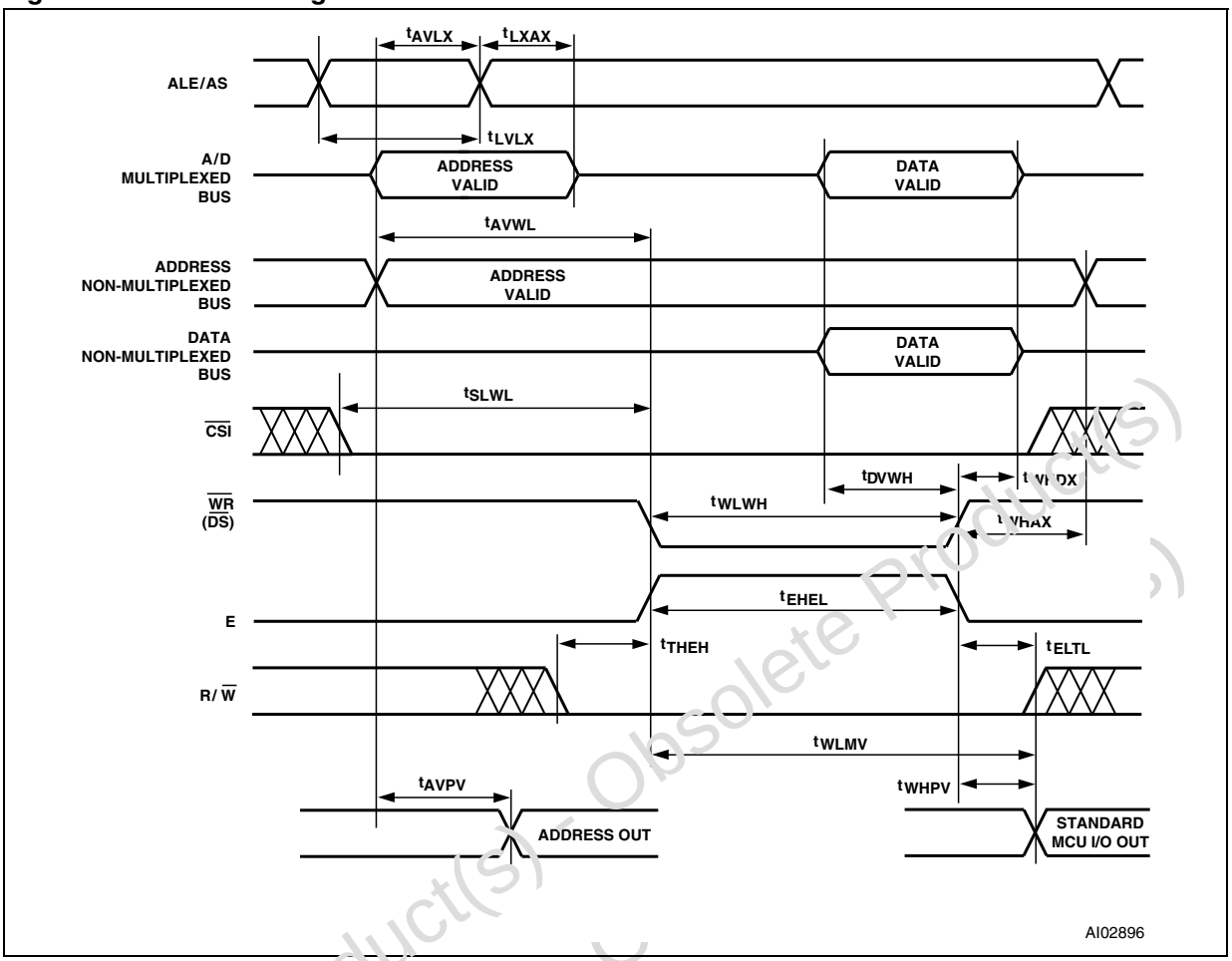


Table 56. WRITE timing (5 V)

Symbol	Parameter	Conditions	-70		-90		Unit
			Min	Max	Min	Max	
t_{LVLX}	ALE or AS pulse width		15		20		ns
t_{AVLX}	Address setup time	(1)	4		6		ns
t_{LXAX}	Address hold time	(1)	7		8		ns
t_{AVWL}	Address valid to leading edge of $\overline{WR}$	(1)(2)	8		15		ns
t_{SLWL}	$\overline{CS}$ Valid to leading edge of $\overline{WR}$	(2)	12		15		ns
t_{DVWH}	$\overline{WR}$ Data setup time	(2)	25		35		ns
t_{WHDX}	$\overline{WR}$ Data Hold time	(2)(3)	4		5		ns
t_{WLWH}	$\overline{WR}$ pulse width	(2)	28		35		ns
t_{WHAX1}	Trailing edge of $\overline{WR}$ to address invalid	(2)	6		8		ns
t_{WHAX2}	Trailing edge of $\overline{WR}$ to DPLD address invalid	(2)(4)	0		0		ns

Table 56. WRITE timing (5 V) (continued)

Symbol	Parameter	Conditions	-70		-90		Unit
			Min	Max	Min	Max	
t_{WHPV}	Trailing edge of $\overline{WR}$ to Port output valid using I/O Port Data register	(2)		27		30	ns
t_{DVMV}	Data valid to Port output valid using macrocell register Preset/Clear	(2)(5)		42		55	ns
t_{AVPV}	Address input valid to address output delay	(6)		20		25	ns
t_{WLMV}	$\overline{WR}$ valid to port output valid using Macrocell register Preset/Clear	(2)(7)		48		55	ns

1. Any input used to select an internal PSD function.
2. $\overline{WR}$ has the same timing as E, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{WRL}$, and $\overline{WRH}$ signals.
3. tWHAX is 6 ns when writing to the output macrocell registers AB and BC.
4. tWHAX2 is the address hold time for DPLD inputs that are used to generate Sector Select signals for internal PSD memory.
5. Assuming WRITE is active before data becomes valid.
6. In multiplexed mode, latched address generated from ADIO delay to address output on any port.
7. Assuming data is stable before active WRITE signal.

Table 57. WRITE timing (3 V)

Symbol	Parameter	Conditions	-90		-12		Unit
			Min	Max	Min	Max	
t_{LVLX}	ALE or AS pulse width		22		24		ns
t_{AVLX}	Address setup time	(1)	7		9		ns
t_{LXAX}	Address hold time	(1)	8		10		ns
t_{AVWL}	Address valid to leading edge of $\overline{WR}$	(1)(2)	15		18		ns
t_{SLWL}	CS valid to leading edge of $\overline{WR}$	(2)	15		18		ns
t_{DVWH}	$\overline{WR}$ Data setup time	(2)	40		45		ns
t_{WHDX}	$\overline{WR}$ Data hold time	(2)(3)	5		8		ns
t_{WLWH}	$\overline{WR}$ pulse width	(2)	40		45		ns
t_{WHAX1}	Trailing edge of $\overline{WR}$ to Address invalid	(2)	8		10		ns
t_{WHAX2}	Trailing edge of $\overline{WR}$ to DPLD Address invalid	(2)(4)	0		0		ns
t_{WHPV}	Trailing edge of $\overline{WR}$ to Port output Valid using I/O Port Data register	(2)		33		33	ns
t_{DVMV}	Data valid to Port output valid using macrocell register Preset/Clear	(2)(5)		65		68	ns

Table 57. WRITE timing (3 V) (continued)

Symbol	Parameter	Conditions	-90		-12		Unit
			Min	Max	Min	Max	
t_{AVPV}	Address input valid to Address output delay	(6)		30		35	ns
t_{WLMV}	$\overline{WR}$ Valid to Port output valid using macrocell register Preset/Clear	(2)(7)		65		70	ns

1. Any input used to select an internal PSD function.
2. $\overline{WR}$ has the same timing as E, $\overline{DS}$, $\overline{LDS}$, $\overline{UDS}$, $\overline{WRL}$, and $\overline{WRH}$ signals.
3. tWHAX is 6 ns when writing to the output macrocell registers AB and BC.
4. tWHAX2 is the address hold time for DPLD inputs that are used to generate Sector Select signals for internal PSD memory.
5. Assuming WRITE is active before data becomes valid.
6. In multiplexed mode, latched address generated from ADIO delay to address output on any port.
7. Assuming data is stable before active WRITE signal.

Figure 37. Input to output Disable/Enable

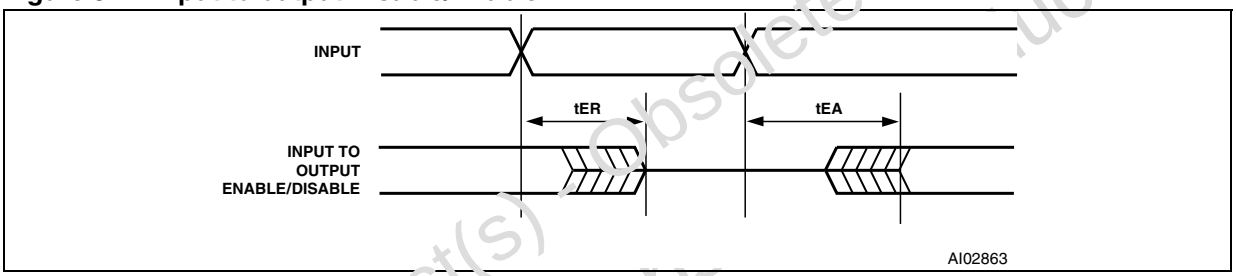


Table 58. PLD Combinatorial timing (5 V)

Symbol	Parameter	Conditions	-70		-90		Fast PT Aloc	Turbo Off	Slew rate (1)	Unit
			Min	Max	Min	Max				
t_{PD}	PLD input Pin/feedback to PLD combinatorial output			20		25	+ 2	+ 12	– 2	ns
t_{ARD}	PLD array delay	Any macrocell		11		16	+ 2			ns

1. Fast Slew Rate output available on Port C and Port F.

Table 59. PLD Combinatorial timing (3 V)

Symbol	Parameter	Conditions	-90		-12		Fast PT Aloc	Turbo Off	Slew rate (1)	Unit
			Min	Max	Min	Max				
t_{PD}	PLD input Pin/Feedback to PLD Combinatorial output			38		43	+ 4	+ 20	– 6	ns
t_{ARD}	PLD Array Delay	Any macrocell		23		27	+ 4			ns

1. Fast Slew Rate output available on Port C and Port F.

Table 60. Power-down timing (5 V)

Symbol	Parameter	Conditions	-70		-90		Unit
			Min	Max	Min	Max	
t_{LVDV}	ALE access time from Power-down			80		90	ns
t_{CLWH}	Maximum delay from APD enabled to internal PDN valid signal	Using CLKIN (PD1)	15 * t_{CLCL} (1)				µs

1. t_{CLCL} is the period of CLKIN (PD1).

Table 61. Power-down timing (3 V)

Symbol	Parameter	Conditions	-90		-12		Unit
			Min	Max	Min	Max	
t_{LVDV}	ALE access time from Power-down			128		135	ns
t_{CLWH}	Maximum delay from APD Enable to internal PDN valid signal	Using CLKIN (PD1)	15 * t_{CLCL} (1)				µs

1. t_{CLCL} is the period of CLKIN (PD1).

Figure 38. Reset ($\overline{\text{RESET}}$) timing

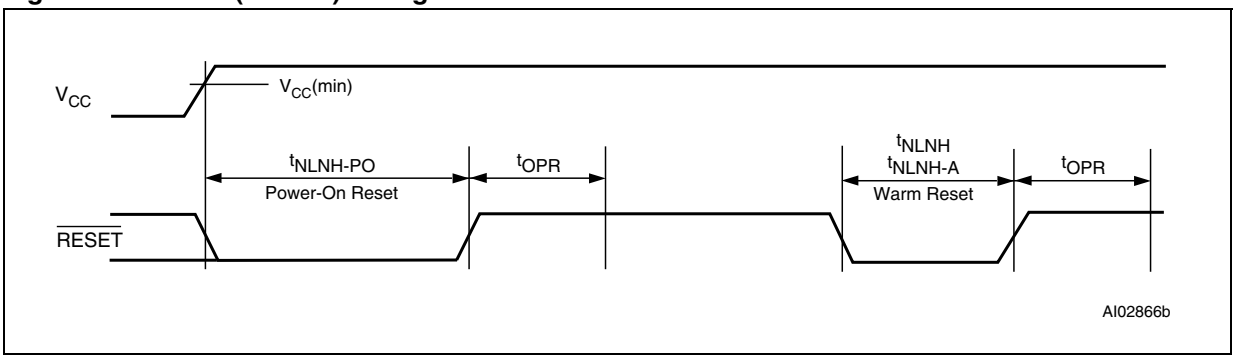


Table 62. Reset ($\overline{\text{RESET}}$) timing (5 V)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{NLNH}	$\overline{\text{RESET}}$ active low time(1)		150		ns
$t_{NLNH-PO}$	Power-on reset active low time		1		ms
t_{NLNH-A}	Warm reset (2)		25		µs
t_{OPR}	$\overline{\text{RESET}}$ high to operational device			120	ns

1. Reset ($\overline{\text{RESET}}$) does not reset Flash memory Program or Erase cycles.
2. Warm reset aborts Flash memory Program or Erase cycles, and puts the device in READ mode.

Table 63. Reset ($\overline{\text{RESET}}$) timing (3 V)

Symbol	Parameter	Conditions	Min	Max	Unit
t_{NLNH}	$\overline{\text{RESET}}$ active low time(1)		300		ns
$t_{NLNH-PO}$	Power-on reset active low time		1		ms
t_{NLNH-A}	Warm reset (2)		25		µs
t_{OPR}	$\overline{\text{RESET}}$ high to operational device			300	ns

1. Reset ($\overline{\text{RESET}}$) does not reset Flash memory Program or Erase cycles.
2. Warm reset aborts Flash memory Program or Erase cycles, and puts the device in READ mode.

Table 64. Program, WRITE and Erase timings (5 V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Flash Program		8.5		s
	Flash Bulk Erase(1) (pre-programmed)		3	30	s
	Flash Bulk Erase (not pre-programmed)		10		s
t_{WHQV3}	Sector Erase (pre-programmed)		1	30	s
t_{WHQV2}	Sector Erase (not pre-programmed)		2.2		s
t_{WHQV1}	Byte Program		14	1200	µs
	Program / Erase Cycles (per Sector)	100,000			cycles
t_{WHWLO}	Sector Erase timeout		100		µs
t_{Q7VQV}	DQ7 Valid to output (DQ7-DQ0) Valid (Data Polling)(2)(3)			30	ns

1. Programmed to all zero before erase.
2. The polling status, DQ7, is valid tQ7VQV time units before the data byte, DQ0-DQ7, is valid for reading.
3. DQ7 is DQ15 for Motorola MCU with 16-bit data bus.

Table 65. Program, WRITE and Erase times (3 V)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Flash Program		8.5		s
	Flash Bulk Erase(1) (pre-programmed)		3	30	s
	Flash Bulk Erase (not pre-programmed)		10		s
t_{WHQV3}	Sector Erase (pre-programmed)		1	30	s
t_{WHQV2}	Sector Erase (not pre-programmed)		2.2		s
t_{WHQV1}	Byte Program		14	1200	µs
	Program / Erase Cycles (per Sector)	100,000			cycles
t_{WHWLO}	Sector Erase timeout		100		µs
t_{Q7VQV}	DQ7 Valid to output (DQ7-DQ0) Valid (Data Polling)(2)(3)			30	ns

1. Programmed to all zero before erase.
2. The polling status, DQ7, is valid tQ7VQV time units before the data byte, DQ0-DQ7, is valid for reading.
3. DQ7 is DQ15 for Motorola MCU with 16-bit data bus.

Figure 39. ISC timing

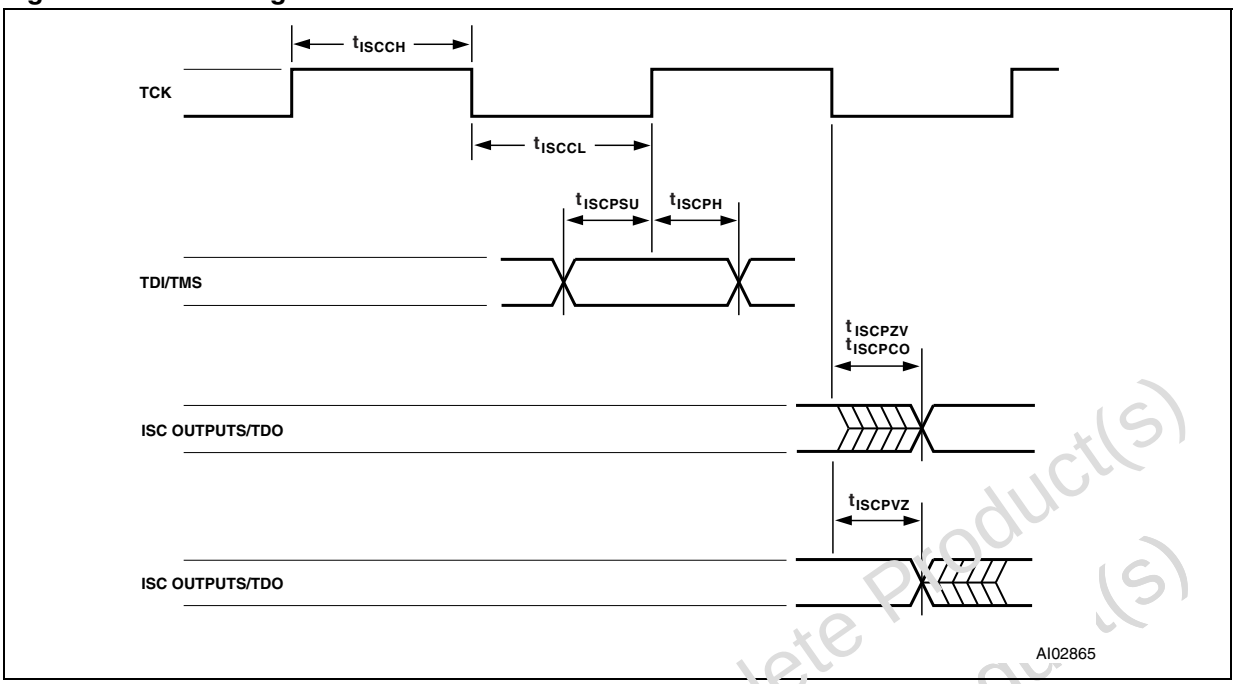


Table 66. ISC timing (5 V)

Symbol	Parameter	Conditions	-70		-90		Unit
			Min	Max	Min	Max	
t_{ISCCF}	Clock (TCK, PC1) frequency (except for PLD)	(1)		20		18	MHz
t_{ISCCH}	Clock (TCK, PC1) high time (except for PLD)		23		26		ns
t_{ISCCL}	Clock (TCK, PC1) low time (except for PLD)		23		26		ns
t_{ISCCFP}	Clock (TCK, PC1) frequency (PLD only)	(2)		2		2	MHz
t_{ISCCHP}	Clock (TCK, PC1) high time (PLD only)		240		240		ns
t_{ISCCLP}	Clock (TCK, PC1) low time (PLD only)		240		240		ns
t_{ISCPSU}	ISC port setup time		6		8		ns
t_{ISCPH}	ISC port hold time		5		5		ns
t_{ISCPCO}	ISC port clock to output			21		23	ns
t_{ISCPZV}	ISC port high-impedance to valid output			21		23	ns
t_{ISCPVZ}	ISC port valid output to high-impedance			21		23	ns

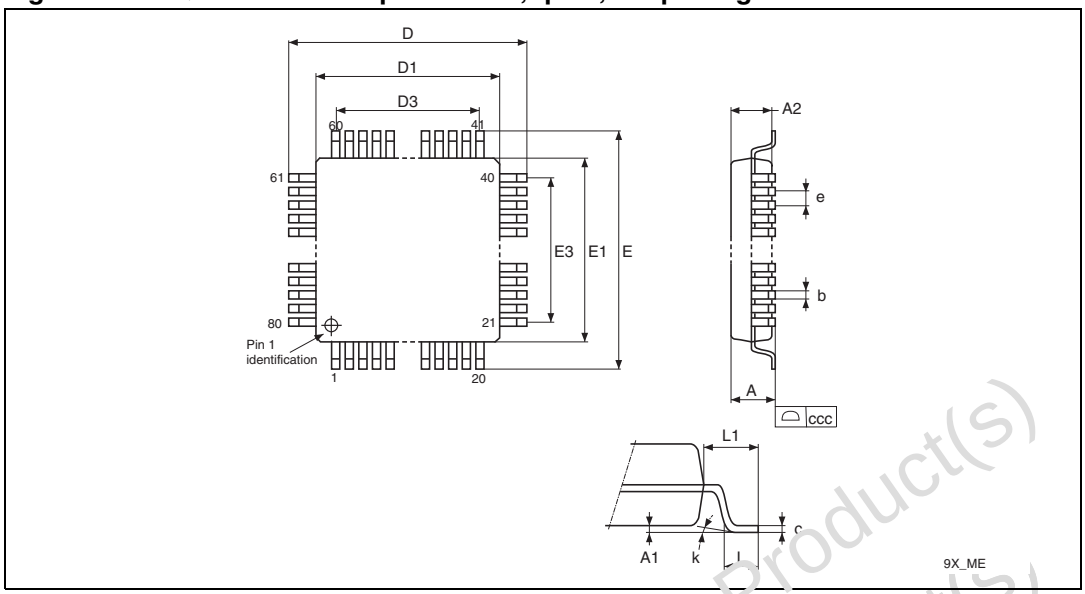
1. For non-PLD Programming, Erase or in ISC by-pass mode.
2. For Program or Erase PLD only.

16 Package mechanical

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance.

ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

Figure 40. LQFP80 - 80-lead plastic thin, quad, flat package outline



1. Drawing is not to scale.

Table 67. LQFP80 - 80-lead plastic thin, quad flat package mechanical data(1)

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A	–	–	1.600	–	–	0.0630
A1	–	0.050	0.150	–	0.0020	0.0060
A2	1.400	1.350	1.450	0.0550	0.0530	0.0570
b	0.220	0.170	0.270	0.0090	0.0070	0.0110
c	–	0.090	0.200	–	0.0040	0.0080
D	14.000	–	–	0.5510	–	–
D1	12.000	–	–	0.4720	–	–
D3	9.500	–	–	0.3740	–	–
E	14.000	–	–	0.5510	–	–
E1	12.000	–	–	0.4720	–	–
E3	9.500	–	–	0.3740	–	–
e	0.500	–	–	0.0200	–	–
L	0.600	0.450	0.750	0.0240	0.0180	0.0300
L1	1.000	–	–	0.0390	–	–
k		0°	7°	3.5	0°	7°
ccc	0.080			–	–	0.003

1. Values in inches are converted from mm and rounded to 4 decimal digits.

17 Part numbering

Table 68. Ordering information scheme

Example: PSD41 3 5 G 2 – 90 U 1 T

Device type

PSD41 = Flash PSD for 16-bit MCUs with simple PSDs

SRAM size

3 = 64 Kbit

Flash memory size

5 = 4 Mbit

I/O count

G = 52 I/O

2nd non-volatile memory

2 = 256 Kbit Flash memory

Operating voltage

blank = V_{CC} = 4.5 to 5.5V

V = V_{CC} = 3.0 to 3.6V

Speed

70 = 70ns

90 = 90ns

12 = 120ns

Package

U = ECOPACK LQFP80

Temperature range

blank = 0 to 70°C (Commercial)

I = –40 to 85°C (Industrial)

Option

T = Tape & Reel Packing

For a list of available options (e.g., Speed, Package) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

Appendix A Pin assignments

Table 69. PSD4235G2 LQFP80

Pin No.	Pin assignments	Pin No.	Pin assignments	Pin No.	Pin assignments	Pin No.	Pin assignments
1	PD2	21	PG0	41	PC0	61	PB0
2	PD3	22	PG1	42	PC1	62	PB1
3	AD0	23	PG2	43	PC2	63	PB2
4	AD1	24	PG3	44	PC3	64	PB3
5	AD2	25	PG4	45	PC4	65	PB4
6	AD3	26	PG5	46	PC5	66	PB5
7	AD4	27	PG6	47	PC6	67	PB6
8	GND	28	PG7	48	PC7	68	PB7
9	V_{CC}	29	V_{CC}	49	GND	69	V_{CC}
10	AD5	30	GND	50	GND	70	GND
11	AD6	31	PF0	51	PA0	71	PE0
12	AD7	32	PF1	52	PA1	72	PE1
13	AD8	33	PF2	53	PA2	73	PE2
14	AD9	34	PF3	54	PA3	74	PE3
15	AD10	35	PF4	55	PA4	75	PE4
16	AD11	36	PF5	56	PA5	76	PE5
17	AD12	37	PF6	57	PA6	77	PE6
18	AD13	38	PF7	58	PA7	78	PE7
19	AD14	39	$\overline{\text{RESET}}$	59	CNTL0	79	PD0
20	AD15	40	CNTL2	60	CNTL1	80	PD1

18 Revision history

Table 70. Document revision history

Date	Revision	Changes
01-May-2000	1	Document written in the WSI format. Initial release
31-Jan-2002	1.1	PSD4135G2: Flash In-System-Programmable Peripherals for 16-Bit MCUs: Front page, and back two pages, in ST format, added to the PDF file Any references to Waferscale, WSI, EasyFLASH and PSDsoft 2000 updated to ST, ST, Flash+PSD and PSDsoft Express
05-May-2009	2	Document reformatted and restructured for consistency with other PSDs datasheet. Added *Table 1: Pin names* and *Figure 2: Logic diagram*. Added 3 V supply voltage PSD4135G2V. Removed SRAM standby mode and backup battery feature. All products are delivered in ECOPACK-compliant packages. Renamed TQFP80 LQFP80, and updated *Table 67: LQFP80 - 80-lead plastic thin, quad, flat package mechanical data*.

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