J108-J110

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N-Channel JFET Switch

INTERSIL

T-35-25

FEATURES
- Low Cost
- Automated Insertion Package
- Low Insertion Loss
- No Offset or Error Voltages Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Fast Switching
- Low Noise

APPLICATIONS
- Analog Switches
- Choppers
- Commutators
- Low-Noise Audio Amplifiers

PIN CONFIGURATION

TO-92

0103-1

5018

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... −25V
Gate Current 50mA
Storage Temperature Range ..... −55°C to +150°C
Operating Temperature Range ..... −55°C to +135°C
Lead Temperature (Soldering, 10sec) ..... +300°C
Power Dissipation 360mW
Derate above 25°C ..... 3.3mW/°C

NOTE: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions		J108			J109			J110			Units
				Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{GSS}	Gate Reverse Current (Note 1)	V_{DS}=0V, V_{GS}=−15V				−3			−3			−3	nA
$V_{GS(off)}$	Gate-Source Cutoff Voltage	V_{DS}=5V, I_D=1μA		−3		−10	−2		−6	−0.5		−4	V
BV_{GSS}	Gate-Source Breakdown Voltage	V_{DS}=0V, I_G=−1μA		−25			−25			−25			
I_{DSS}	Drain Saturation Current (Note 2)	V_{DS}=15V, V_{GS}=0V		80			40			10			mA
$I_{D(off)}$	Drain Cutoff Current (Note 1)	V_{DS}=5V, V_{GS}=−10V				3			3			3	nA
$r_{DS(on)}$	Drain-Source ON Resistance	V_{DS}≤0.1V, V_{GS}=0V				8			12			18	Ω
$C_{dg(off)}$	Drain-Gate OFF Capacitance	V_{DS}=0V, V_{GS}=−10V (Note 3)	f=1MHz			15			15			15	pF
$C_{sg(off)}$	Source-Gate OFF Capacitance					15			15			15	
$C_{dg(on)}$ + $C_{sg(on)}$	Drain-Gate Plus Source-Gate ON Capacitance	V_{DS}=V_{GS}=0 (Note 3)				85			85			85	
$t_{d(on)}$	Turn ON Delay Time	Switching Time Test Conditions (Note 3)			4			4			4		ns
t_r	Rise Time				1			1			1		
$t_{d(off)}$	Turn OFF Delay Time	V_{DD}	J108 1.5V, J109 1.5V, J110 1.5V		6			6			6		
t_f	Fall Time	$V_{GS(off)}$ / R_L	J108 −12V / 150Ω, J109 −7V / 150Ω, J110 −5V / 150Ω		30			30			30		

NOTE 1: Approximately doubles for every 10°C increase in T_A.

2: Pulse test duration = 300μs; duty cycle ≤ 3%.

3: For design reference only, not 100% tested.

NOTE: All typical values have been characterized but are not tested.