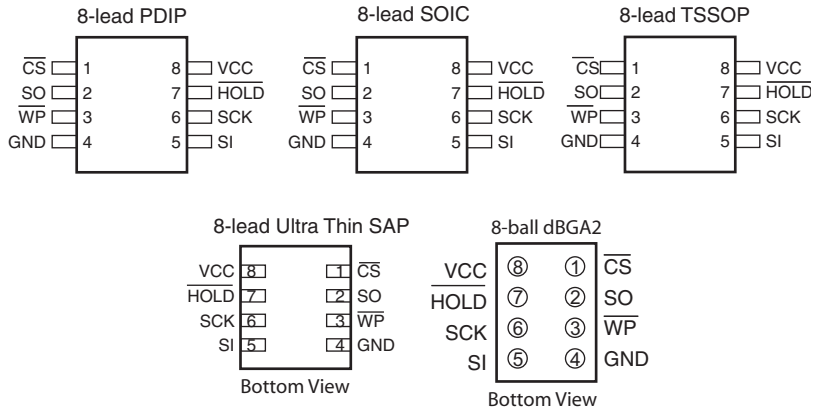
Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
- Data Sheet Describes Mode 0 Operation
- Low-voltage and Standard-voltage Operation
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- 20 MHz Clock Rate (5V)
- 64-byte Page Mode and Byte Write Operation
- Block Write Protection
  - Protect 1/4, 1/2, or Entire Array
- Write Protect ($\overline{WP}$) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-timed Write Cycle (5 ms Max)
- High-reliability
  - Endurance: 1 Million Write Cycles
  - Data Retention: >100 Years
- 8-lead PDIP, 8-lead EIAJ SOIC, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-ball dBGA2 and 8-lead Ultra Thin SAP Packages
- Lead-free/Halogen-free
- Available in Automotive
- Die Sales: Wafer Form, Waffle Pack, and Bumped Die

Description

The AT25128A/256A provides 131,072/262,144 bits of serial electrically-erasable programmable read only memory (EEPROM) organized as 16,384/32,768 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space saving 8-lead PDIP, 8-lead EIAJ SOIC, 8-lead JEDEC SOIC, 8-lead TSSOP, 8-ball dBGA2 and 8-lead SAP packages. In addition, the entire family is available in 2.7V (2.7V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

The AT25128A/256A is enabled through the Chip Select pin ($\overline{CS}$) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate Erase cycle is required before Write.



SPI Serial EEPROMs

128K (16,384 x 8)

256K (32,768 x 8)

AT25128A
AT25256A

Table 0-1. Pin Configurations

Pin Name	Function
$\overline{CS}$	Chip Select
SCK	Serial Data Clock
SI	Serial Data Input
SO	Serial Data Output
GND	Ground
VCC	Power Supply
$\overline{WP}$	Write Protect
$\overline{HOLD}$	Suspends Serial Input
NC	No Connect

Block Write protection is enabled by programming the status register with top ¼, top ½ or entire array of write protection. Separate Program Enable and Program Disable instructions are provided for additional data protection. Hardware data protection is provided via the $\overline{WP}$ pin to protect against inadvertent write attempts to the status register. The $\overline{HOLD}$ pin may be used to suspend any serial communication without resetting the serial sequence.

1. Absolute Maximum Ratings*

Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Voltage on Any Pin with Respect to Ground	–1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 1-1. Block Diagram

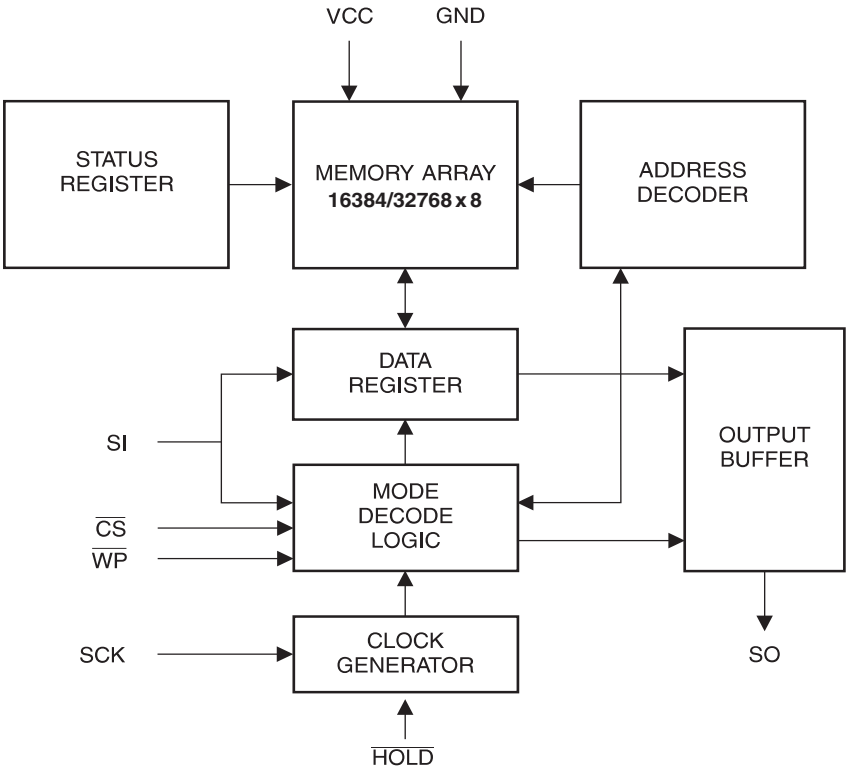


Table 1-1. Pin Capacitance[1]

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +5.0V (unless otherwise noted)

Symbol	Test Conditions	Max	Units	Conditions
C_{OUT}	Output Capacitance (SO)	8	pF	V_{OUT} = 0V
C_{IN}	Input Capacitance ($\overline{CS}$, SCK, SI, $\overline{WP}$, $\overline{HOLD}$)	6	pF	V_{IN} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

Table 1-2. DC Characteristics

Applicable over recommended operating range from T_{AI} = –40°C to +85°C, V_{CC} = +1.8V to +5.5V, T_{AE} = –40°C to +125°C, V_{CC} = +1.8V to +5.5V(unless otherwise noted)

Symbol	Parameter	Test Condition		Min	Typ	Max	Units
V_{CC1}	Supply Voltage			1.8		5.5	V
V_{CC2}	Supply Voltage			2.7		5.5	V
V_{CC3}	Supply Voltage			4.5		5.5	V
I_{CC1}	Supply Current	V_{CC} = 5.0V at 20 MHz, SO = Open, Read			9.0	10.0	mA
I_{CC2}	Supply Current	V_{CC} = 5.0V at 10 MHz, SO = Open, Read, Write			5.0	7.0	mA
I_{CC3}	Supply Current	V_{CC} = 5.0V at 1 MHz, SO = Open, Read, Write			2.2	3.5	mA
I_{SB1}	Standby Current	V_{CC} = 1.8V, $\overline{CS}$ = V_{CC}			0.2	3.0	µA
I_{SB2}	Standby Current	V_{CC} = 2.7V, $\overline{CS}$ = V_{CC}			0.5	3.0	µA
I_{SB3}	Standby Current	V_{CC} = 5.0V, $\overline{CS}$ = V_{CC}			2.0	5.0	µA
I_{IL}	Input Leakage	V_{IN} = 0V to V_{CC}		–3.0		3.0	µA
I_{OL}	Output Leakage	V_{IN} = 0V to V_{CC}, T_{AC} = 0°C to 70°C		–3.0		3.0	µA
V_{IL} (1)	Input Low-voltage			–1.0		V_{CC} x 0.3	V
V_{IH} (1)	Input High-voltage			V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL1}	Output Low-voltage	3.6 ≤ V_{CC} ≤ 5.5V	I_{OL} = 3.0 mA			0.4	V
V_{OH1}	Output High-voltage		I_{OH} = –1.6 mA	V_{CC} –0.8			V
V_{OL2}	Output Low-voltage	1.8V ≤ V_{CC} ≤ 3.6V	I_{OL} = 0.15 mA			0.2	V
V_{OH2}	Output High-voltage		I_{OH} = –100 µA	V_{CC} –0.2			V

Note: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 1-3. AC Characteristics

Applicable over recommended operating range from T_{AI} = –40°C to + 85°C, T_{AE} = –40°C to +125°C, V_{CC} = As Specified, CL = 1 TTL Gate and 30 pF (unless otherwise noted)

Symbol	Parameter	Voltage	Min	Max	Units
f_{SCK}	SCK Clock Frequency	4.5–5.5 2.7–5.5 1.8–5.5	0 0 0	20 10 5	MHz
t_{RI}	Input Rise Time	4.5–5.5 2.7–5.5 1.8–5.5		2 2 2	µs
t_{FI}	Input Fall Time	4.5–5.5 2.7–5.5 1.8–5.5		2 2 2	µs
t_{WH}	SCK High Time	4.5–5.5 2.7–5.5 1.8–5.5	20 40 80		ns
t_{WL}	SCK Low Time	4.5–5.5 2.7–5.5 1.8–5.5	20 40 80		ns
t_{CS}	$\overline{CS}$ High Time	4.5–5.5 2.7–5.5 1.8–5.5	100 100 200		ns
t_{CSS}	$\overline{CS}$ Setup Time	4.5–5.5 2.7–5.5 1.8–5.5	100 100 200		ns
t_{CSH}	$\overline{CS}$ Hold Time	4.5–5.5 2.7–5.5 1.8–5.5	100 100 200		ns
t_{SU}	Data In Setup Time	4.5–5.5 2.7–5.5 1.8–5.5	5 10 20		ns
t_H	Data In Hold Time	4.5–5.5 2.7–5.5 1.8–5.5	5 10 20		ns
t_{HD}	$\overline{Hold}$ Setup Time	4.5–5.5 2.7–5.5 1.8–5.5	5 10 20		ns
t_{CD}	$\overline{Hold}$ Hold Time	4.5–5.5 2.7–5.5 1.8–5.5	5 10 20		ns
t_V	Output Valid	4.5–5.5 2.7–5.5 1.8–5.5	0 0 0	20 40 80	ns
t_{HO}	Output Hold Time	4.5–5.5 2.7–5.5 1.8–5.5	0 0 0		ns
t_{LZ}	$\overline{Hold}$ to Output Low Z	4.5–5.5 2.7–5.5 1.8–5.5	0 0 0	25 50 100	ns

Table 1-3. AC Characteristics (Continued)

Applicable over recommended operating range from T_{AI} = –40°C to + 85°C, T_{AE} = –40°C to +125°C, V_{CC} = As Specified, CL = 1 TTL Gate and 30 pF (unless otherwise noted)

Symbol	Parameter	Voltage	Min	Max	Units
t_{HZ}	$\overline{\text{Hold}}$ to Output High Z	4.5–5.5 2.7–5.5 1.8–5.5		25 50 100	ns
t_{DIS}	Output Disable Time	4.5–5.5 2.7–5.5 1.8–5.5		25 50 100	ns
t_{WC}	Write Cycle Time	4.5–5.5 2.7–5.5 1.8–5.5		5 5 5	ms
Endurance[1]	5.0V, 25°C, Page Mode		1M		Write Cycles

Notes: 1. This parameter is characterized and is not 100% tested. Contact Atmel for further information.

5. AT25128A Ordering Information[1]

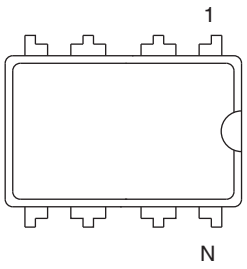
Ordering Code	Package	Operation Range
AT25128A-10PU-2.7[2]	8P3	Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C)
AT25128A-10PU-1.8[2]	8P3	
AT25128AN-10SU-2.7[2]	8S1	
AT25128AN-10SU-1.8[2]	8S1	
AT25128AW-10SU-2.7[2]	8S2	
AT25128AW-10SU-1.8[2]	8S2	
AT25128A-10TU-2.7[2]	8A2	
AT25128A-10TU-1.8[2]	8A2	
AT25128AU2-10UU-1.8[2]	8U2-1	
AT25128AY7-10YH-1.8[2]	8Y7	
AT25128A-W1.8-11[3]	Die Sale	Industrial Temperature (–40°C to 85°C)

Notes:
1. For 2.7V devices used in the 4.5V to 5.5V range, please refer to performance values in the AC and DC Characteristics tables.
2. “U” designates Green package + RoHS compliant.
3. Available in waffle pack and wafer form; order as SL788 for wafer form. Bumped die available upon request. Please Contact Serial Interface Marketing.

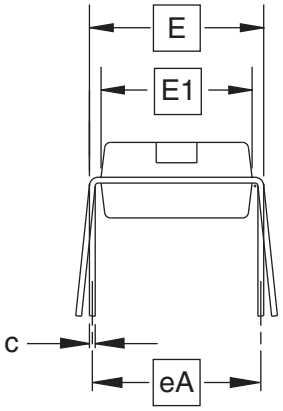
Package Type	
8P3	8-lead, 0.300" Wide, Plastic Dual In-line Package (PDIP)
8S1	8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC)
8S2	8-lead, 0.200" Wide, Plastic Gull Wing Small Outline Package (EIAJ SOIC)
8U2-1	8-ball, die Ball Grid Array Package (dBGA2)
8A2	8-lead, 4.4 mm Body, Thin Shrink Small Outline Package (TSSOP)
8Y7	8-lead, 6.00 mm x 4.90 mm Body, Ultra Thin, Dual Footprint, Non-leaded, Small Array Package (SAP)
Options	
–2.7	Low-voltage (2.7V to 5.5V)
–1.8	Low-voltage (1.8V to 5.5V)

6. Packaging Information

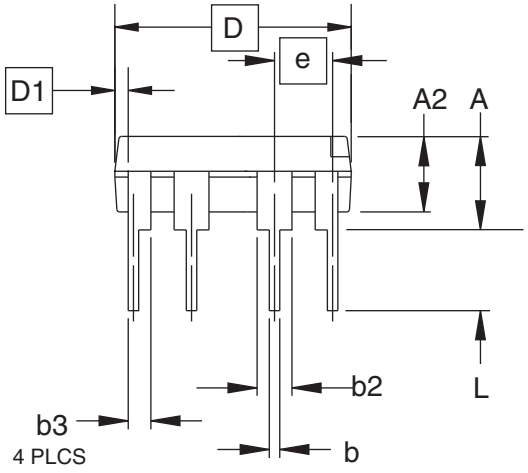
8P3 – PDIP



Top View



End View



Side View

COMMON DIMENSIONS
(Unit of Measure = inches)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	0.210	2
A2	0.115	0.130	0.195	
b	0.014	0.018	0.022	5
b2	0.045	0.060	0.070	6
b3	0.030	0.039	0.045	6
c	0.008	0.010	0.014	
D	0.355	0.365	0.400	3
D1	0.005	–	–	3
E	0.300	0.310	0.325	4
E1	0.240	0.250	0.280	3
e	0.100 BSC			
eA	0.300 BSC			4
L	0.115	0.130	0.150	2

Notes:
1. This drawing is for general information only; refer to JEDEC Drawing MS-001, Variation BA, for additional information.
2. Dimensions A and L are measured with the package seated in JEDEC seating plane Gauge GS-3.
3. D, D1 and E1 dimensions do not include mold Flash or protrusions. Mold Flash or protrusions shall not exceed 0.010 inch.
4. E and eA measured with the leads constrained to be perpendicular to datum.
5. Pointed or rounded lead tips are preferred to ease insertion.
6. b2 and b3 maximum dimensions do not include Dambar protrusions. Dambar protrusions shall not exceed 0.010 (0.25 mm).

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead, 0.300" Wide Body, Plastic Dual In-line Package (PDIP)	8P3	B