



TPS730 Low-Noise, High PSRR, RF, 200-mA Low-Dropout Linear Regulators

1 Features

- 200-mA RF Low-Dropout Regulator With Enable
- Available in Fixed Voltages from 1.8 V to 3.3 V and Adjustable Voltages (1.22 V to 5.5 V)
- High PSRR (68 dB at 100 Hz)
- Low Noise (33 μV_{RMS} , TPS73018)
- Fast Start-Up Time (50 μs)
- Stable With a 2.2- μF Ceramic Capacitor
- Excellent Load/Line Transient Response
- Very Low Dropout Voltage (120 mV at 200 mA)
- 5- and 6-Pin SOT-23 (DBV), and Wafer Chip Scale (YZQ) Packages

2 Applications

- RF: VCOs, Receivers, ADCs
- Audio
- Cellular and Cordless Telephones
- Bluetooth®, Wireless LAN
- Handheld Organizers, PDAs

3 Description

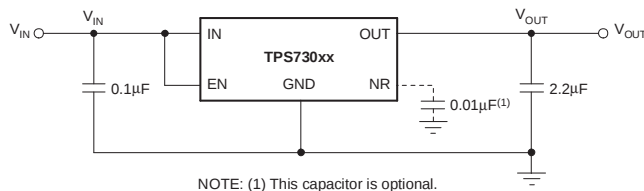
The TPS730 family of low-dropout (LDO) low-power linear voltage regulators features high power-supply rejection ratio (PSRR), low noise, fast start-up, and excellent line and load transient responses in a small SOT-23 package. NanoStar™ packaging gives an ultrasmall footprint as well as an ultralow profile and package weight, making it ideal for portable applications such as handsets and PDAs. Each device in the family is stable, with a small, 2.2- μF ceramic capacitor on the output. The TPS730 family uses an advanced, proprietary BiCMOS fabrication process to yield low dropout voltages (for example, 120 mV at 200 mA, TPS73030). Each device achieves fast start-up times (approximately 50 μs with a 0.001- μF bypass capacitor) while consuming low quiescent current (170 μA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA . The TPS73018 exhibits approximately 33 μV_{RMS} of output voltage noise at 1.8 V output with a 0.01- μF bypass capacitor. Applications with analog components that are noise-sensitive, such as portable RF electronics, benefit from the high PSRR and low-noise features as well as the fast response time.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS730	SOT-23 (5)	2.90 mm × 1.60 mm
	SOT-23 (6)	2.90 mm × 1.60 mm
	DSBGA (5)	1.35 mm × 1.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



Ripple Rejection vs Frequency

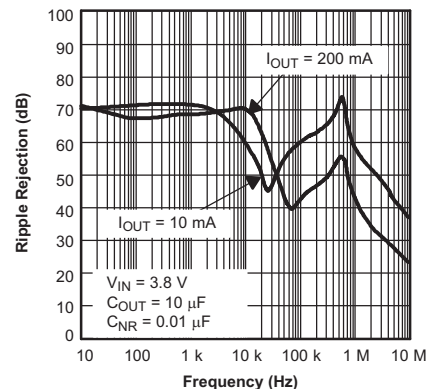


Table of Contents

1 Features	1	8.1 Application Information.....	11
2 Applications	1	8.2 Typical Application	13
3 Description	1	8.3 Do's and Don'ts.....	14
4 Revision History	2	9 Power Supply Recommendations	15
5 Pin Configuration and Functions	3	10 Layout	15
6 Specifications	4	10.1 Layout Guidelines	15
6.1 Absolute Maximum Ratings	4	10.2 Layout Example	15
6.2 ESD Ratings	4	10.3 Thermal Considerations	16
6.3 Recommended Operating Conditions.....	4	10.4 Power Dissipation	16
6.4 Thermal Information	4	11 Device and Documentation Support	18
6.5 Electrical Characteristics	5	11.1 Device Support.....	18
6.6 Typical Characteristics	6	11.2 Documentation Support	18
7 Detailed Description	9	11.3 Trademarks	18
7.1 Overview	9	11.4 Electrostatic Discharge Caution.....	18
7.2 Functional Block Diagrams	9	11.5 Glossary	18
7.3 Feature Description.....	10	12 Mechanical, Packaging, and Orderable Information	18
7.4 Device Functional Modes.....	10	12.1 TPS730YZQ Nanostar™ Wafer Chip Scale Information	19
8 Application and Implementation	11		

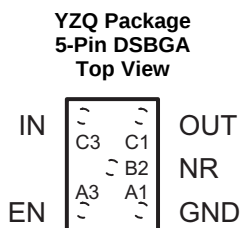
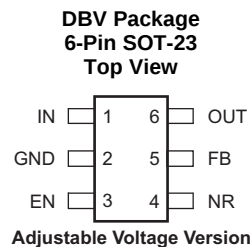
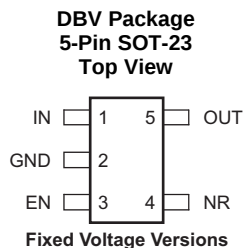
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (February, 2011) to Revision J	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section	1
• Changed fourth bullet of <i>Features</i> list to <i>low noise</i>	1
• Changed front-page figure	1
• Added <i>Pin Configuration and Functions</i> section	3
• Changed "free-air temperature" to "junction temperature" in <i>Absolute Maximum Ratings</i> condition statement	4
• Deleted <i>Dissipation Ratings</i> table; added <i>Thermal Information</i> table	4
• Added condition statement to <i>Typical Characteristics</i>	6
• Moved <i>Ordering Information</i> to <i>Device Nomenclature</i> section	18

Changes from Revision H (October, 2007) to Revision I	Page
• Corrected units in y-axis of <i>Figure 5</i>	6

5 Pin Configuration and Functions



Pin Functions

PIN			I/O	DESCRIPTION
NAME	NO.			
	SOT-23	DSBGA		
EN	3	A3	I	Enable pin. Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. EN can be connected to IN if not used.
FB	5	N/A	I	Feedback pin. This terminal is the feedback input pin for the adjustable device. Fixed-voltage versions in the DBV package do not have this pin.
GND	2	A1	—	Regulator ground.
IN	1	C3	I	Input to the device.
OUT	6	C1	O	Output of the regulator.
NR	4	B2	—	Noise Reduction pin. Connecting an external capacitor to this pin filters noise generated by the internal bandgap. This configuration improves power-supply rejection and reduces output noise.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Voltage	Input range, V _{IN}		−0.3	6	V
	Enable range, V _{EN}		−0.3	6	
	Output range, V _{OUT}		−0.3	6	
Current	Peak output, I _{OUT(max)}		Internally limited		
Continuous total power dissipation			See Thermal Information		
Temperature	Junction, T _J	DBV package	−40	150	°C
		YZQ package	−40	125	
	Storage, T _{stg}		−65	150	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾		±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	2.7		5.5	V
V_{EN}	Enable supply voltage	0		V_{IN}	V
V_{OUT}	Output voltage	V_{FB}		5	V
I_{OUT}	Output current	0		200	mA
T_J	Operating junction temperature	−40		125	°C
C_{IN}	Input capacitor	0.1	1		μF
C_{OUT}	Output capacitor	2.2 ⁽¹⁾	10		μF
C_{NR}	Noise reduction capacitor	0	10		nF
C_{FF}	Feed-forward capacitor		15		pF
R_2	Lower feedback resistor		30.1		kΩ

- (1) If C_{FF} is not used or $V_{OUT(nom)} < 1.8$ V, the minimum recommended $C_{OUT} = 4.7$ μF.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS73001		UNIT
		DBV (SOT-23)	YZQ (DSBGA)	
		6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	225.1	178.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.4	1.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	54.7	62.1	
Ψ_{JT}	Junction-to-top characterization parameter	3.3	0.9	
Ψ_{JB}	Junction-to-board characterization parameter	53.8	62.1	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

6.5 Electrical Characteristics

Over recommended operating temperature range $T_J = -40$ to $+125^\circ\text{C}$, $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}^{(1)}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$ (unless otherwise noted). Typical values are at 25°C .

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IN}	Input voltage range ⁽¹⁾			2.7		5.5	V
I _{OUT}	Continuous output current			0		200	mA
V _{FB}	Internal reference (TPS73001)			1.201	1.225	1.25	V
V _{OUT}	Output voltage range	TPS73001		V _{FB}	5.5 – V _{DO}		V
	Output voltage accuracy		0 μA ≤ I _{OUT} ≤ 200 mA, 2.75 V ≤ V _{IN} ≤ 5.5 V	–2%	V _{OUT(nom)}	2%	V
ΔV _{OUT(ΔVIN)}	Line regulation ⁽¹⁾		V _{OUT} + 1 V ≤ V _{IN} ≤ 5.5 V	0.05			%/V
ΔV _{OUT(ΔIOUT)}	Load regulation		0 μA ≤ I _{OUT} ≤ 200 mA, T _J = 25°C	5			mV
V _{DO}	Dropout voltage ⁽²⁾ (V _{IN} = V _{OUT(nom)} – 0.1 V)		I _{OUT} = 200 mA		120	210	mV
I _{CL}	Output current limit		V _{OUT} = 0 V	285		600	mA
I _{GND}	Ground pin current		0 μA < I _{OUT} < 200 mA		170	250	μA
I _{SHUTDOWN}	Shutdown current ⁽³⁾		V _{EN} = 0 V, 2.7 V ≤ V _{IN} ≤ 5.5 V		0.07	1	μA
I _{FB}	FB pin current		V _{FB} = 1.8 V			1	μA
PSRR	Power-supply rejection ratio	TPS73028	f = 100 Hz, I _{OUT} = 200 mA, T _J = 25°C		68		dB
V _n	Output noise voltage	TPS73018	BW = 200 Hz to 100 kHz, I _{OUT} = 200 mA, C _{NR} = 0.01 μF		33		μV _{RMS}
t _{STR}	Start-up time	TPS73018	R _L = 14 Ω, C _{OUT} = 1 μF, C _{NR} = 0.001 μF		50		μs
V _{EN(high)}	High-level enable input voltage		2.7 V ≤ V _{IN} ≤ 5.5 V	1.7		V _{IN}	V
V _{EN(low)}	Low-level enable input voltage		2.7 V ≤ V _{IN} ≤ 5.5 V	0		0.7	V
I _{EN}	EN pin current		V _{EN} = 0 V	–1		1	μA
UVLO			Threshold, V _{CC} rising	2.25		2.65	V
			Hysteresis		100		mV

(1) Minimum V_{IN} is 2.7 V or $V_{OUT} + V_{DO}$, whichever is greater.

(2) Dropout is not measured for the TPS73018 and TPS73025 since minimum $V_{IN} = 2.7\text{ V}$.

(3) For adjustable versions, this applies only after V_{IN} is applied; then V_{EN} transitions high to low.

6.6 Typical Characteristics

Over recommended operating temperature range $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{\text{EN}} = V_{\text{IN}}$, $V_{\text{IN}} = V_{\text{OUT(nom)}} + 1\text{ V}$, $I_{\text{OUT}} = 1\text{ mA}$, $C_{\text{OUT}} = 10\text{ }\mu\text{F}$, $C_{\text{NR}} = 0.01\text{ }\mu\text{F}$, $V_{\text{OUT(nom)}} = 2.8\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$.

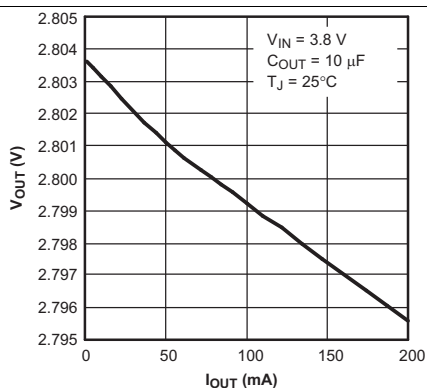


Figure 1. TPS73028 Output Voltage vs Output Current

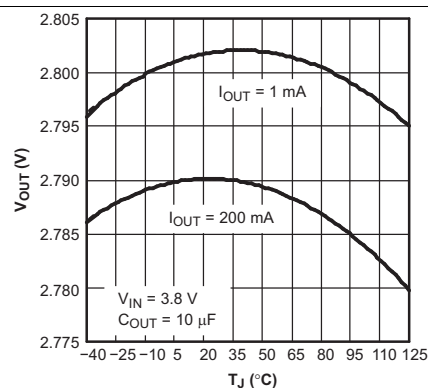


Figure 2. TPS73028 Output Voltage vs Junction Temperature

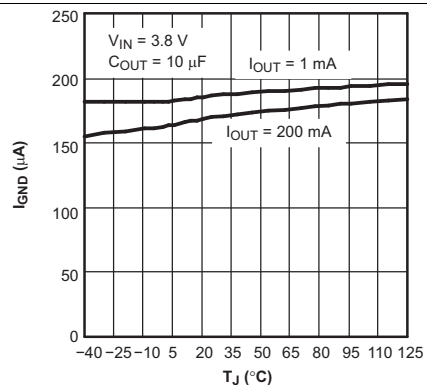


Figure 3. TPS73028 Ground Current vs Junction Temperature

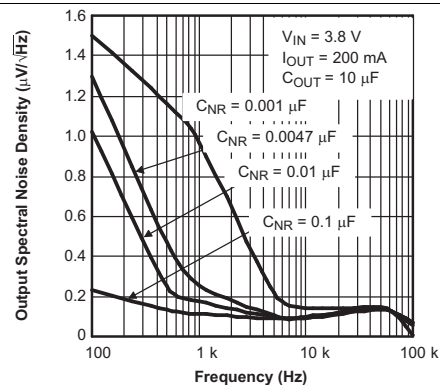


Figure 4. TPS73028 Output Spectral Noise Density vs Frequency

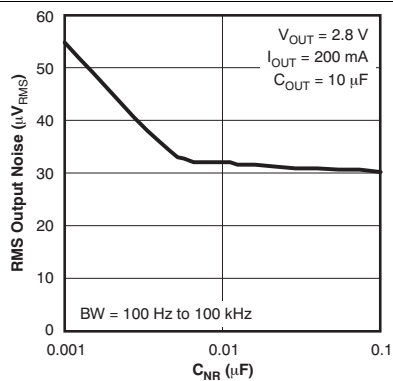


Figure 5. Root Mean Square Output Noise vs C_{NR}

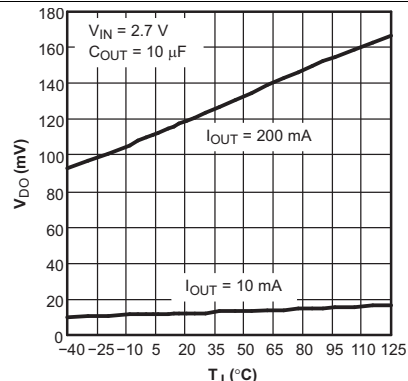


Figure 6. TPS73028 Dropout Voltage vs Junction Temperature

Typical Characteristics (continued)

Over recommended operating temperature range $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, $V_{OUT(nom)} = 2.8\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$.

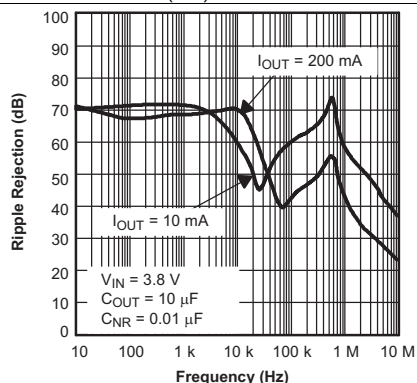


Figure 7. TPS73028 Ripple Rejection vs Frequency

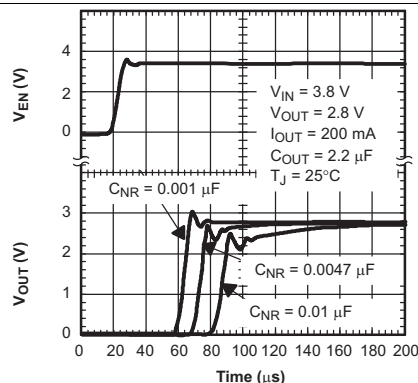


Figure 8. TPS73028 Output Voltage, Enable Voltage vs Time (Start-Up)

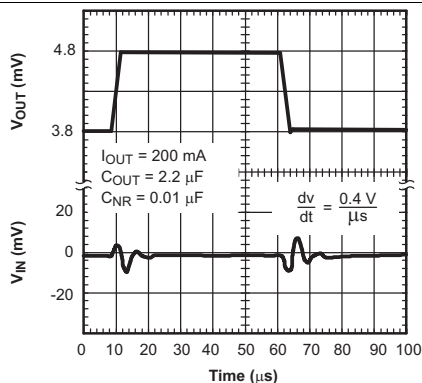


Figure 9. TPS73028 Line Transient Response

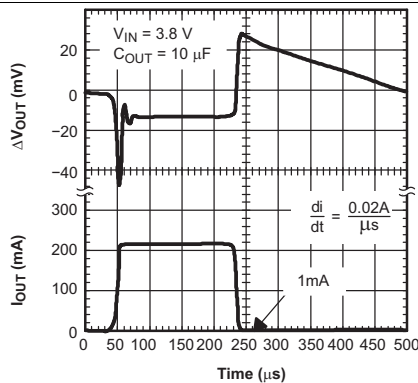


Figure 10. TPS73028 Load Transient Response

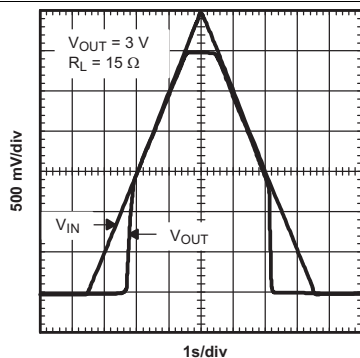


Figure 11. Power Up and Power Down

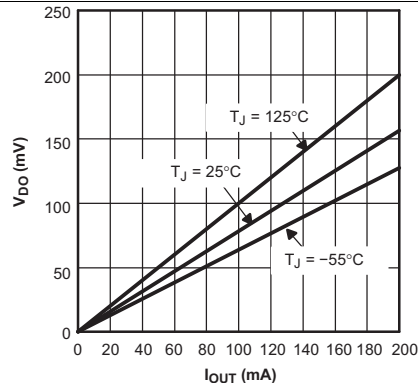


Figure 12. Dropout Voltage vs Output Current

Typical Characteristics (continued)

Over recommended operating temperature range $T_J = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{EN} = V_{IN}$, $V_{IN} = V_{OUT(nom)} + 1\text{ V}$, $I_{OUT} = 1\text{ mA}$, $C_{OUT} = 10\text{ }\mu\text{F}$, $C_{NR} = 0.01\text{ }\mu\text{F}$, $V_{OUT(nom)} = 2.8\text{ V}$ (unless otherwise noted). Typical values are at $T_J = 25^{\circ}\text{C}$.

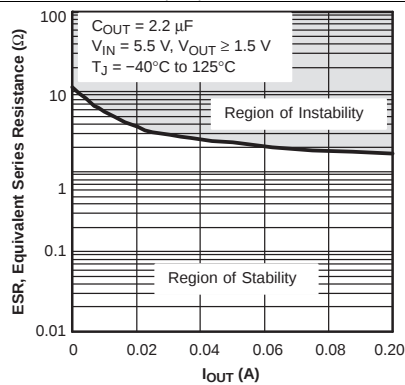


Figure 13. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

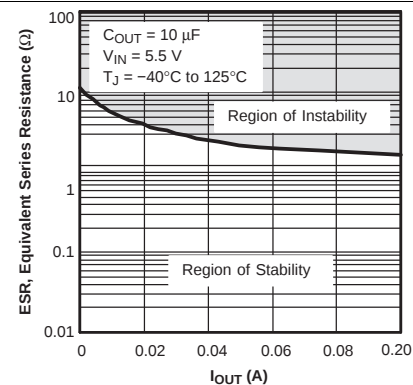


Figure 14. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

7 Detailed Description

7.1 Overview

The TPS730 family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive, battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultra-low output noise, low quiescent current (170 μA typically), and enable-input to reduce supply currents to less than 1 μA when the regulator is turned off.

7.2 Functional Block Diagrams

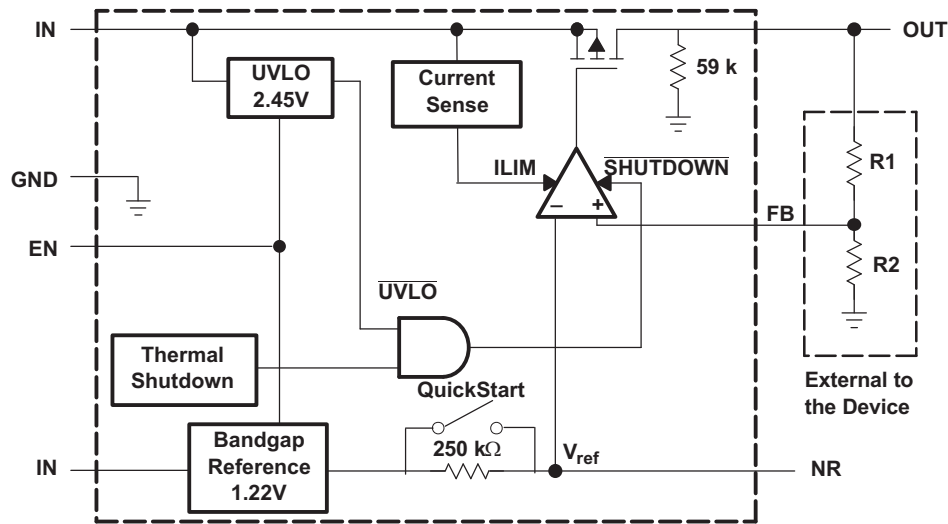


Figure 15. TPS730 Block Diagram (Adjustable-Voltage Version)

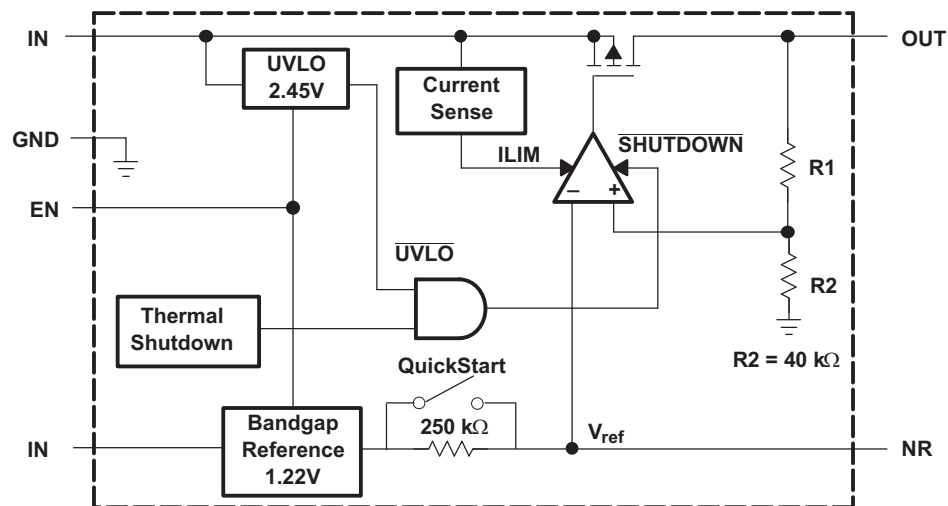


Figure 16. TPS730 Block Diagram (Fixed-Voltage Versions)

7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The TPS730 uses an undervoltage lockout (UVLO) circuit that disables the output until the input voltage is greater than the rising UVLO voltage. This circuit ensures that the device does not exhibit any unpredictable behavior when the supply voltage is lower than the operational range of the internal circuitry, $V_{IN(min)}$.

7.3.2 Shutdown

The enable pin (EN) is active high. Enable the device by forcing the EN pin to exceed $V_{EN(high)}$ (1.7 V, minimum). Turn off the device by forcing the EN pin to drop below 0.7 V. If shutdown capability is not required, connect EN to IN.

7.3.3 Foldback Current Limit

The TPS730 features internal current limiting and thermal protection. During normal operation, the TPS730 limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, do not exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage is greater than $V_{EN(min)}$.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device is in the linear region and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.
- The input voltage is less than $UVLO_{falling}$.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN(high)}$	$I_{OUT} < I_{LIM}$	$T_J < 125^{\circ}C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN(high)}$	—	$T_J < 125^{\circ}C$
Disabled mode (any true condition disables the device)	$V_{IN} < UVLO_{falling}$	$V_{EN} < V_{EN(low)}$	—	$T_J > 165^{\circ}C^{(1)}$

(1) Approximate value for thermal shutdown.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS730 family of low-dropout (LDO) regulators has been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultra-low output noise, low quiescent current (170 μ A typically), and enable-input to reduce supply currents to less than 1 μ A when the regulator is turned off.

8.1.1 Adjustable Operation

The output voltage of the TPS73001 adjustable regulator is programmed using an external resistor divider as shown in [Figure 17](#). The output voltage is calculated using [Equation 1](#):

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2} \right)$$

Where:

- $V_{REF} = 1.225$ V typical (the internal reference voltage) (1)

Resistors R_1 and R_2 should be chosen for approximately 50- μ A divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistors values can cause accuracy issues and other problems. The recommended design procedure is to choose $R_2 = 30.1$ k Ω to set the divider current at 50 μ A, $C_1 = 15$ pF for stability, and then calculate R_1 using [Equation 2](#):

$$R_1 = \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \times R_2$$
 (2)

To improve the stability of the adjustable version, TI suggests placing a small compensation capacitor between OUT and FB. For output voltages < 1.8 V, the value of this capacitor should be 100 pF. For output voltages > 1.8 V, use [Equation 3](#) to calculate the approximate value of this capacitor.

$$C_1 = \frac{(3 \times 10^{-7}) \times (R_1 + R_2)}{(R_1 \times R_2)}$$
 (3)

[Figure 17](#) shows the suggested value of this capacitor for several resistor ratios. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage < 1.8 V is chosen, then the minimum recommended output capacitor is 4.7 μ F instead of 2.2 μ F.

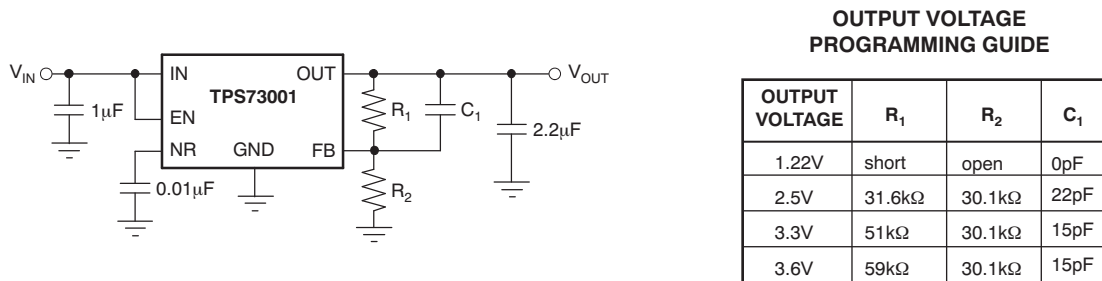


Figure 17. TPS73001 Adjustable LDO Regulator Programming

Application Information (continued)

8.1.2 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors should be used for the input, output, noise reduction, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, while ceramic X5R capacitors are more cost-effective and are available in higher values.

8.1.3 Input and Output Capacitor Requirements

A 0.1- μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS730, is required for stability and improves transient response, noise rejection, and ripple rejection. A higher-value input capacitor may be necessary if large, fast-rise-time load transients are anticipated or the device is located several inches from the power source.

Like most low-dropout regulators, the TPS730 requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 2.2 μF . Any 2.2- μF or larger ceramic capacitor is suitable, provided the capacitance does not vary significantly over temperature. If load current is not expected to exceed 100 mA, a 1- μF ceramic capacitor can be used. If a feed-forward capacitor is not used (such as in a unity-gain configuration) or if an output voltage less than 1.8 V is chosen, then the minimum recommended output capacitor is 4.7 μF instead of 2.2 μF . [Table 2](#) lists the recommended output capacitor sizes for several common configurations.

Table 2. Output Capacitor Sizing

CONDITION	C _{OUT} (μF)
$V_{\text{OUT}} < 1.8 \text{ V}$ or $C_{\text{FF}} = 0 \text{ nF}$	4.7
$V_{\text{OUT}} > 1.8 \text{ V}$, $I_{\text{OUT}} > 100 \text{ mA}$	2.2
$V_{\text{OUT}} > 1.8 \text{ V}$, $I_{\text{OUT}} < 100 \text{ mA}$	1

8.1.4 Noise Reduction and Feed-Forward Capacitor Requirements

The internal voltage reference is a key source of noise in an LDO regulator. The TPS730 has an NR pin which is connected to the voltage reference through a 250-k Ω internal resistor. The 250-k Ω internal resistor, in conjunction with an external bypass capacitor connected to the NR pin, creates a low-pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the NR pin must be at a minimum, because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current. The bypass capacitor should be no more than 0.1 μF to ensure that it is fully charged during the quick-start time provided by the internal switch shown in the [Functional Block Diagram](#) section.

As an example, the TPS73018 exhibits only 33 μV_{RMS} of output voltage noise using a 0.01- μF ceramic bypass capacitor and a 2.2- μF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the NR pin that is created by the internal 250-k Ω resistor and external capacitor.

A feed-forward capacitor is recommended to improve the stability of the device. If $R_2 = 30.1 \text{ k}\Omega$, set C_1 to 15 pF for optimal performance. For voltages less than 1.8 V, the value of this capacitor should be 100 pF. For voltages greater than 1.8 V, the approximate value of this capacitor can be calculated as shown in [Equation 3](#).

8.1.5 Reverse Current Operation

The TPS730 PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (for example, during power-down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate. If extended reverse voltage operation is anticipated, external limiting to 5% of the rated output current is recommended.

8.2 Typical Application

A typical application circuit is shown in [Figure 18](#).

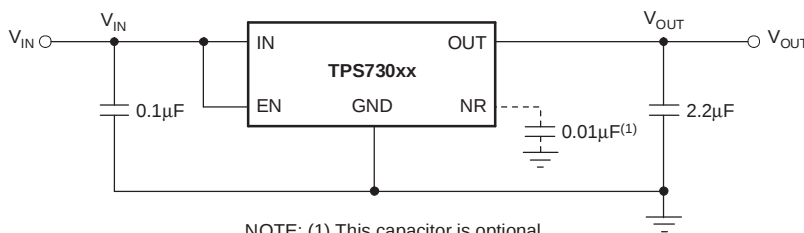


Figure 18. Typical Application Circuit

8.2.1 Design Requirements

[Table 3](#) lists the design requirements.

Table 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	4.2 V to 3 V (Lithium Ion battery)
Output voltage	1.8 V, $\pm 1\%$
DC output current	10 mA
Peak output current	75 mA
Maximum ambient temperature	65°C

8.2.2 Detailed Design Procedure

Pick the desired output voltage option. An input capacitor of 0.1 μF is used as the battery is connected to the input through a via and a short 10-mil (0.01-in) trace. An output capacitor of 10 μF is used to provide optimal response time for the load transient. Verify that the maximum junction temperature is not exceed by referring to [Figure 24](#).

8.2.3 Application Curves

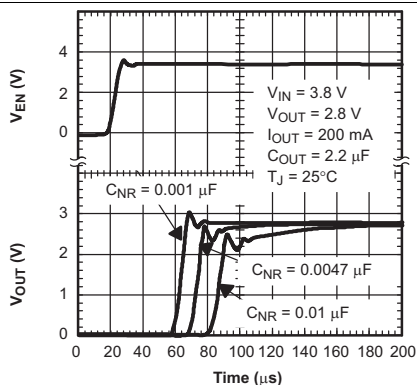


Figure 19. TPS73028 Output Voltage, Enable Voltage vs Time (Start-Up)

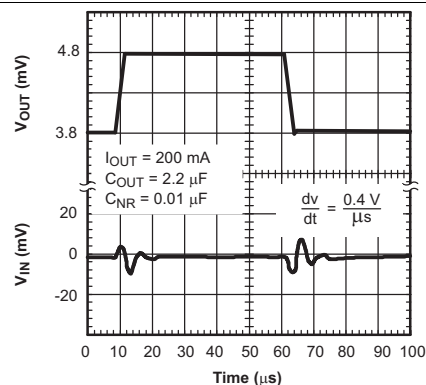
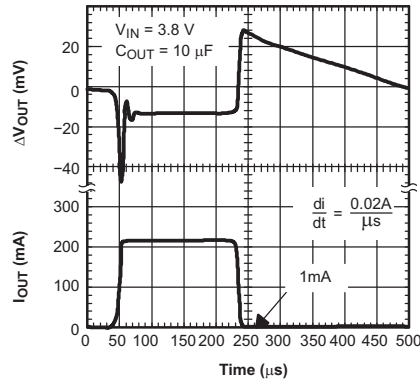
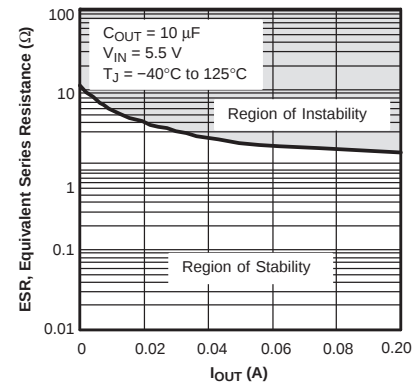


Figure 20. TPS73028 Line Transient Response


Figure 21. TPS73028 Load Transient Response

Figure 22. Typical Regions of Stability Equivalent Series Resistance (ESR) vs Output Current

8.3 Do's and Don'ts

Do place at least one, low-ESR, 2.2-μF capacitor as close as possible between the OUT pin of the regulator and the GND pin.

Do place at least one, low-ESR, 0.1-μF capacitor as close as possible between the IN pin of the regulator and the GND pin.

Do provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the Enable (EN) pin.

Do not resistively or inductively load the NR pin.

Do not let the output voltage get more than 0.3 V above the input voltage.

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 2.7 V to 5.5 V. The input voltage range must provide adequate headroom in order for the device to have a regulated output. This input supply must be well-regulated and stable. A 0.1- μ F input capacitor is required for stability; if the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN} , C_{OUT} , $C_{NR/SS}$, C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits may impact system performance negatively, and even cause instability.

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC measurements like PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

10.2 Layout Example

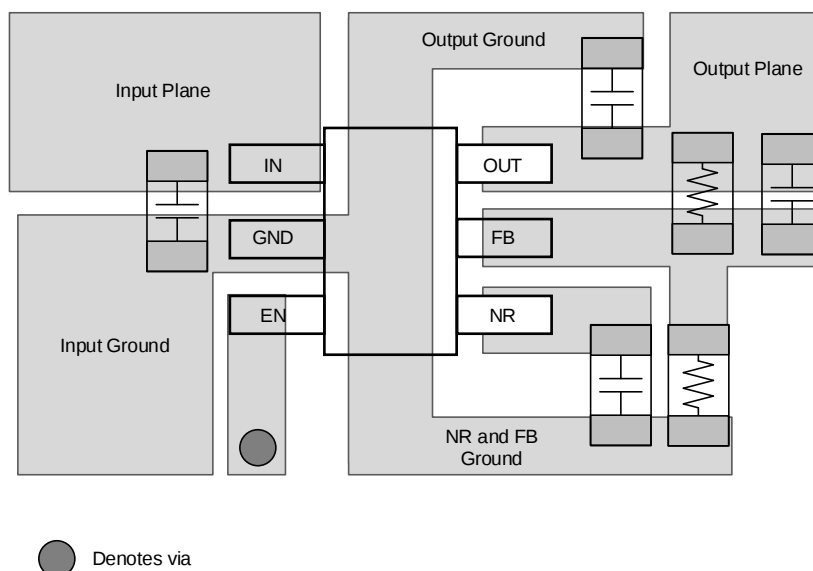


Figure 23. Layout Example (DBV Package)

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 165°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature must be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions.

The TPS730 internal protection circuitry is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS730 into thermal shutdown degrades device reliability.

10.4 Power Dissipation

Specified regulator operation is assured to a junction temperature of +125°C; the maximum junction temperature should be restricted to +125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D , which must be less than or equal to $P_{D(max)}$.

The maximum power dissipation limit is determined using [Equation 4](#):

$$P_{D(max)} = \frac{T_{Jmax} - T_A}{R_{\theta JA}}$$

Where:

- T_{Jmax} is the maximum allowable junction temperature.
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package (see the [Thermal Information](#) table).
- T_A is the ambient temperature.

(4)

The regulator dissipation is calculated using [Equation 5](#):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$$

(5)

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

[Figure 24](#) shows the maximum ambient temperature versus the power dissipation of the TPS730. This figure assumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to ensure the TPS730 does not operate above a junction temperature of 125°C.

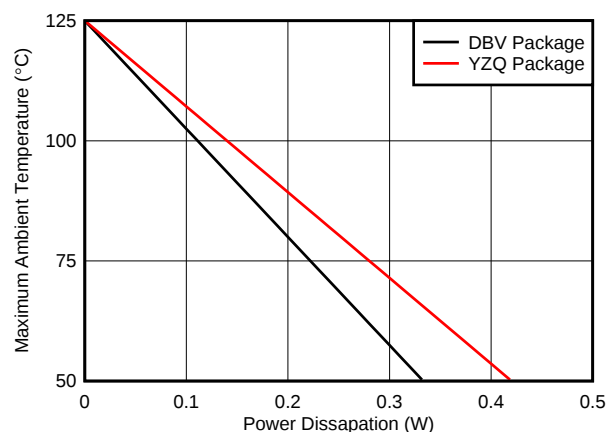


Figure 24. Maximum Ambient Temperature vs Power Dissipation

Power Dissipation (continued)

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB} , shown in the [Thermal Information](#) table. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with [Equation 6](#).

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \cdot P_D$$

$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \cdot P_D$$

where

- P_D is the power dissipation shown by [Equation 5](#),
- T_T is the temperature at the center-top of the IC package,
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface*. (6)

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B , see the application note *Using New Thermal Metrics* ([SBVA025](#)), available for download at www.ti.com.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS730 is available through the product folders under *Tools & Software*.

11.1.2 Device Nomenclature

Table 4. Ordering Information⁽¹⁾⁽²⁾

PRODUCT	V _{OUT}
TPS730xyyyz	XX(X) is the nominal output voltage (for example, 28 = 2.8 V; 285 = 2.85 V; 01 = adjustable version). YYY is the package designator. Z is the package quantity. R is for reel (3000 pieces), T is for tape (250 pieces).

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.
- (2) Output voltages from 1.2 V to 4.8 V in 50-mV increments are available. Contact the factory for details and availability.

11.2 Documentation Support

11.2.1 Related Documentation

- *Using New Thermal Metrics*, [SBVA025](#)
- *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, [SBVA042](#)

11.3 Trademarks

NanoStar is a trademark of Texas Instruments.
 Bluetooth is a registered trademark of Bluetooth Sig, Inc.
 All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

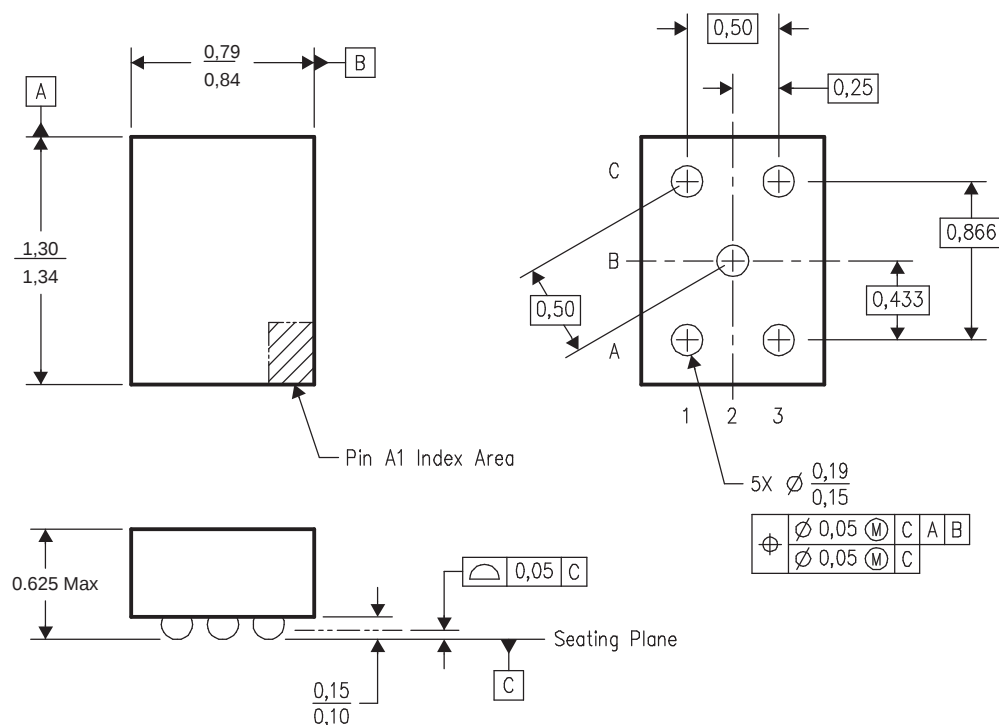
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 TPS730YZQ Nanostar™ Wafer Chip Scale Information



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. NanoStar™ package configuration.
 D. This package is tin-lead (SnPb); consult the factory for availability of lead-free material.

NanoStar is a trademark of Texas Instruments.

Figure 25. Nanostar™ Wafer Chip Scale Package

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73001DBVR	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGVI	Samples
TPS73001DBVRG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGVI	Samples
TPS73001DBVT	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGVI	Samples
TPS73001DBVTG4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGVI	Samples
TPS73018DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHHI	Samples
TPS73018DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHHI	Samples
TPS73018DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHHI	Samples
TPS73018DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHHI	Samples
TPS73025DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGWI	Samples
TPS73025DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGWI	Samples
TPS73025DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGWI	Samples
TPS73025DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGWI	Samples
TPS73025YZQR	ACTIVE	DSBGA	YZQ	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	E4	Samples
TPS73025YZQT	ACTIVE	DSBGA	YZQ	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	E4	Samples
TPS730285DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHII	Samples
TPS730285DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHII	Samples
TPS730285DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHII	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73028DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGXI	Samples
TPS73028DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGXI	Samples
TPS73028DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGXI	Samples
TPS73028DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGXI	Samples
TPS73028YZQR	ACTIVE	DSBGA	YZQ	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	E2	Samples
TPS73028YZQT	ACTIVE	DSBGA	YZQ	5	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	E2	Samples
TPS73030DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGYI	Samples
TPS73030DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGYI	Samples
TPS73030DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGYI	Samples
TPS73030DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PGYI	Samples
TPS73033DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHUI	Samples
TPS73033DBVRG4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHUI	Samples
TPS73033DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHUI	Samples
TPS73033DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PHUI	Samples
TPS73047DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PETI	Samples
TPS73047DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PETI	Samples
TPS73047DBVTG4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PETI	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

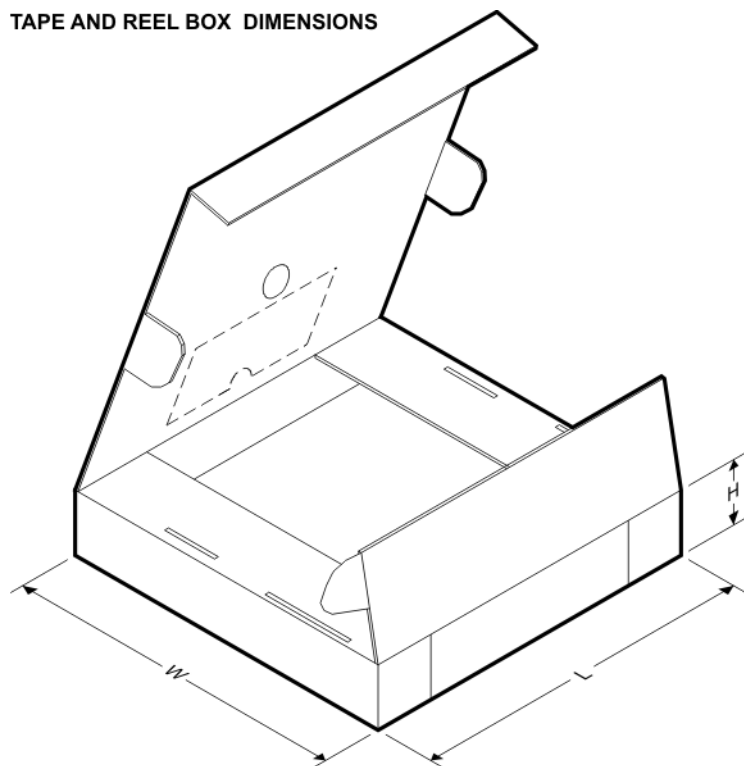
TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73001DBVR	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73001DBVR	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73001DBVT	SOT-23	DBV	6	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73018DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73018DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73025DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73025DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73025YZQR	DSBGA	YZQ	5	3000	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS73025YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS730285DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS730285DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73028DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73028DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73028YZQR	DSBGA	YZQ	5	3000	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS73028YZQT	DSBGA	YZQ	5	250	178.0	8.4	0.98	1.46	0.69	4.0	8.0	Q1
TPS73030DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73030DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73033DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73033DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73047DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



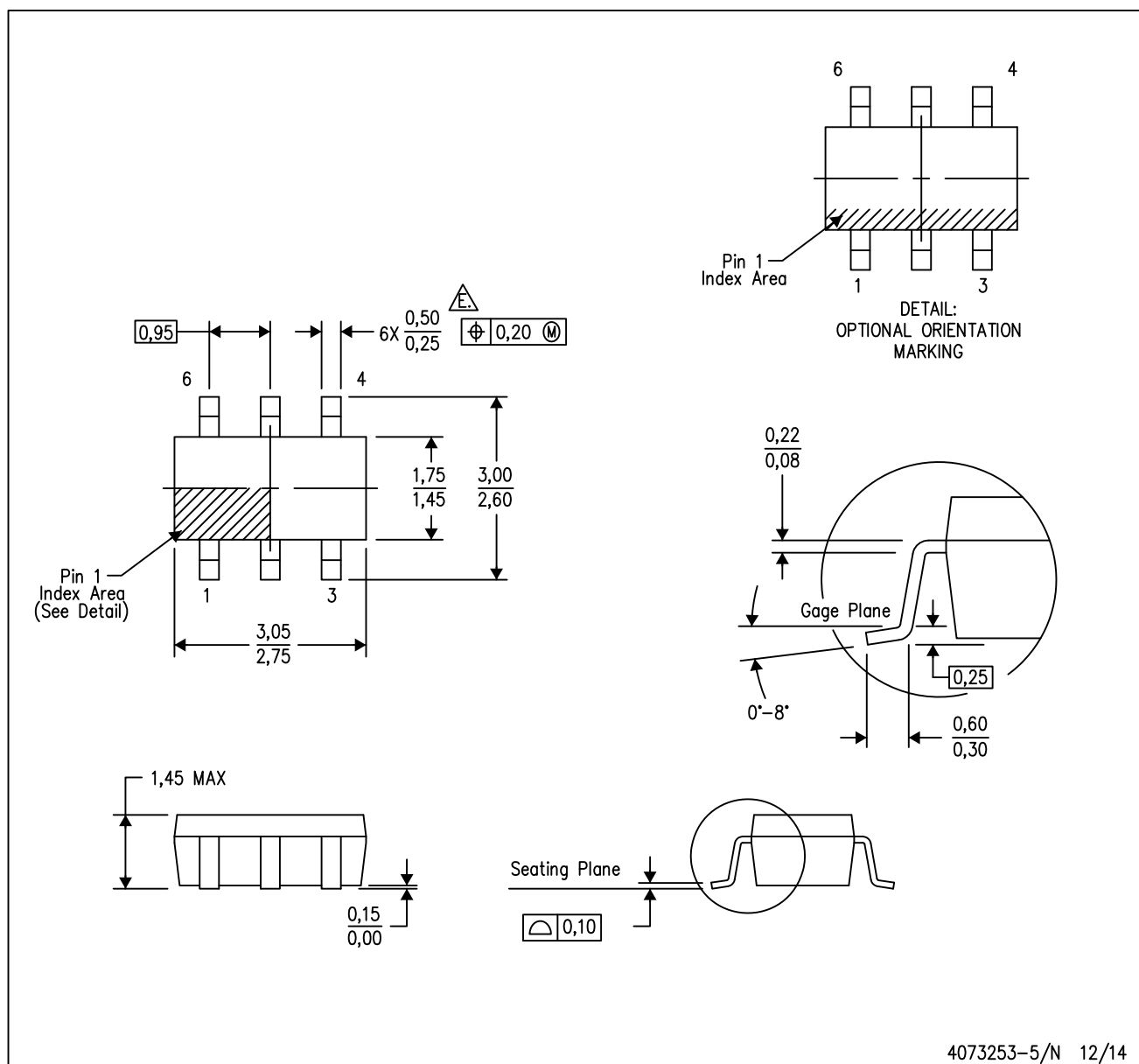
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73001DBVR	SOT-23	DBV	6	3000	203.0	203.0	35.0
TPS73001DBVR	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS73001DBVT	SOT-23	DBV	6	250	180.0	180.0	18.0
TPS73018DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73018DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73025DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73025DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73025YZQR	DSBGA	YZQ	5	3000	217.0	193.0	35.0
TPS73025YZQT	DSBGA	YZQ	5	250	217.0	193.0	35.0
TPS730285DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS730285DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73028DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73028DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73028YZQR	DSBGA	YZQ	5	3000	217.0	193.0	35.0
TPS73028YZQT	DSBGA	YZQ	5	250	217.0	193.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73030DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73030DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73033DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73033DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73047DBVR	SOT-23	DBV	5	3000	203.0	203.0	35.0

DBV (R-PDSO-G6)

PLASTIC SMALL-OUTLINE PACKAGE

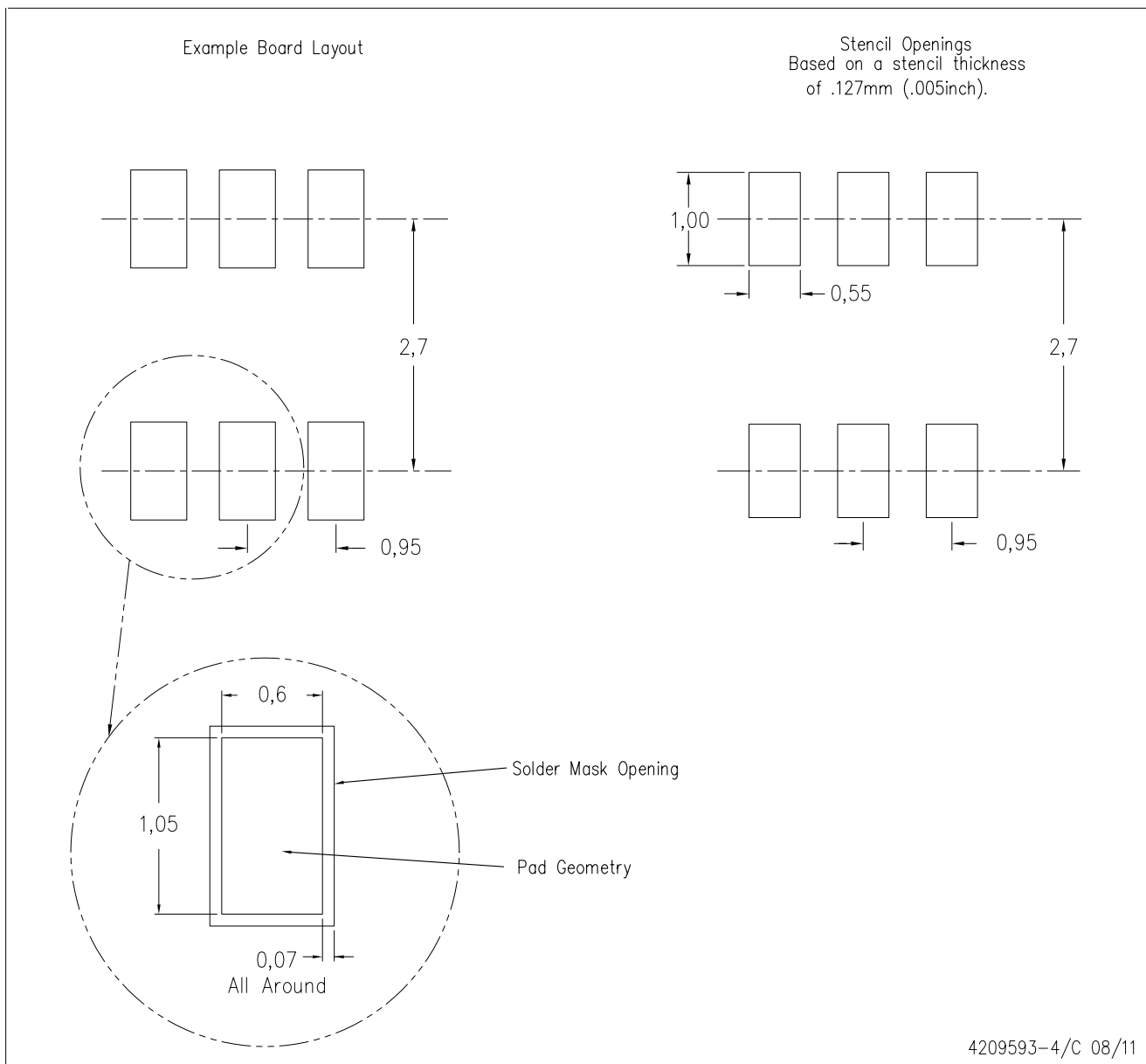


4073253-5/N 12/14

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
 - E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

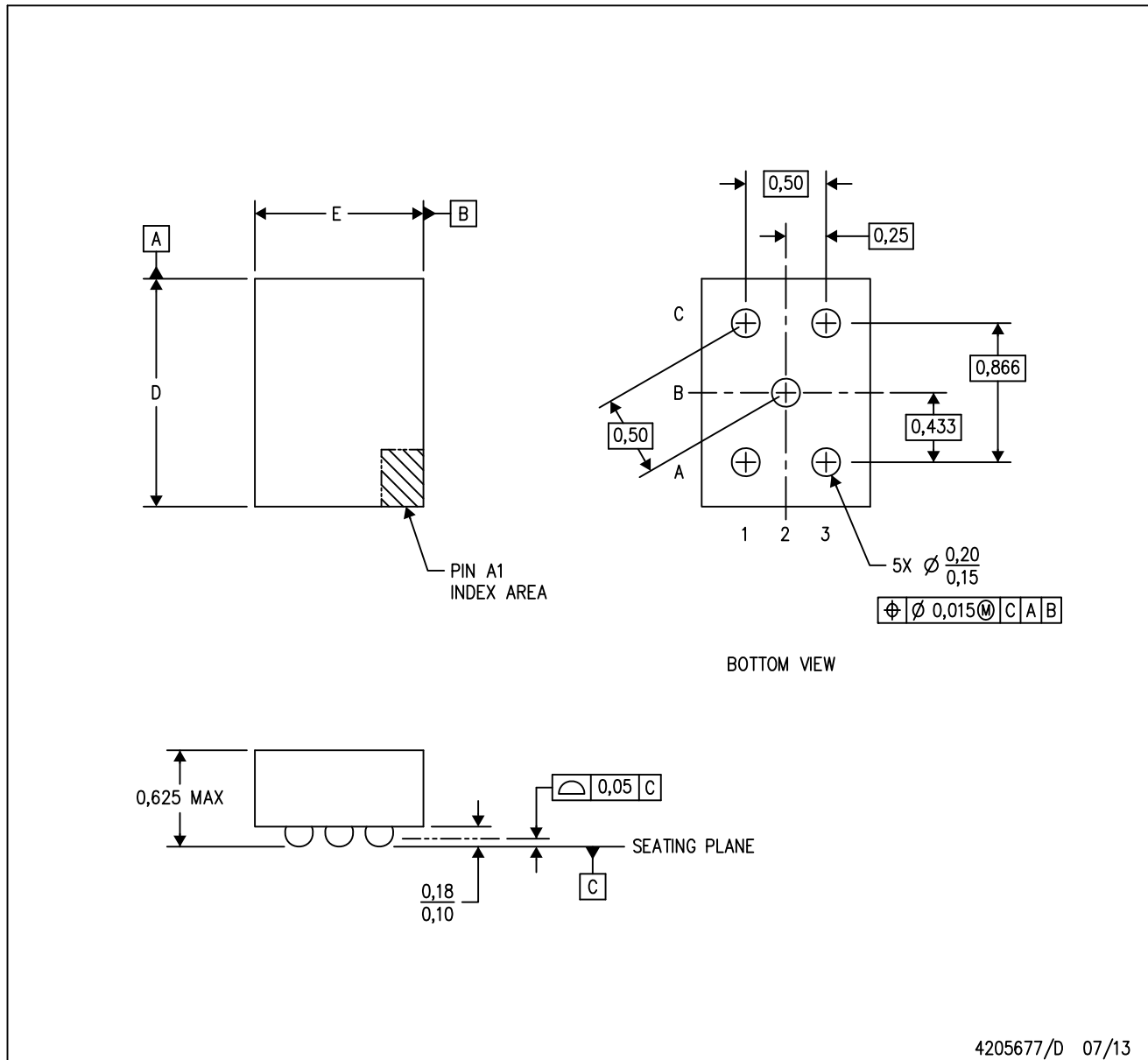
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

YZQ (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



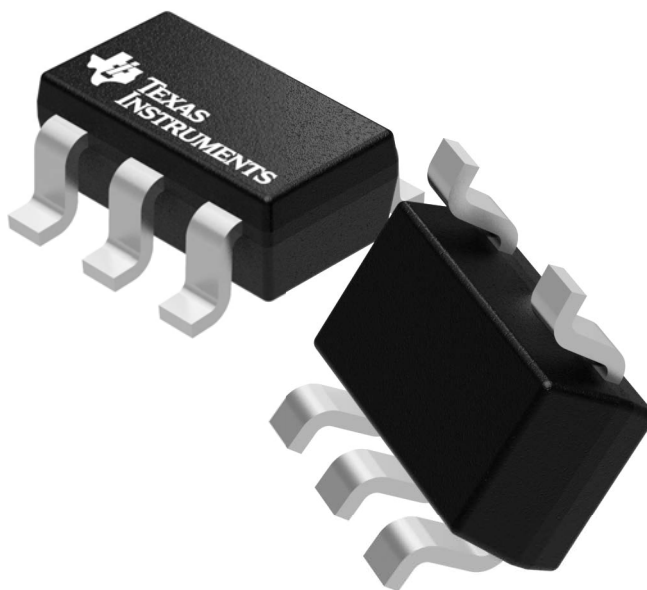
- Notes:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.

GENERIC PACKAGE VIEW

DBV 5

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

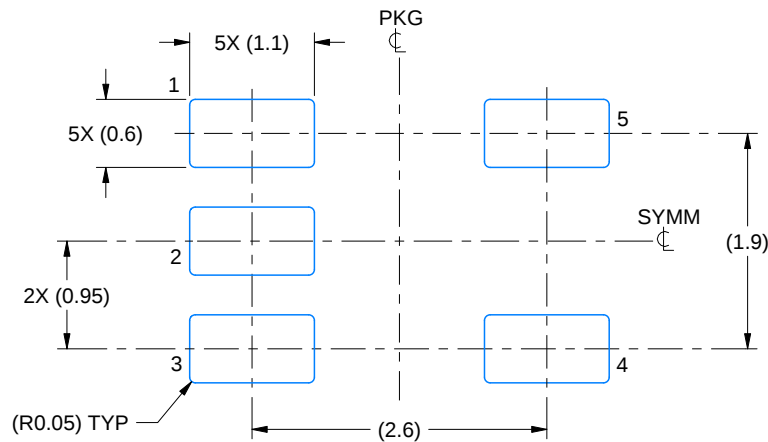
4073253/P

EXAMPLE BOARD LAYOUT

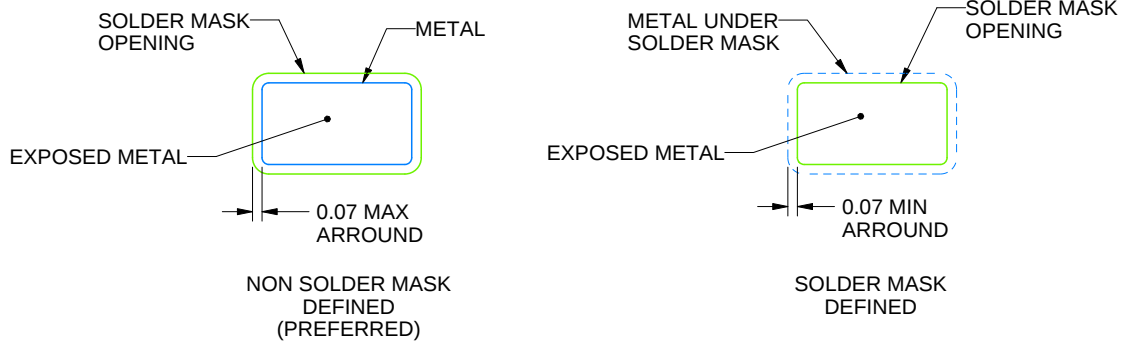
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/C 04/2017

NOTES: (continued)

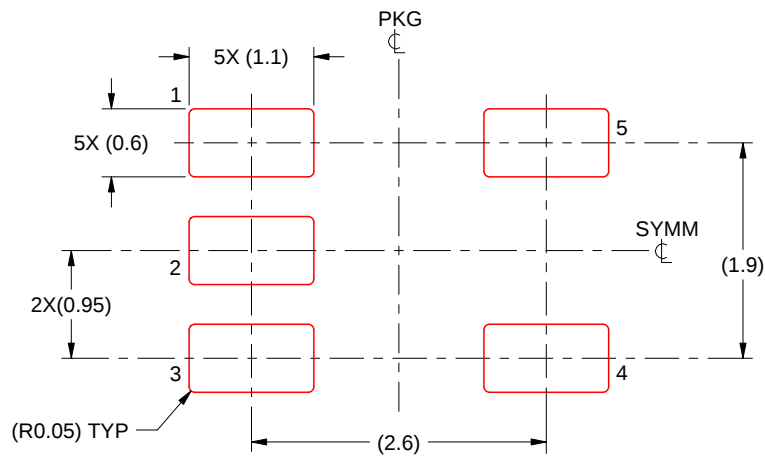
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/C 04/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.