TLF4949

5V Low Drop Out Linear Voltage Regulator

TLF4949SJ
TLF4949EJ

Data Sheet

Rev. 1.0, 2012-05-07

Automotive Power

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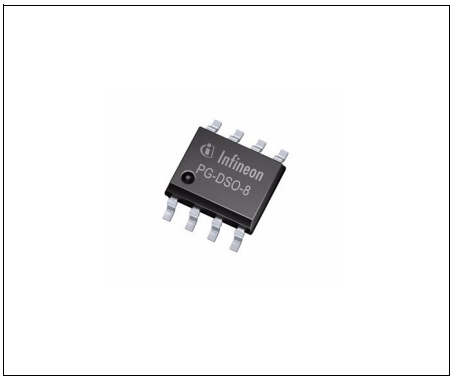
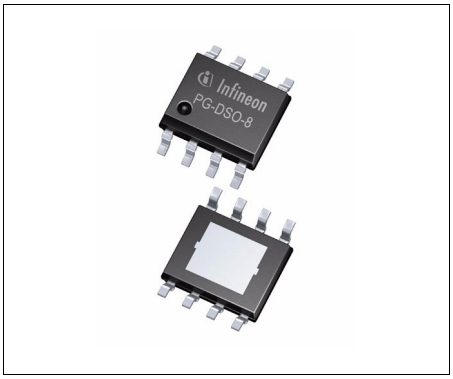
1 Overview



PG-DSO-8



PG-DSO-8 Exposed Pad

Features

- Operating DC Supply Voltage Range 5 V to 28 V
- Transient Supply Voltage up to 40 V
- Extremely low Quiescent Current in Standby Mode
- High Precision Standby Output Voltage 5 V ±1%
- Output Current Capability up to 100 mA
- Very low Dropout Voltage less than 0.5 V
- Reset Circuit sensing the Output Voltage
- Programmable Reset Pulse Delay with External Capacitor
- Voltage Sense Comparator
- Thermal Shutdown and Short Circuit Protections
- Suitable for Use in Automotive Electronics
- Green Product (RoHS)
- AEC Qualified

Description

The TLF4949 is a monolithic integrated 5V voltage regulator with a very low dropout output and additional functions as undervoltage reset with power-on reset delay and input voltage sense. It is designed to supply microcontroller controlled systems especially in automotive applications.

Type	Package	Marking
TLF4949SJ	PG-DSO-8	TLF4949S
TLF4949EJ	PG-DSO-8 Exposed Pad	TLF4949E

2 Block Diagram

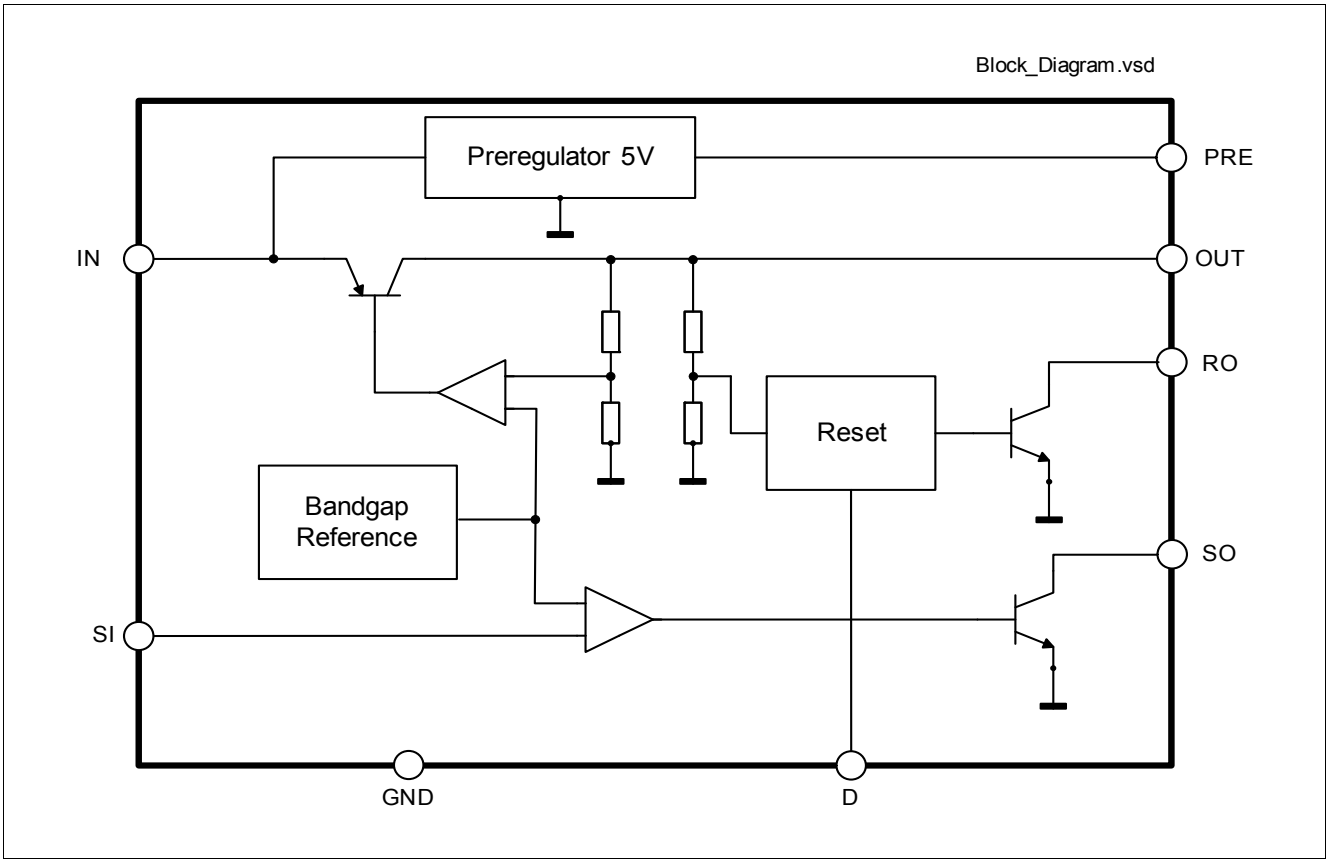


Figure 1 Block Diagram

3 Pin Configuration

3.1 Pin Assignment PG-DSO-8

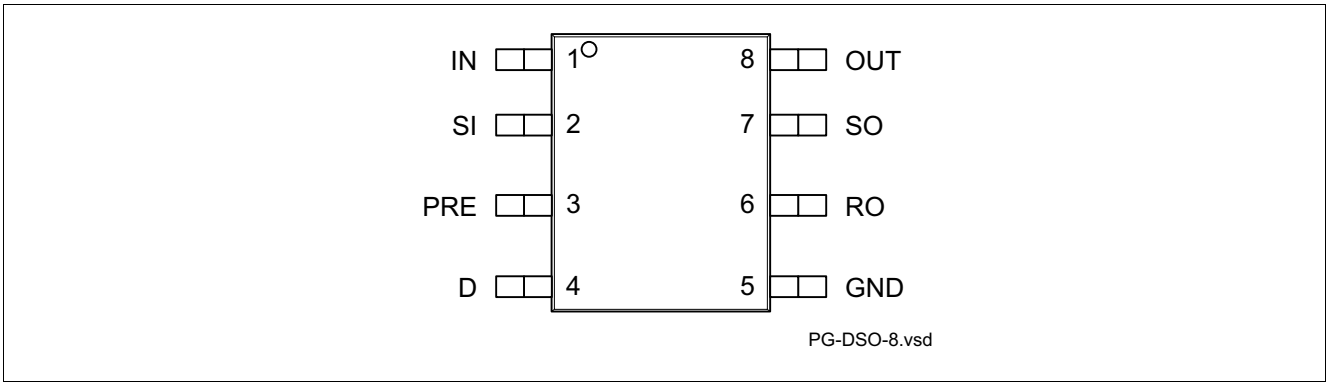


Figure 2 Pin Configuration PG-DSO-8

3.2 Pin Definitions and Functions PG-DSO-8

Pin	Symbol	Function
1	IN	**Input;** block to GND directly at the IC with a ceramic capacitor.
2	SI	**Sense Input;** if not needed connect to OUT
3	PRE	**Preregulator Output;**
4	D	**Reset Delay;** to select delay time, connect to GND via capacitor.
5	GND	**Ground**
6	RO	**Reset Output;** open-collector output. Keep open, if not needed.
7	SO	**Sense Output;** open-collector output. Keep open, if not needed.
8	OUT	**5-V Output;** connect to GND with a capacitor $\geq 4.7\mu F$, ESR < 10 Ω.[1) 2)]

1) For the usage of capacitors with very low ESR-values it is recommended to use a small 1Ω resistor in series.

2) Measured at f = 10kHz.

3.3 Pin Assignment PG-DSO-8 Exposed Pad

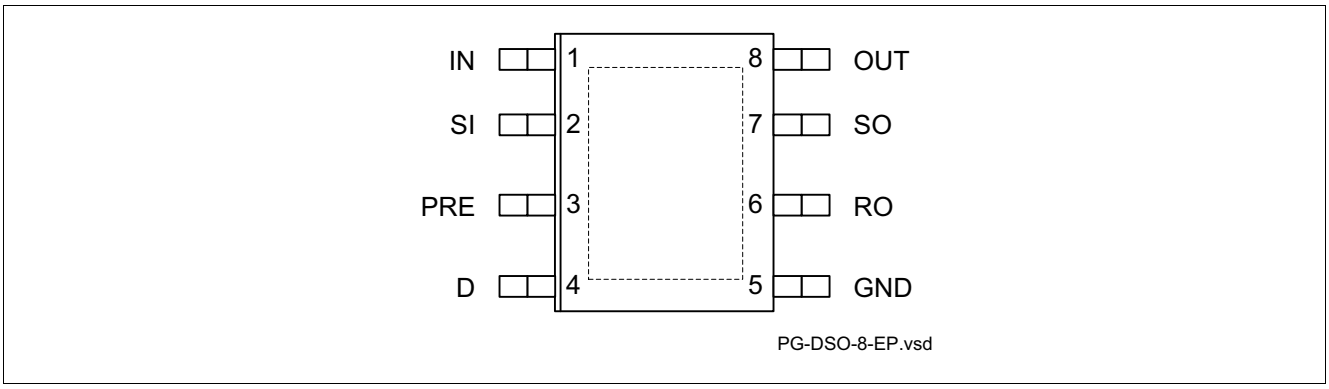


Figure 3 Pin Configuration PG DSO-8 Exposed Pad

3.4 Pin Definitions and Functions PG-DSO-8 Exposed Pad

Pin	Symbol	Function
1	IN	**Input;** block to GND directly at the IC with a ceramic capacitor.
2	SI	**Sense Input;** if not needed connect to OUT.
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5	GND	**Ground**
6	RO	**Reset Output;** open-collector output. Keep open, if not needed.
7	SO	**Sense Output;** open-collector output. Keep open, if not needed.
8	OUT	**5-V Output;** connect to GND with a capacitor $\geq 4.7\mu F$, ESR < 10 Ω[1) 2)].
Exposed Pad	PAD	**Heat sink** connect to PCB heat sink area and GND

1) For the usage of capacitors with very low ESR-values it is recommended to use a small 1Ω resistor in series.

2) Measured at f = 10kHz.

4 General Product Characteristics

4.1 Absolute Maximum Ratings

Absolute Maximum Ratings [1)]

T_j = -40°C to +125°C; all voltages with respect to ground, direction of current as shown in **Figure 4 "Application Diagram" on Page 15** (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
Voltage Rating						
4.1.1	DC Operating Supply	V_{IN}	-0.3	28	V	–
4.1.2	Transient Supply Voltage	V_{IN_TR}	–	45	V	2)
4.1.3	Preregulator Output	V_{PRE}	–	7	V	–
4.1.4	Voltage Regulator Output	V_{OUT}	-0.3	20	V	–
4.1.5	Reset Output	V_{RO}	-0.3	20	V	–
4.1.6	Sense Input	V_{SI}	-30	40	V	–
4.1.7	Sense Output Voltage	V_{SO}	-0.3	20	V	–
4.1.8	Reset Delay	V_D	-0.3	7	V	–
Current Rating						
4.1.9	Preregulator Output	I_{PRE}	–	5	mA	–
4.1.10	Reset Out	I_{RO}	–	5	mA	–
4.1.11	Sense Out	I_{SO}	–	5	mA	–
Temperatures						
4.1.12	Junction Temperature	T_j	-40	150	°C	–
4.1.13	Storage Temperature	T_{stg}	-50	150	°C	–
ESD Susceptibility						
4.1.14	ESD Resistivity to GND	V_{ESD}	-4	4	kV	HBM[3)]
4.1.15	ESD Resistivity to GND	V_{ESD}	-1	1	kV	CDM[4)]

1) Not subject to production test, specified by design.

2) For transient durations of t_{TR} < 1s.

3) ESD susceptibility, HBM according to ANSI/ESDA/JEDEC JS-001 (1.5 kΩ, 100 pF).

4) ESD susceptibility, Charged Device Model "CDM" ESDA STM5.3.1 or ANSI/ESD S.5.3.1.

Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.

4.2 Functional Range

Table 1

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Input Voltage Range for Normal Operation	V_{IN}	5.5	28	V	–
4.2.2	Extended Input Voltage Range	V_{IN}	3.5	40	V	–[1) 2)]

1) The output voltage will follow the input voltage for input voltages below V_{OUT} + V_{DR}, i.e device is in tracking mode until $V_{OUT} + V_{DR}$ is reached.

2) Input voltages ranging from > 28 V up to 40 V may only be applied for transient periods t_{TR} < 1s.

Note: Within the functional or operating range, the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the Electrical Characteristics table.

4.3 Thermal Resistance

*Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to **www.jedec.org**.*

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
TLF4949SJ (PG-DSO-8)							
4.3.3	Junction to Soldering Point[1)]	R_{thJSP}	–	71	–	K/W	–
4.3.4	Junction to Ambient[1)]	R_{thJA}	–	116	–	K/W	–[2)]
4.3.5			–	172	–	K/W	Footprint only[3)]
4.3.6			–	145	–	K/W	300 mm² heatsink area on PCB[3)]
4.3.7			–	139	–	K/W	600 mm² heatsink area on PCB[3)]
TLF4949EJ (PG-DSO-8 Exposed Pad)							
4.3.1	Junction to Case[1)]	R_{thJC}	–	19	–	K/W	–
4.3.2	Junction to Ambient[1)]	R_{thJA}	–	52	–	K/W	–[4)]
4.3.3			–	167	–	K/W	Footprint only[3)]
4.3.4			–	78	–	K/W	300 mm² heatsink area on PCB[3)]
4.3.5			–	66	–	K/W	600 mm² heatsink area on PCB[3)]
Thermal Shutdown							
4.3.6	Junction Temperature	T_{JSD}	–	165	–	°C	[1)]

1) Not subject to production test, specified by design.

2) Specified R_{thJA} value is according to Jedec JESD51-2,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu).

3) Specified R_{thJA} value is according to JEDEC JESD 51-3 at natural convection on FR4 1s0p board; The Product (Chip+Package) was simulated on a 76.2 × 114.3 × 1.5 mm³ board with 1 copper layer (1 x 70µm Cu).

4) Specified R_{thJA} value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

4.4 Electrical Characteristics

4.4.1 Voltage Regulator

Electrical Characteristics: Regulator

V_{IN} = 14 V, T_j = -40°C to +125°C, all voltages with respect to ground, direction of current as shown in **Figure 4 "Application Diagram" on Page 15** (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.4.1	Output Voltage	V_{OUT}	4.95	5	5.05	V	T_J = 25°C; I_{OUT} = 1mA
4.4.2			4.90	5	5.10	V	6V ≤ V_{IN} ≤ 28V; 1mA ≤ I_{OUT} ≤ 50mA
4.4.3			4.85	–	5.15	V	V_{IN} = 40V[1]; 5mA ≤ I_{OUT} ≤ 100mA
4.4.4			4.85	5	5.15		6V ≤ V_{IN} ≤ 28V; 0mA ≤ I_{OUT} ≤ 100mA
4.4.5	Dropout Voltage V_{DR} = V_{IN} - V_{OUT}	V_{DR}		0.1 0.2 0.3	0.25 0.4 0.5	V V V	I_{OUT} = 10mA I_{OUT} = 50mA I_{OUT} = 100mA
4.4.6	Input to Output Voltage Difference in Undervoltage Condition	V_{IO}	–	0.17	0.4	V	V_{IN} = 3.5V; I_{OUT} = 35mA
4.4.7	Current Sink Capability from Output to GND	I_{outh}[2]	-30	-55	–	µA	V_{IN} = 25V; V_{OUT} = 5.5V
4.4.8	Line Regulation	$\Delta V_{OUT,line}$	–	1	15	mV	6V < V_{IN} < 28V; I_{OUT} = 1mA
4.4.9	Load Regulation	$\Delta V_{OUT,load}$	–	4	20	mV	1mA ≤ I_{OUT} ≤ 100mA
4.4.10	Current Limit	$I_{OUT,lim}$	120	240 180	400	mA mA	V_{OUT} = 4.5V V_{OUT} = 0V [3]
4.4.11	Quiescent Current	I_{QSE}	–	180	300	µA	I_{OUT} = 0.3mA
4.4.12	Quiescent Current	I_Q	–	–	3.6	mA	I_{OUT} = 100mA

1) V_{IN} = 40V may be only applied as transient supply voltage to the device for maximum period of t_{TR} < 1s. Please note that also for such transient conditions, especially under higher load conditions, the absolute maximum rating of T_J must be respected at any time. If transient conditions up to V_{IN} = 40V and elevated load currents are expected in the application a sufficient cooling must be provided to meet the power dissipation. Testing this parameter for the maximum allowed period of T = 1s is for thermal reasons not subject to production test but guaranteed by design.

2) The test of this parameter ensures that the output voltage will not exceed 5.5V in a corresponding "no load current"-condition. A sufficiently high value for I_{outh} will allow the output to react in a fast manner in case of a sudden decrease of load current (e.g. if load is switching to standby or powerdown mode) .

3) Foldback characteristic.

4.4.2 RESET

Electrical Characteristics: Reset

V_{IN} = 14 V, T_j = -40°C to +125°C, all voltages with respect to ground, direction of current as shown in **Figure 4 "Application Diagram" on Page 15** (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.4.13	Reset Threshold Voltage	V_{RT}	4.25	4.5	4.75	V	–
4.4.14	Reset Threshold Hysteresis	V_{RTH}	50	100	200	mV	–
4.4.15	Reset Pulse Delay	t_{RD}	55	100	180	ms	Calculated Value: C_D = 100nF; $t_R \geq$ 100µs
4.4.16	Reset Output Low Voltage	V_{RL}	–	–	0.4	V	$R_{RES} \geq$ 10kΩ to V_{OUT}; $V_{IN} \geq$ 0V and $V_{OUT} \geq$ 1V[1)]
4.4.17	Reset Output High Leakage Current	I_{RH}	–	–	1	µA	V_{RES} = 5V
4.4.18	Delay Comparator Threshold	$V_{D,th}$	–	2	–	V	–
4.4.19	Delay Comparator Threshold Hysteresis	$V_{D,th,\ hy}$	–	100	–	mV	–
4.4.20	Delay Capacitor charge current	$I_{D,chg}$	–	2	–	µA	V_D = 1V; current flowing out of D pin
4.4.21	Delay Capacitor discharge current	$I_{D,dchg}$	–	9	–	mA	V_D = 1V; current flowing into D pin

1) Device entering this condition by decreasing V_{IN} from powered up and fully initialized operation state.

4.4.3 Sense

Electrical Characteristics: Sense

V_{IN} = 14 V, T_j = -40°C to +125°C, all voltages with respect to ground, direction of current as shown in **Figure 4 "Application Diagram" on Page 15** (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Sense							
4.4.22	Sense Low Threshold	V_{ST}	1.16	1.23	1.35	V	–
4.4.23	Sense Threshold Hysteresis	V_{STH}	20	100	200	mV	–
4.4.24	Sense Output Low Voltage	V_{SL}	–	–	0.4	V	$V_{SI} \leq$ 1.16V; $V_{IN} \geq$ 3.5V; $R_{SO} \geq$ 10KΩ to V_{OUT}
4.4.25	Sense Output Leakage	I_{SH}	–	–	1	µA	V_{SO}= 5V; $V_{SI} \geq$ 1.5V
4.4.26	Sense Input Current	I_{SI}	-5	-1.5	0	µA	V_{SI} = 0

4.4.4 Preregulator

Electrical Characteristics: Preregulator

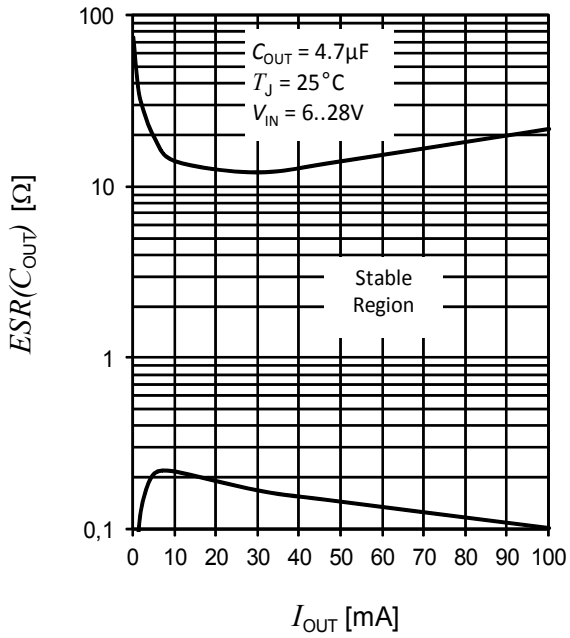
V_{IN} = 14 V, T_j = -40°C to +125°C, all voltages with respect to ground, direction of current as shown in **Figure 4 "Application Diagram" on Page 15** (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
Preregulator							
4.4.27	Preregulator Output Voltage	V_{PRE}	4.5	5	6	V	I_{PRE} = 10 µA
4.4.28	Preregulator Output Current	I_{PRE}	–	–	10	µA	–

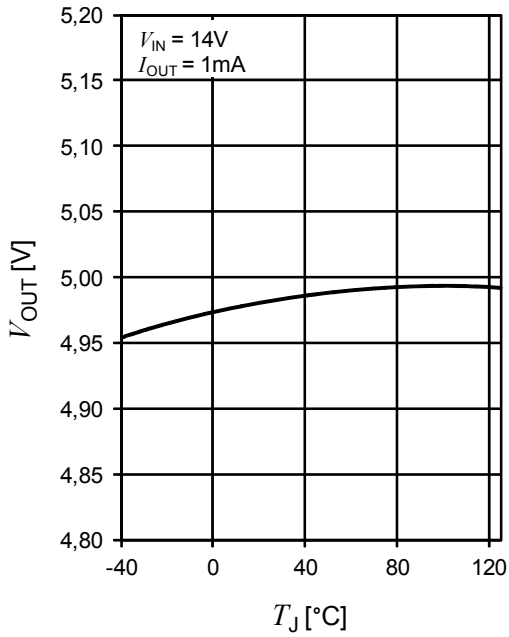
4.5 Typical Performance Graphs

Typical Performance Characteristics

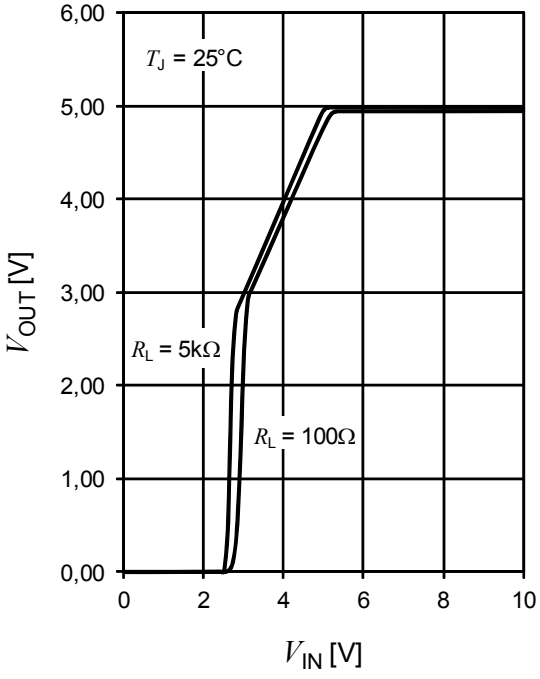
Equivalent Series Resistance $ESR(C_{OUT})$ versus Output Current I_{OUT}



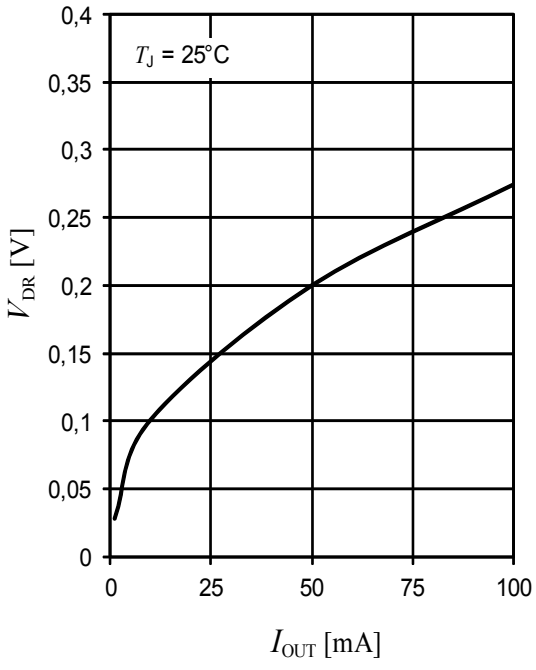
Output Voltage V_{OUT} versus Junction Temperature T_J



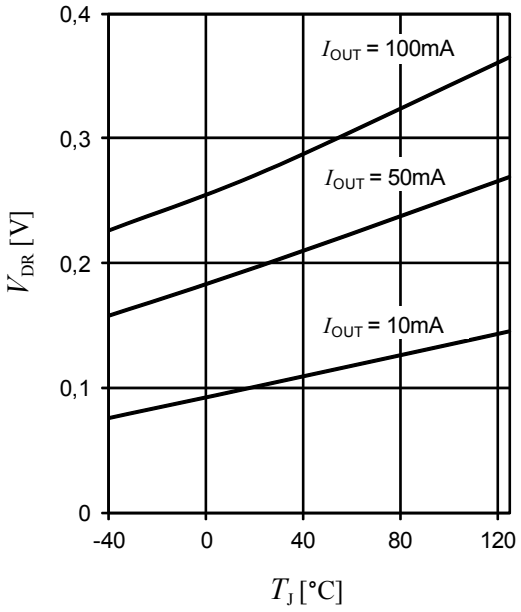
Output Voltage V_{OUT} versus Input Voltage V_{IN}



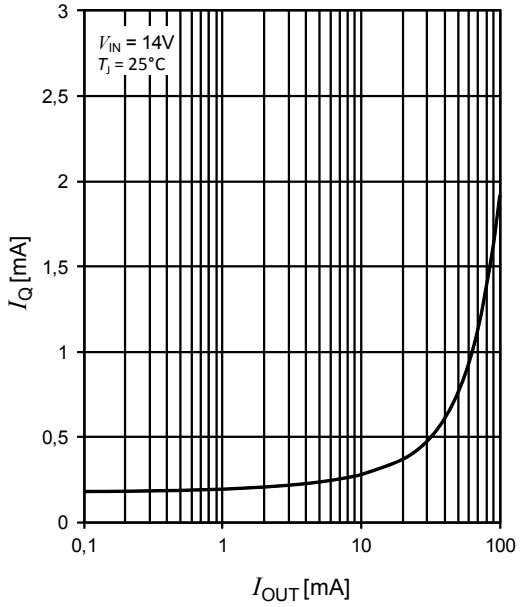
Dropout Voltage V_{DR} versus Output Current I_{OUT}



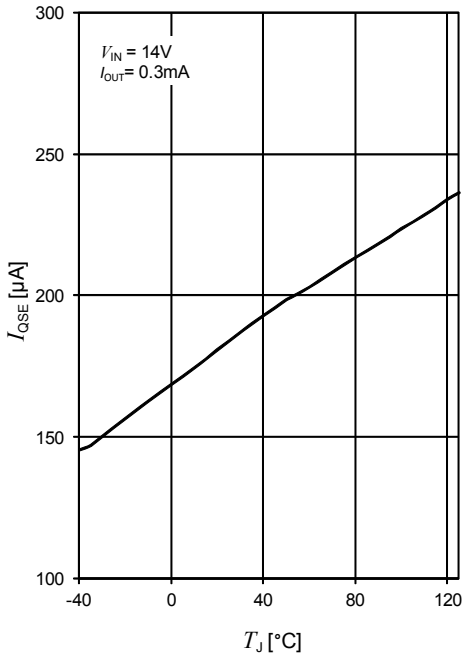
Dropout Voltage V_{DR} versus Junction Temperature T_J



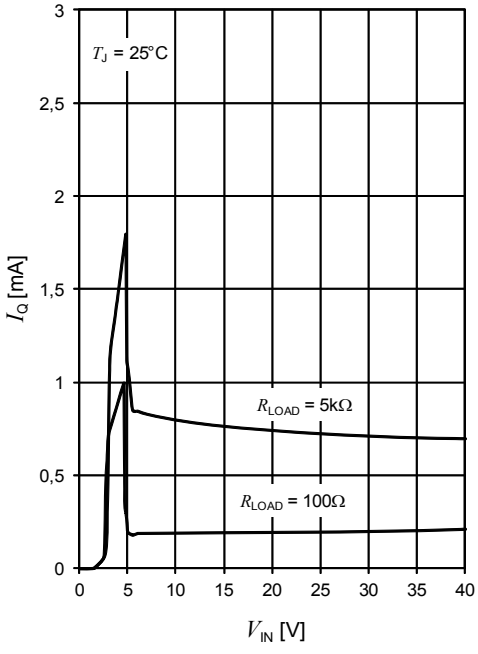
Quiescent Current I_Q versus Output Current I_{OUT}



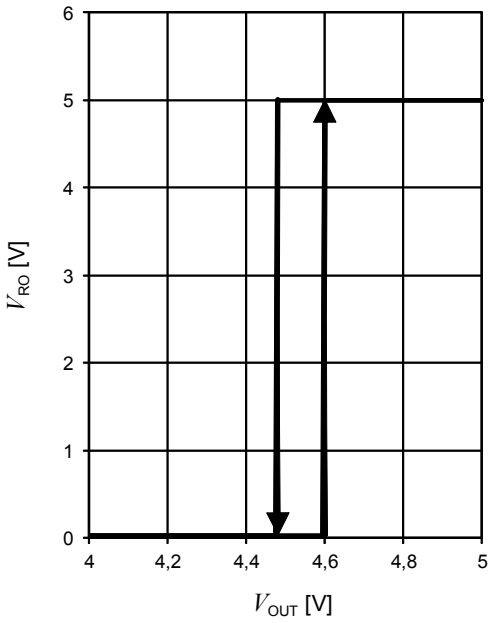
Quiescent Current I_{QSE} versus Junction Temperature T_J



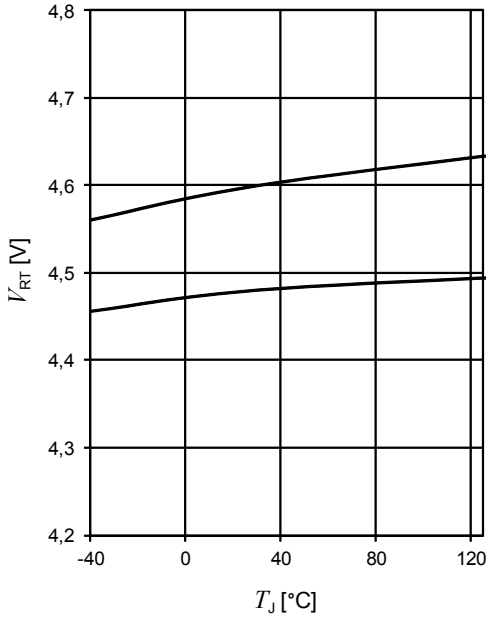
Quiescent Current I_Q versus Input Voltage V_{IN}



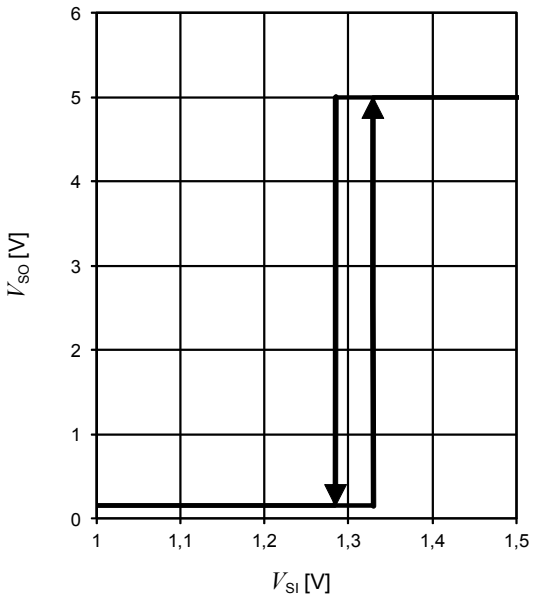
Reset Output Voltage V_{RO} versus Regulator Output Voltage V_{OUT}



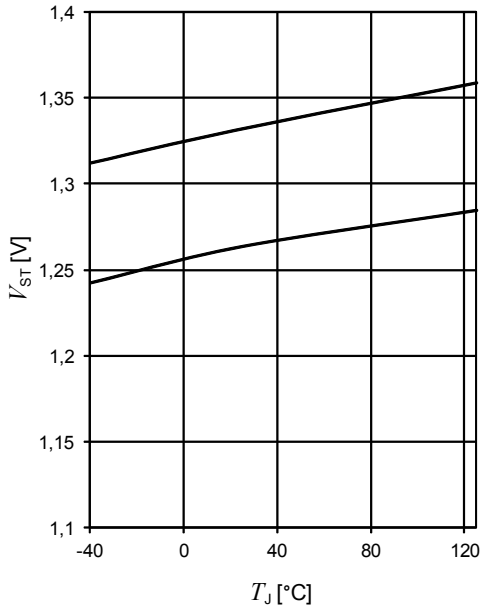
Reset Thresholds V_{RT} versus Junction Temperature T_J



Sense Output Voltage V_{SO} versus Sense Input Voltage V_{SI}



Sense Thresholds V_{ST} versus Junction Temperature T_J



5 Application Information

Note: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

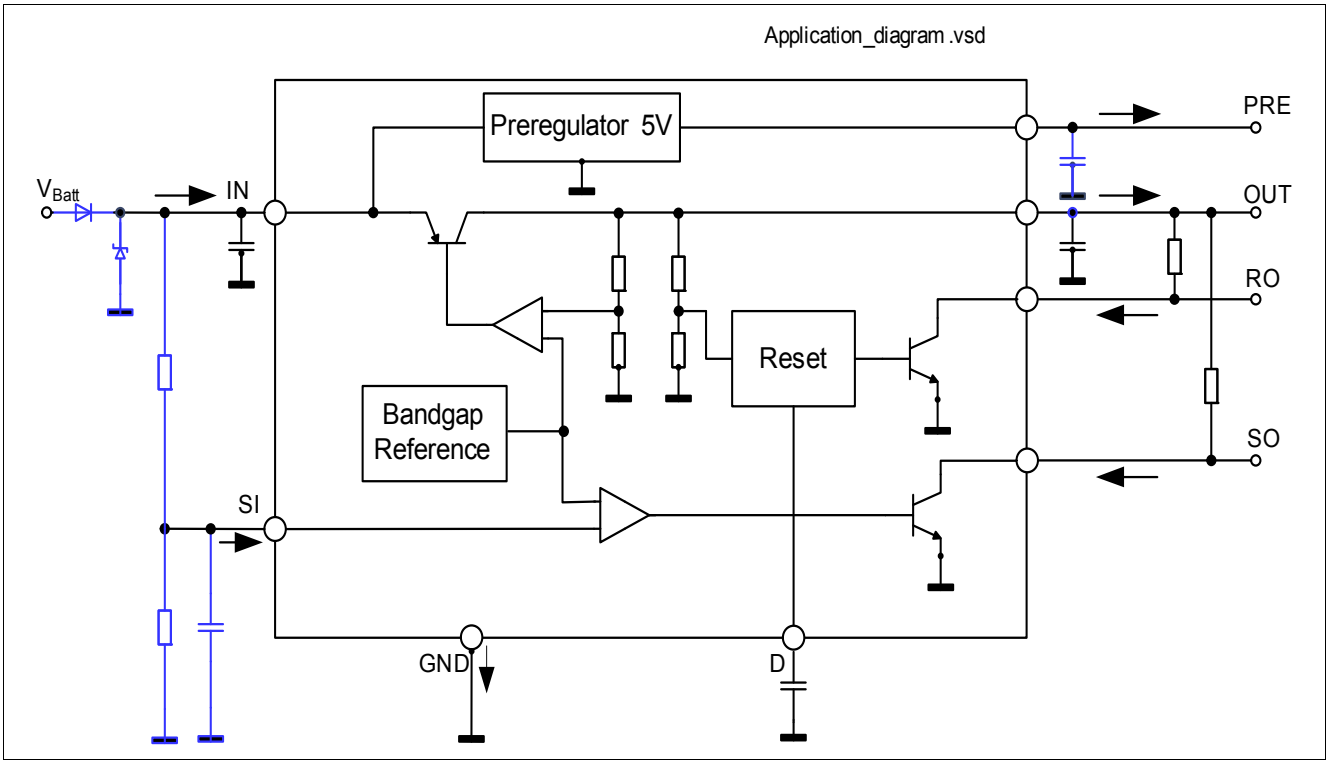


Figure 4 Application Diagram

Note: This is a very simplified example of an application circuit. The function must be verified in the real application

5.1 Supply Voltage Transients

For many other voltage regulators fast supply voltage transients can often be the cause of unwanted reset output signal perturbations. In contrast the TLF4949 shows a very high immunity of its reset output against such supply voltage transients. Already starting from input voltages as low as 5.5 V the TLF4949 shows an immunity of the reset output against supply transients of more than 100 V/µs even without an additional external capacitor at the PRE pin[1) 2)].

5.2 Functional Description

Description

The TLF4949 is a monolithic integrated low dropout voltage regulator. Several outstanding features and auxiliary functions are implemented to meet the requirements of supplying microprocessor systems in automotive applications. Nevertheless, it is suitable also in other applications where the present functions are required. The modular approach of this device allows to get easily also other features and functions when required.

1) Please note that also for the case of such input transients the absolute maximum ratings must not be violated.

2) The PRE pin of the IFX4949 offers the possibility to connect a bypass capacitor to GND to stabilize PRE output and to optimize the transient behaviour. See also section **“Preregulator ” on Page 17**.

Voltage Regulator

The voltage regulator uses a PNP transistor as a regulation element. With this structure a very low dropout voltage at currents of up to 100mA is obtained.

The dropout operation of the standby regulator is maintained down to 3.5V input supply voltage. The output voltage is regulated up to a transient input supply voltage of 40V. With this feature no functional interruption due to over voltage pulses is generated. The typical curve showing the standby output voltage as a function of the input supply voltage V_S is shown in **Figure 5 "Output Voltage vs. Input Voltage" on Page 16**.Typical values of the current consumption of this device at small loads (quiescent current) are less than 200µA.

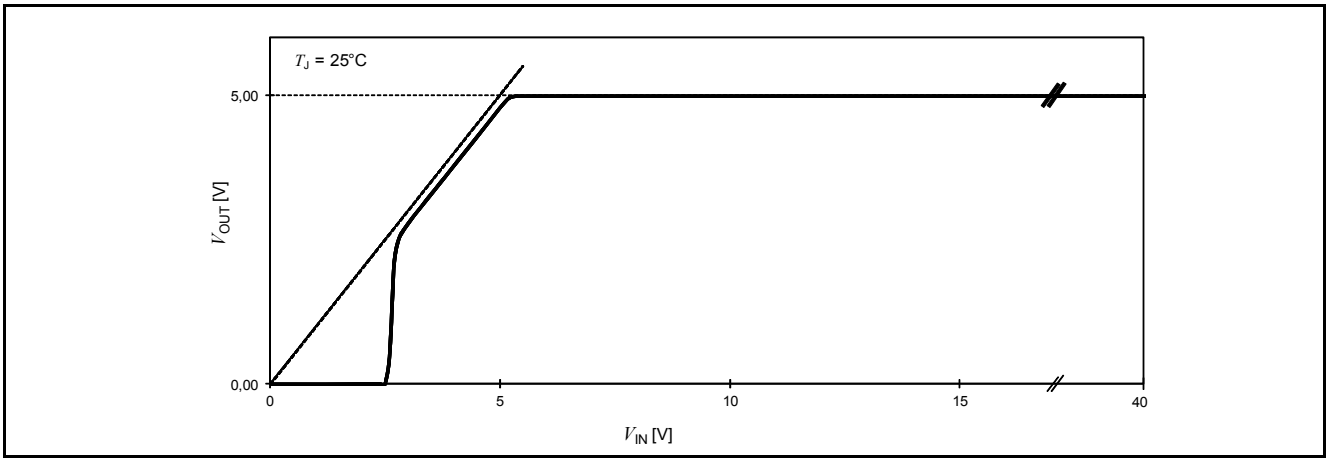


Figure 5 Output Voltage vs. Input Voltage

To reduce the quiescent current peak in the undervoltage region and to improve the transient response in this region, the dropout voltage is controlled. The quiescent current as a function of the supply input voltage is shown for two different load conditions in **Figure 6 "Quiescent Current vs. Supply Voltage" on Page 16**.

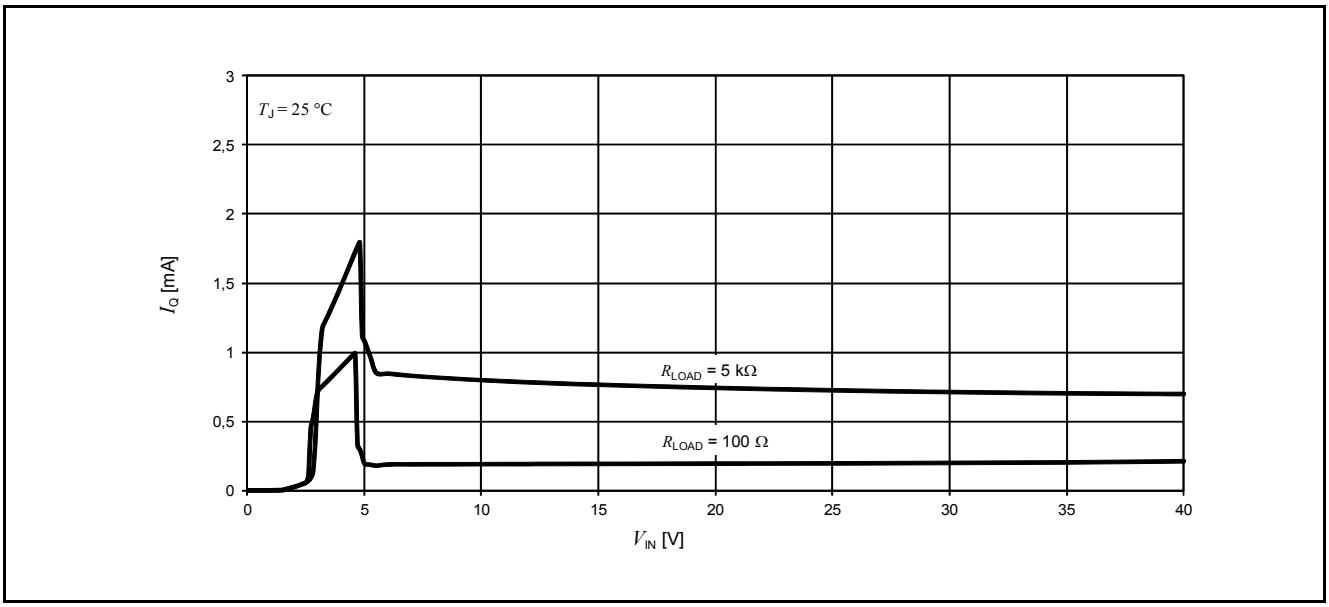


Figure 6 Quiescent Current vs. Supply Voltage

Short Circuit Protection

The maximum output current of the device is internally limited. In case of short circuit, the output current is foldback limited as described in **Figure 7 "Foldback Characteristics of VOUT" on Page 17**.

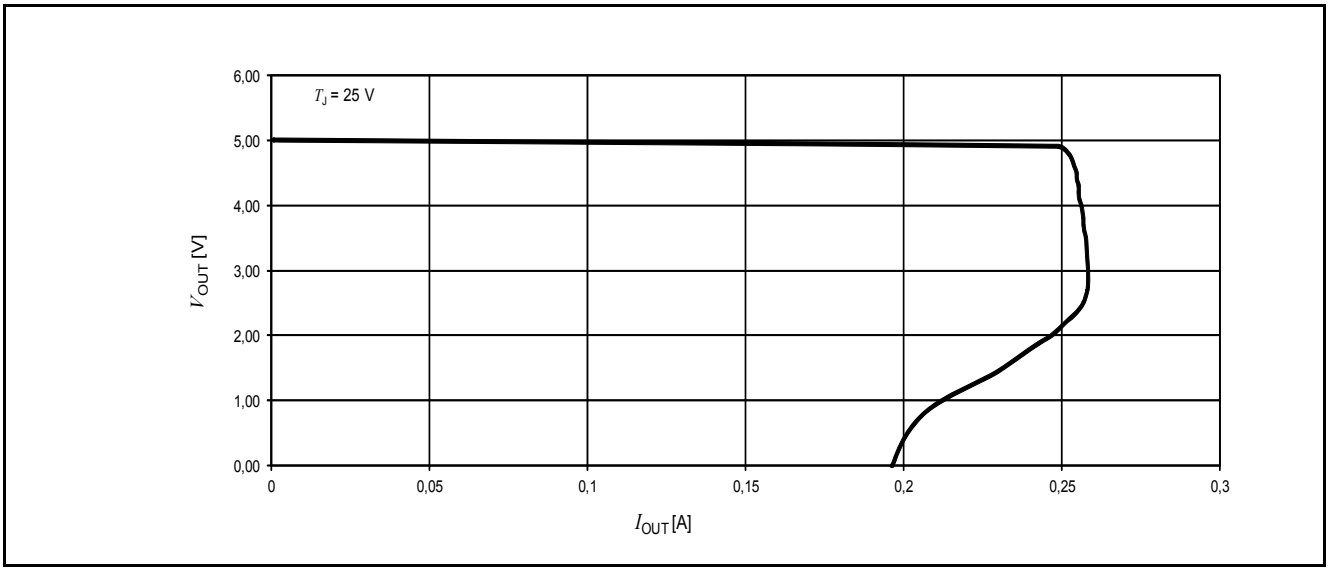


Figure 7 Foldback Characteristics of V_{OUT}

Preregulator

To improve the transient immunity a preregulator stabilizes the internal supply voltage to 5V. This internal voltage is also present at the PRE pin (Pin 3). This voltage should not be used as an output because the output capability is very small (≤ 10 µA).

This output at the PRE pin may be used as an option when an improved transient behavior for supply voltages less than 8V is desired. In this case a capacitor (100nF -1µF) can be connected between the PRE pin and GND. At the same time the usage of such a bypass capacitor is suitable to reduce output noise at the OUT pin. If this feature is not used the PRE pin must be left open.

Reset Circuit

The block circuit diagram of the reset circuit is shown in **Figure 8 “Reset Circuit” on Page 18**. The reset circuit supervises the output voltage. The reset threshold of 4.5V is defined by the internal reference voltage and standby output divider. The reset pulse delay time t_{RD}, is defined by the charge time of an external capacitor C_D:

$$t_{RD} = \frac{C_D \times 2.0\ V}{2.0\ \mu A}$$

The reaction time of the reset circuit originates from the discharge time limitation of the reset capacitor C_D and is proportional to the value of C_D.

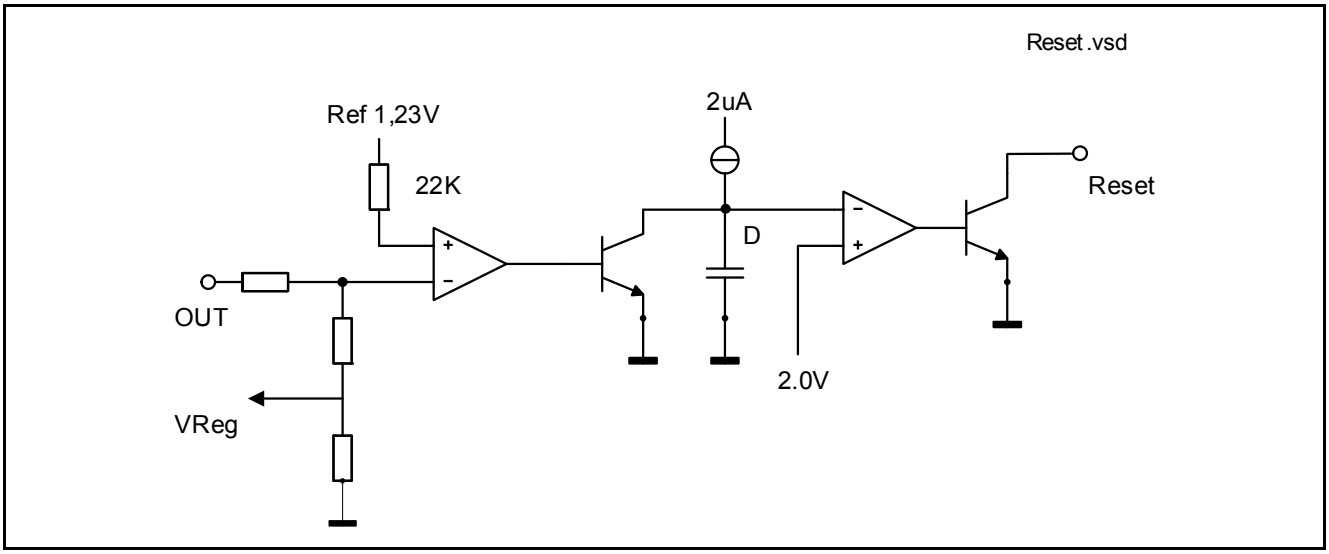


Figure 8 Reset Circuit

The reaction time of the reset circuit corresponds to its noise immunity. Standby output voltage drops below the reset threshold that are only marginally longer than the reaction time will result in a shorter reset delay times.

The nominal reset delay time will be generated for standby output voltage drops longer than approximately 50µs.

The typical reset output waveforms are shown in **Figure 9 “Typical Reset Output Waveforms” on Page 18**.

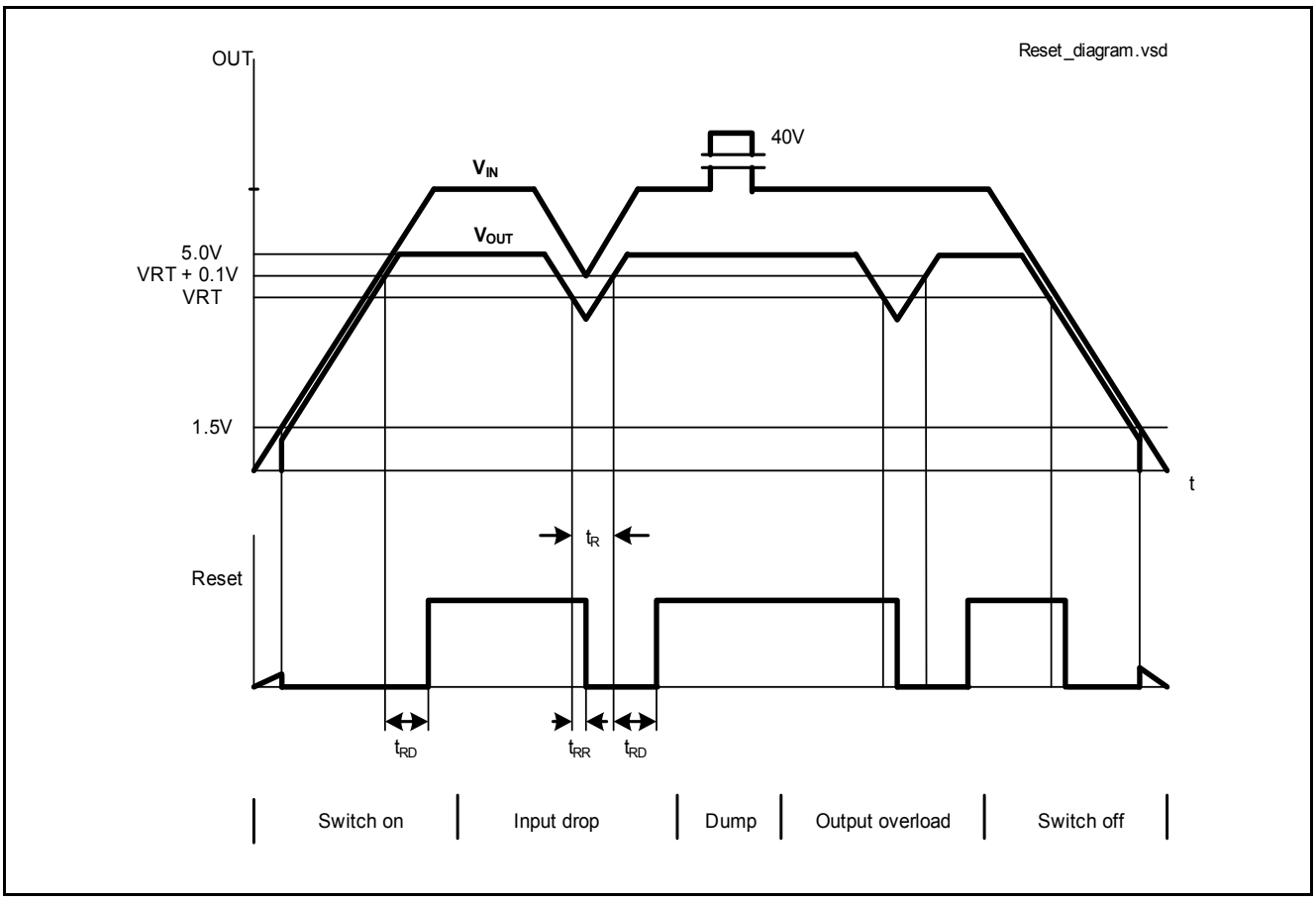


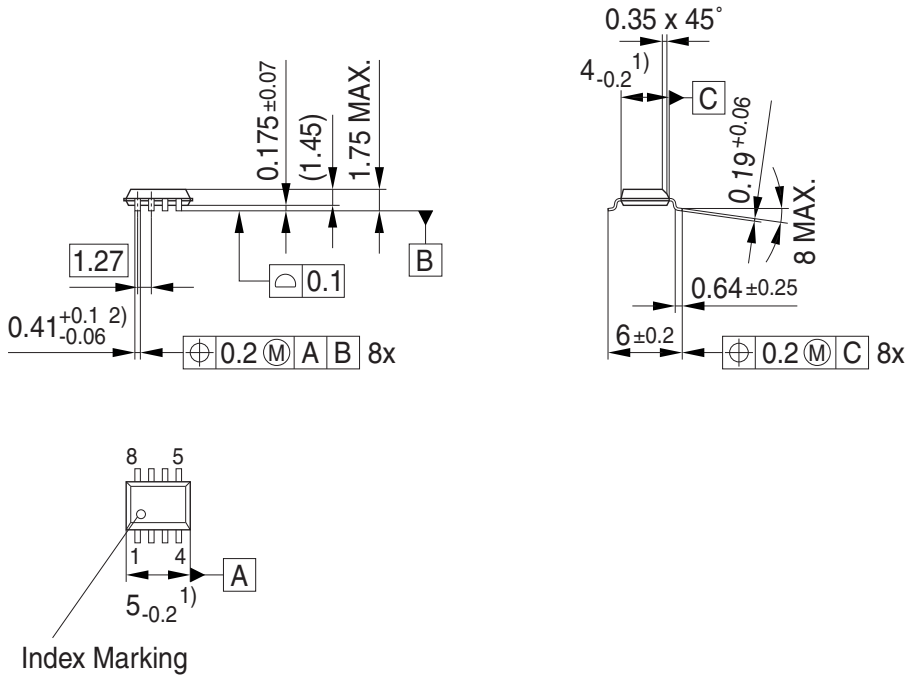
Figure 9 Typical Reset Output Waveforms

Sense Comparator

The sense comparator compares an input signal with the internal voltage reference of typical 1.23V. The use of an external voltage divider makes this comparator very flexible in the application.

It can be used to supervise the input voltage either before or after a protection diode and to give additional informations to the microprocessor like low voltage warnings.

6 Package Outlines



1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Lead width can be 0.61 max. in dambar area

GPS01181

Figure 10 PG-DSO-8

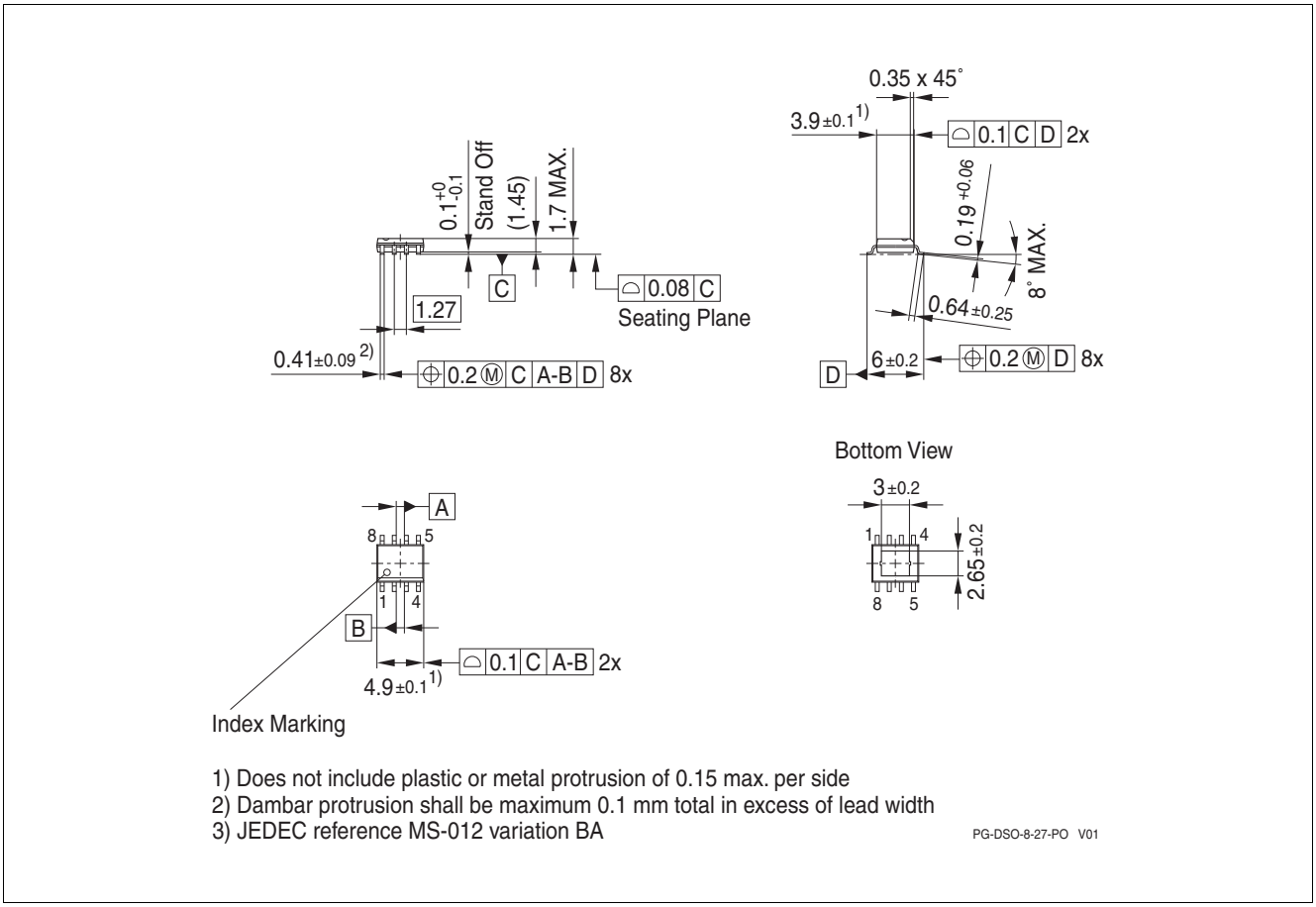


Figure 11 PG-DSO-8 Exposed Pad

Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

For further information on packages, please visit our website:
http://www.infineon.com/packages.

Dimensions in mm

7 Revision History

Revision	Date	Changes
1.0	2012-05-07	Data Sheet – Initial Release.

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