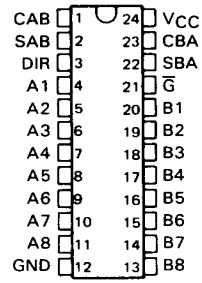
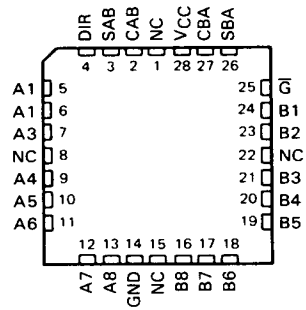
- **Inputs are TTL-Voltage Compatible**
- **Independent Registers for A and B Buses**
- **Multiplexed Real-Time and Stored Data**
- **Choice of True or Inverting Data Paths**
- **High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads**
- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54HCT' . . . JT PACKAGE
SN74HCT' . . . DW OR NT PACKAGE
(TOP VIEW)



SN54HCT' . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

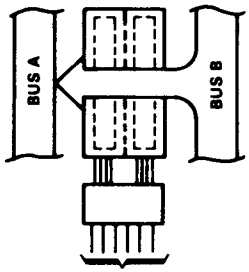
description

These devices consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers on the low-to-high transition of the appropriate clock pin (CAB or CBA). The examples on the following page demonstrate the four fundamental bus-management functions that can be performed with the 'HCT646 or 'HCT648.

Enable ($\overline{G}$) and direction (DIR) pins are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select controls (SAB and SBA) can multiplex stored and real-time (transparent mode) data. The direction control determines which bus will receive data when the enable $\overline{G}$ is active (low). In the isolation mode (enable $\overline{G}$ high), A data may be stored in one register and/or B data may be stored in the other register.

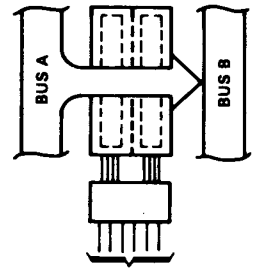
When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, A or B, may be driven at a time.

The SN54HCT' family is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74HCT' family is characterized for operation from −40°C to 85°C.



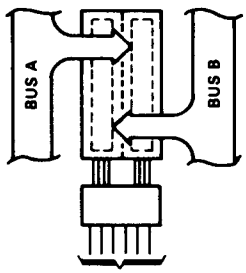
(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	X	X	L

REAL-TIME TRANSFER
BUS B TO BUS A



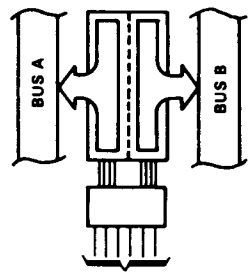
(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	H	X	X	L	X

REAL-TIME TRANSFER
BUS A TO BUS B



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

STORAGE FROM
A, B, OR A AND B



(21) $\overline{G}$	(3) DIR	(1) CAB	(23) CBA	(2) SAB	(22) SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

TRANSFER STORED DATA
TO A OR B

Pin numbers shown are for DW, JT, and NT packages.

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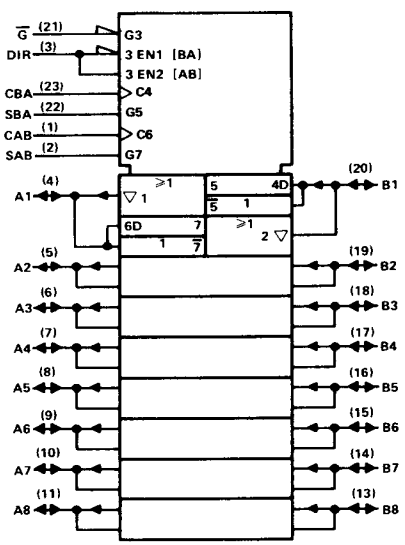
FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION	
$\overline{G}$	DIR	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	'HCT646	'HCT648
X	X	↑	X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X	↑	X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
H	X	H or L	H or L	X	X			Isolation, hold storage	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus	Real-Time $\overline{B}$ Data to A Bus
L	L	X	H or L	X	H			Stored B Data to A Bus	Stored $\overline{B}$ Data to A Bus
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus	Real-Time $\overline{A}$ Data to B Bus
L	H	H or L	X	H	X			Stored A Data to B Bus	Stored $\overline{A}$ Data to B Bus

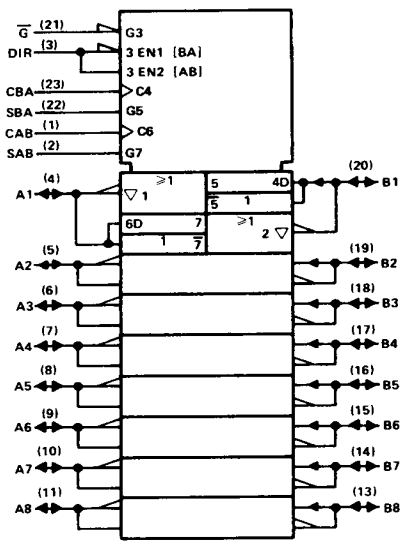
† The data output functions may be enabled or disabled by various signals at the $\overline{G}$ and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols‡

'HCT646



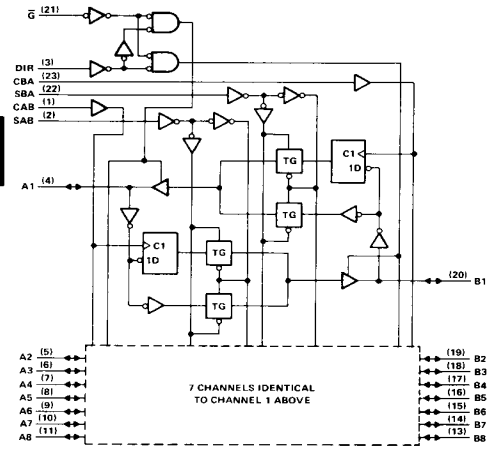
'HCT648



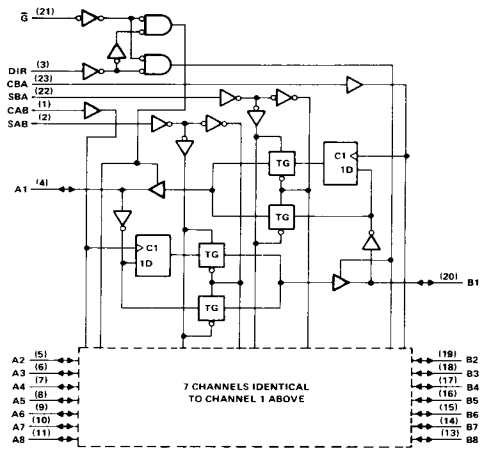
‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for DW, JT, and NT packages.

logic diagrams (positive logic)

'HCT646



'HCT648



Pin numbers shown are for DW, JT, and NT packages.

absolute maximum ratings over operating free-air temperature range†

Supply voltage, V_{CC}	−0.5 V to 7 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±35 mA
Continuous current through V_{CC} or GND pins	±70 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package	260°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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recommended operating conditions

			SN54HCT646 SN54HCT648			SN74HCT646 SN74HCT648			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5	5.5	4.5	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 4.5 V to 5.5 V	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = 4.5 V to 5.5 V	0		0.8	0		0.8	V
V_I	Input voltage		0		V_{CC}	0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	0		V_{CC}	V
t_t	Input transition (rise and fall) times		0		500	0		500	ns
T_A	Operating free-air temperature		−55		125	−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			SN54HCT646 SN54HCT648		SN74HCT646 SN74HCT648		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V_{OH}		V_I = V_{IH} or V_{IL}, I_{OH} = −20 μA	4.5 V	4.4	4.499		4.4		4.4		V
		V_I = V_{IH} or V_{IL}, I_{OH} = −6 mA	4.5 V	3.98	4.30		3.7		3.84		
V_{OL}		V_I = V_{IH} or V_{IL}, I_{OL} = 20 μA	4.5 V		0.001	0.1		0.1		0.1	V
		V_I = V_{IH} or V_{IL}, I_{OL} = 6 mA	4.5 V		0.17	0.26		0.4		0.33	
I_I	Control Inputs	V_I = V_{CC} or 0	5.5 V		±0.1	±100		±1000		±1000	nA
I_{OZ}	A or B	V_O = V_{CC} or 0	5.5 V		±0.01	±0.5		±10		±5	μA
I_{CC}		V_I = V_{CC} or 0, I_O = 0	5.5 V			8		160		80	μA
ΔI_{CC}†		One input at 0.5 V or 2.4 V Other inputs at 0 V or V_{CC}	5.5 V		1.4	2.4		3		2.9	mA
C_i	Control Inputs		4.5 to 5.5 V		3	10		10		10	pF

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V_{CC}	T_A = 25°C		SN54HCT646 SN54HCT648		SN74HCT646 SN74HCT648		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency	4.5 V	0	31	0	22	0	27	MHz
		5.5 V	0	36	0	24	0	29	
t_w	Pulse duration, CBA or CAB high or low	4.5 V	16		23		19		ns
		5.5 V	14		21		17		
t_{su}	Setup time, A before CAB† or B before CBA†	4.5 V	20		30		25		ns
		5.5 V	18		27		23		
t_h	Hold time, A after CAB† or B after CBA†	4.5 V	5		5		5		ns
		5.5 V	5		5		5		

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 50 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT646 SN54HCT648		SN74HCT646 SN74HCT648		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			4.5 V	31	54		22		27		MHz
			5.5 V	36	64		24		29		
t_{pd}	CBA or CAB	A or B	4.5 V		18	36		54		45	ns
			5.5 V		16	32		49		41	
t_{pd}	A or B	B or A	4.5 V		14	27		41		34	ns
			5.5 V		12	24		37		31	
t_{pd}	SBA or SAB†	A or B	4.5 V		20	38		57		48	ns
			5.5 V		17	34		51		43	
t_{en}	$\overline{G}$	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_{dis}	$\overline{G}$	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_{en}	DIR	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_{dis}	DIR	A or B	4.5 V		25	49		74		61	ns
			5.5 V		22	44		67		55	
t_t		Any	4.5 V		9	12		18		15	ns
			5.5 V		7	11		16		14	

C_{pd}	Power dissipation capacitance	No load, T_A = 25°C	50 pF typ

switching characteristics over recommended operating free-air temperature range (unless otherwise noted), C_L = 150 pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			SN54HCT646 SN54HCT648		SN74HCT646 SN74HCT648		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{pd}	CBA or CAB	A or B	4.5 V		24	53		80		66	ns
			5.5 V		22	47		52		60	
t_{pd}	A or B	B or A	4.5 V		22	44		67		55	ns
			5.5 V		20	39		60		50	
t_{pd}	SBA or SAB†	A or B	4.5 V		26	55		83		69	ns
			5.5 V		24	49		74		62	
t_{en}	$\overline{G}$	A or B	4.5 V		33	66		100		87	ns
			5.5 V		22	59		90		74	
t_{en}	DIR	A or B	4.5 V		33	66		100		87	ns
			5.5 V		22	59		90		74	
t_t		Any	4.5 V		17	42		63		53	ns
			5.5 V		14	38		57		48	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.
†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

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