CY62168EV30 MoBL®

16-Mbit (2 M × 8) Static RAM

Features

- Very high speed: 45 ns
- Wide voltage range: 2.20 V to 3.60 V
- Ultra low standby power
  - Typical standby current: 1.5 µA
  - Maximum standby current: 12 µA
- Ultra low active power
  - Typical active current: 2.2 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2 and $\overline{OE}$ features
- Automatic power-down when deselected
- CMOS for optimum speed/power
- Offered in Pb-free 48-ball FBGA package. For Pb-free 48-pin TSOP I package, refer to CY62167EV30 data sheet.

Functional Description

The CY62168EV30 is a high performance CMOS static RAM organized as 2 M words by 8-bits. This device features advanced circuit design to provide an ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption by 90% when addresses are not toggling. Placing the device into standby mode reduces power consumption by more than 99% when deselected (Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 (CE_2) LOW). The input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when: the device is deselected (Chip Enable 1 ($\overline{CE}_1$) HIGH or Chip Enable 2 (CE_2) LOW), outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress (Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and $\overline{WE}$ LOW).

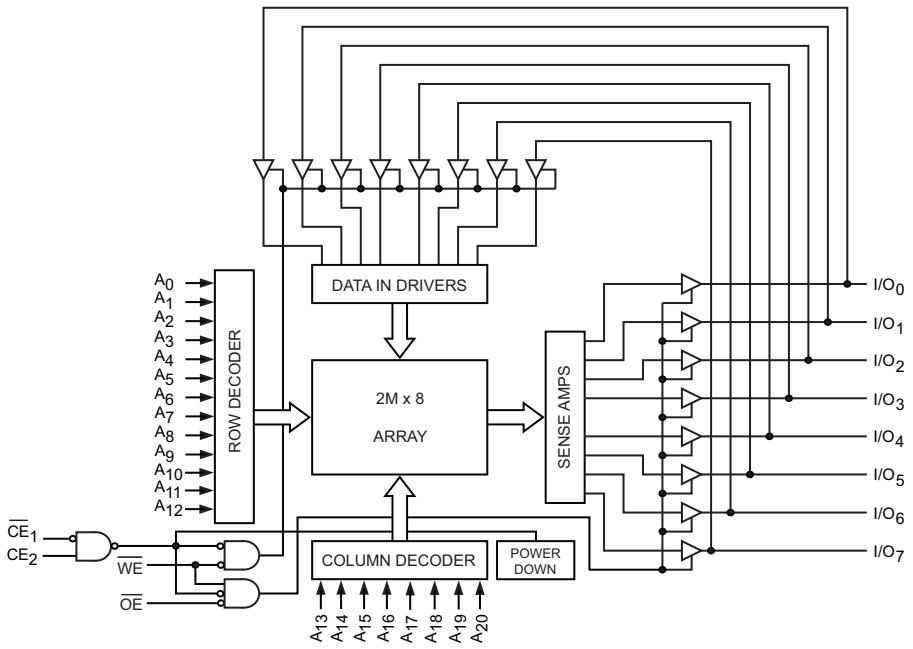
Write to the device by taking Chip Enable 1 ($\overline{CE}_1$) LOW and Chip Enable 2 (CE_2) HIGH and the Write Enable (WE) input LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{20}).

Read from the device by taking Chip Enable 1 ($\overline{CE}_1$) and Output Enable ($\overline{OE}$) LOW and Chip Enable 2 (CE_2) HIGH while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW). See the Truth Table on page 11 for a complete description of read and write modes.

For a complete list of related documentation, click here.

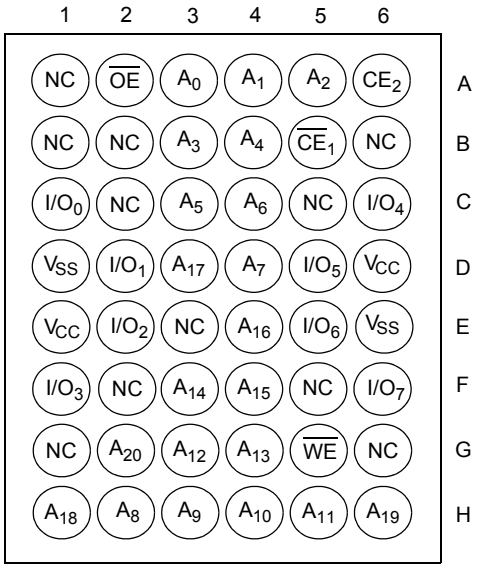
Logic Block Diagram



Contents

Pin Configuration

Figure 1. 48-ball FBGA pinout (Top View) [1]



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{max}			
	Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62168EV30LL	2.2	3.0	3.6	45	2.2	4.0	25	30	1.5	12

Notes
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential [3, 4] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs in high Z state [3, 4] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage [3, 4] .....–0.3 V to V_{CC}(max) + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Range	Ambient Temperature (T_A) [5]	V_{CC} [6]
Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

DC Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions		CY62168EV30-45			Unit
				Min	Typ [7]	Max	
V_{OH}	Output HIGH voltage	$2.2 \le V_{CC} \le 2.7$	I_{OH} = –0.1 mA	2.0	–	–	V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = –1.0 mA	2.4	–	–	
V_{OL}	Output LOW voltage	$2.2 \le V_{CC} \le 2.7$	I_{OL} = 0.1 mA	–	–	0.4	V
		$2.7 \le V_{CC} \le 3.6$	I_{OH} = 2.1 mA	–	–	0.4	
V_{IH}	Input HIGH voltage	$2.2 \le V_{CC} \le 2.7$		1.8	–	V_{CC} + 0.3	V
		$2.7 \le V_{CC} \le 3.6$		2.2	–	V_{CC} + 0.3	
V_{IL}	Input LOW voltage	$2.2 \le V_{CC} \le 2.7$		–0.3	–	0.6	V
		$2.7 \le V_{CC} \le 3.6$		–0.3	–	0.8	
I_{IX}	Input leakage current	$GND \le V_I \le V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	$GND \le V_O \le V_{CC}$, Output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	$f = f_{MAX} = 1/t_{RC}$	V_{CC} = 3.6 V, I_{OUT} = 0 mA, CMOS level	–	25	30	mA
		f = 1 MHz		–	2.2	4.0	
I_{SB1}[8]	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1 \ge V_{CC} - 0.2$ V or $CE_2 \le 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V, $V_{IN} \le 0.2$ V, f = f_{MAX} (address and data only), f = 0 ($\overline{OE}$, $\overline{WE}$)		–	1.5	12	µA
I_{SB2}[8]	Automatic CE power-down current – CMOS inputs	$\overline{CE}_1 \ge V_{CC} - 0.2$ V or $CE_2 \le 0.2$ V, $V_{IN} \ge V_{CC} - 0.2$ V or $V_{IN} \le 0.2$ V, f = 0, V_{CC} = 3.6 V		–	1.5	12	µA

Notes

3. V_{IL}(min) = –2.0 V for pulse durations less than 20 ns.
4. V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. T_A is the "Instant-On" case temperature.
6. Full device AC operation assumes a 100 µs ramp time from 0 to V_{CC}(min) and 200 µs wait time after V_{CC} stabilization.
7. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC}(typ), T_A = 25 °C.
8. Chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

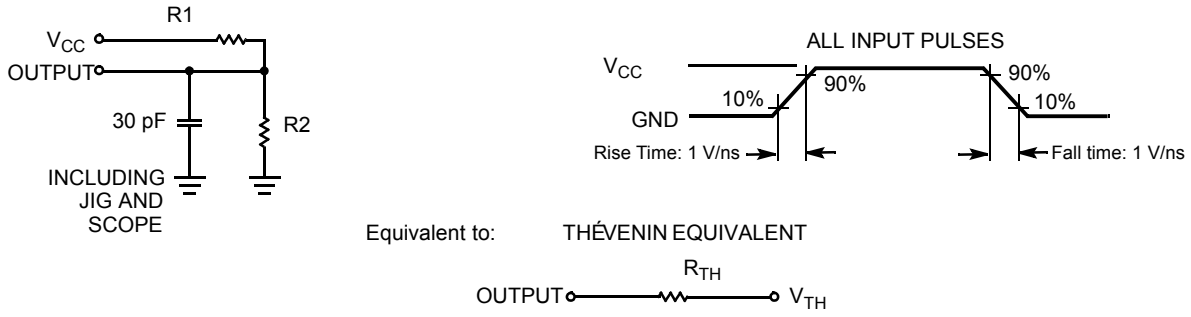
Parameter [9]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	8	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [9]	Description	Test Conditions	48-ball FBGA	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	52.3	°C/W
Θ_{JC}	Thermal resistance (junction to case)		7.91	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms



Parameters	2.5 V (2.2 V to 2.7 V)	3.0 V (2.7 V to 3.6 V)	Unit
R1	16600	1103	Ω
R2	15400	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.2	1.75	V

Note
9. Tested initially and after any design or process changes that may affect these parameters.

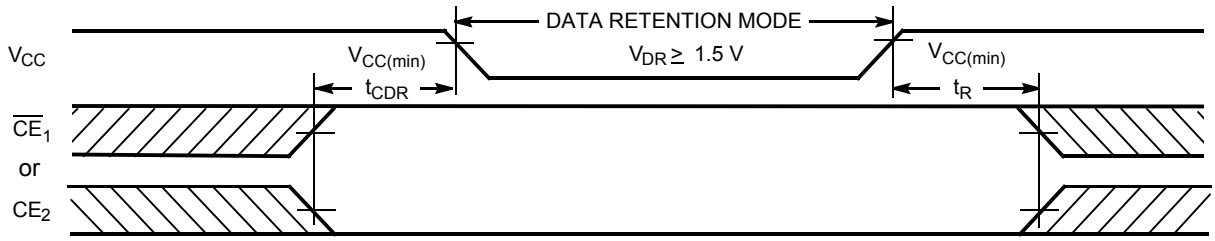
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions	Min	Typ [10]	Max	Unit
V_{DR}	V_{CC} for data retention		1.5	–	3.6	V
I_{CCDR}[11]	Data retention current	V_{CC} = 1.5 V $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	–	–	10	µA
t_{CDR}[12]	Chip deselect to data retention time		0	–	–	ns
t_R[13]	Operation recovery time		45	–	–	ns

Data Retention Waveform

Figure 3. Data Retention Waveform



Notes

10. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC}(typ)$, T_A = 25 °C.
11. Chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
12. Tested initially and after any design or process changes that may affect these parameters.
13. Full Device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC}(min) \geq 100$ µs or stable at $V_{CC}(min) \geq 100$ µs.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to low Z [16]	10	–	ns
t_{HZCE}	$\overline{CE}_1$ HIGH or CE_2 LOW to high Z [16, 17]	–	18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to power-up	0	–	ns
t_{PD}	$\overline{CE}_1$ HIGH or CE_2 LOW to power-down	–	45	ns
Write Cycle [18, 19]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [16]	10	–	ns

Notes

14. In an earlier revision of this device, under a specific application condition, READ and WRITE operations were limited to switching of the chip enable signal as described in the Application Note AN66311. However, the issue has been fixed and in production now, and hence, this Application Note is no longer applicable. It is available for download on our website as it contains information on the date code of the parts, beyond which the fix has been in production.
15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in Figure 2 on page 5.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
19. The minimum write cycle pulse width for Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) should be equal to sum of t_{SD} and t_{HZWE}.

Switching Waveforms

Figure 4. Read Cycle No. 1 (Address Transition Controlled) [20, 21]

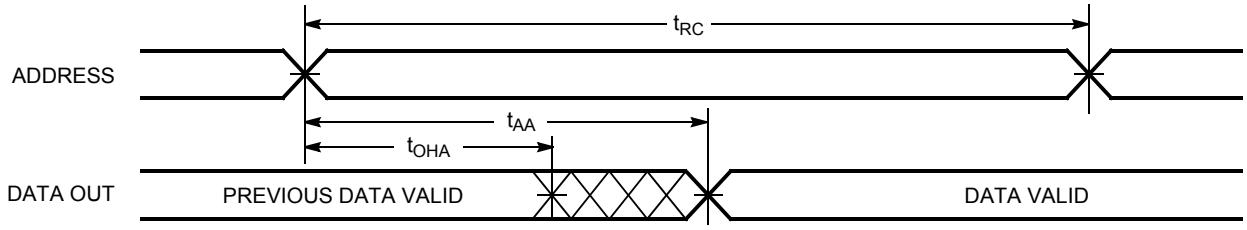
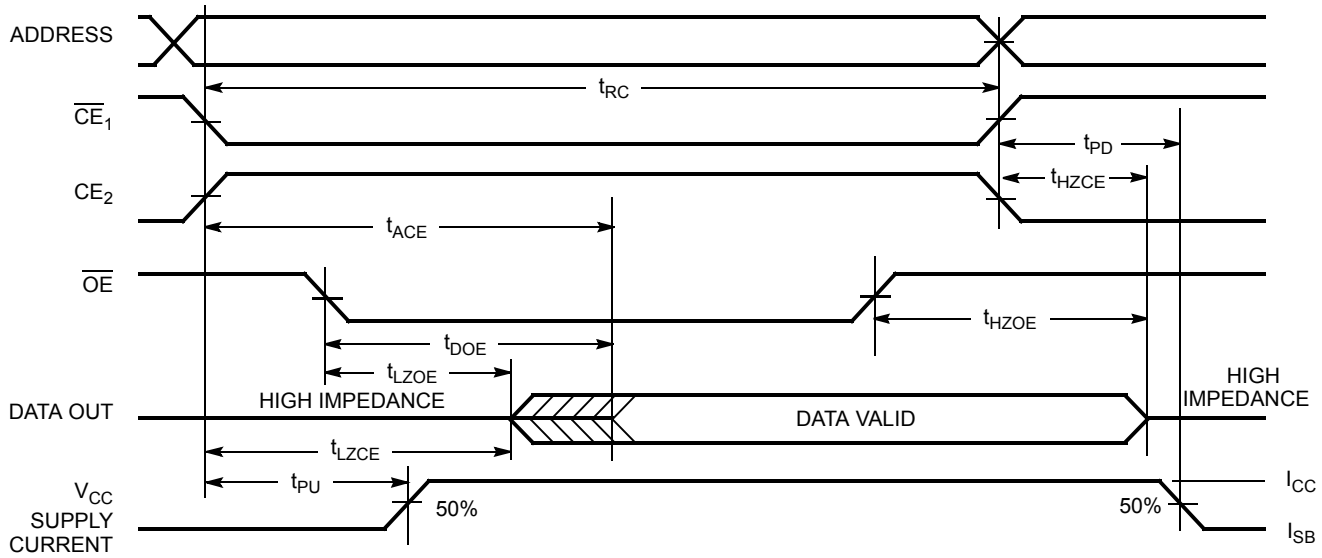


Figure 5. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22]



Notes
20. The device is continuously selected. $\overline{OE}$, $\overline{CE}_1$ = V_{IL}, and CE_2 = V_{IH}.
21. $\overline{WE}$ is HIGH for read cycle.
22. Address valid before or similar to $\overline{CE}_1$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1 ($\overline{WE}$ Controlled) [23, 24, 25]

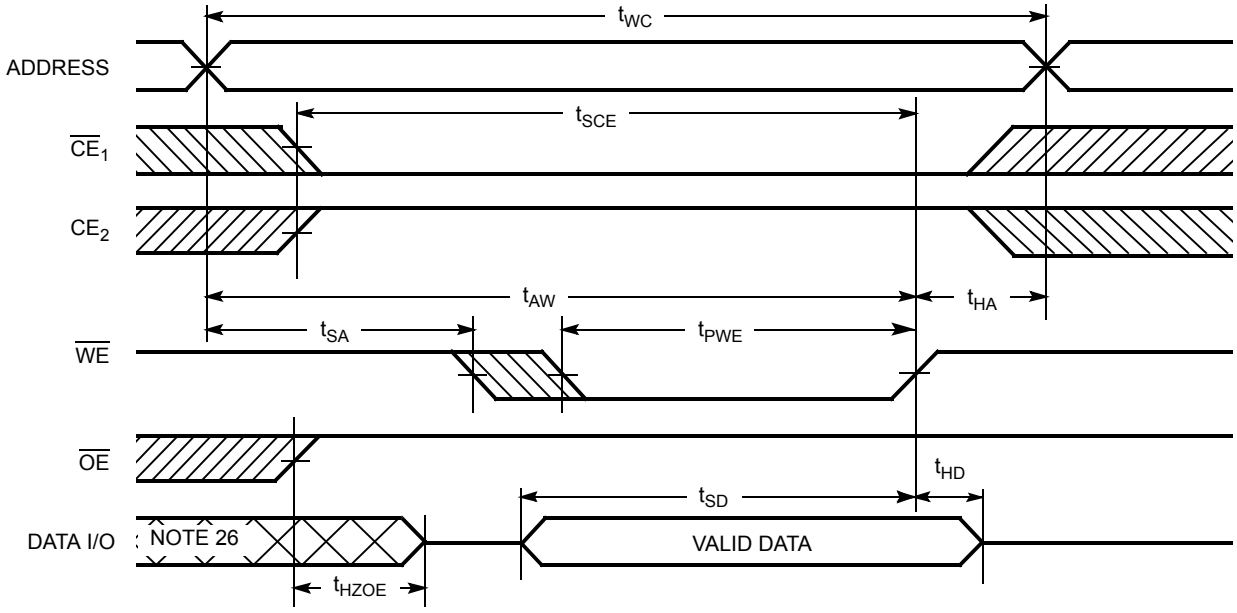
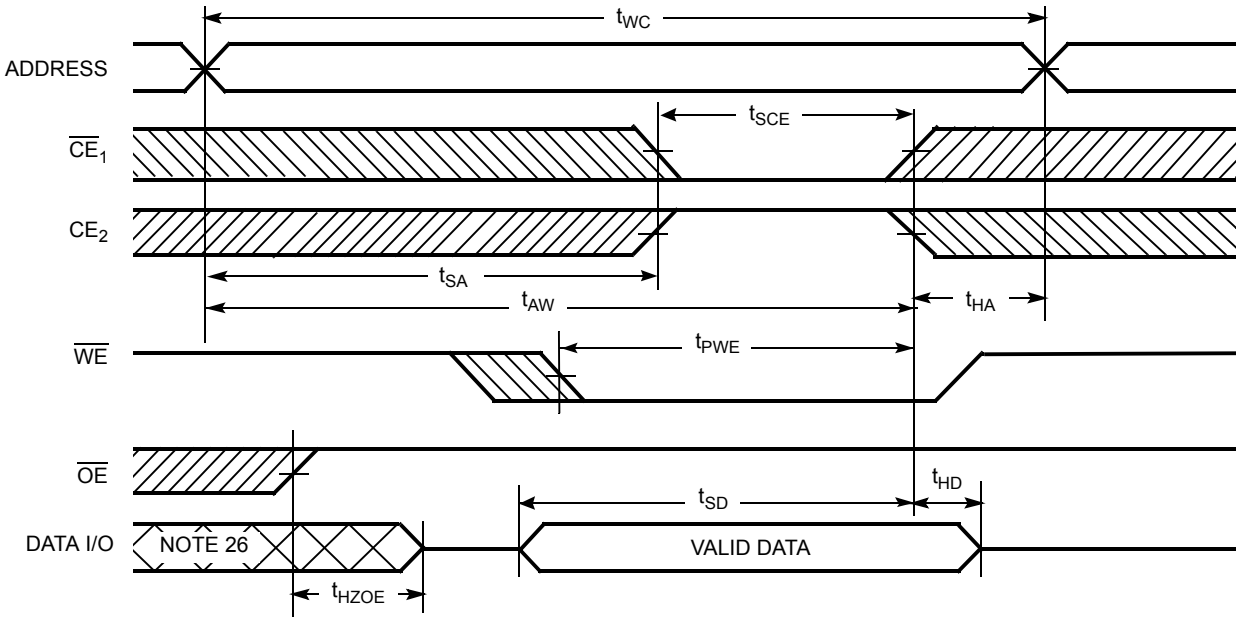


Figure 7. Write Cycle No. 2 ($\overline{CE_1}$ or CE_2 Controlled) [23, 24, 25]

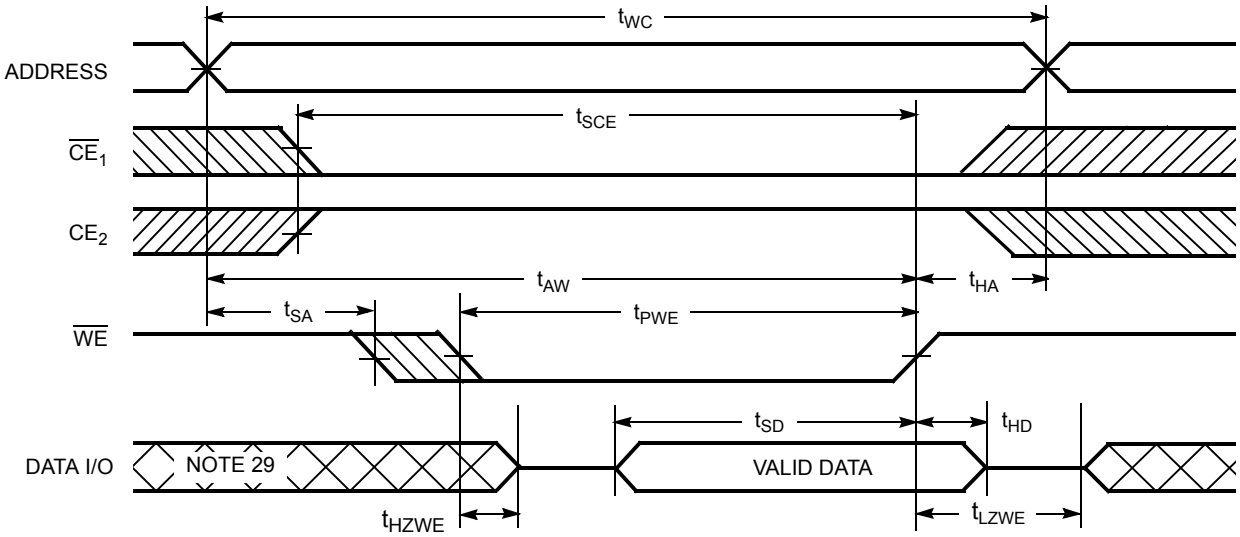


Notes

23. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE_1}$ = V_{IL}, and CE_2 = V_{IH}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
24. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
25. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
26. During this period the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [27, 28]



Notes
27. If $\overline{CE}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE}$ = V_{IH}, the output remains in a high impedance state.
28. The minimum write cycle pulse width should be equal to sum of t_{SD} and t_{HZWE}.
29. During this period the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	I/O	Mode	Power
H	X[30]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
X[30]	L	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	H	L	Data out (I/O_0–I/O_7)	Read	Active (I_{CC})
L	H	H	H	High Z	Output disabled	Active (I_{CC})
L	H	L	X	Data in (I/O_0–I/O_7)	Write	Active (I_{CC})

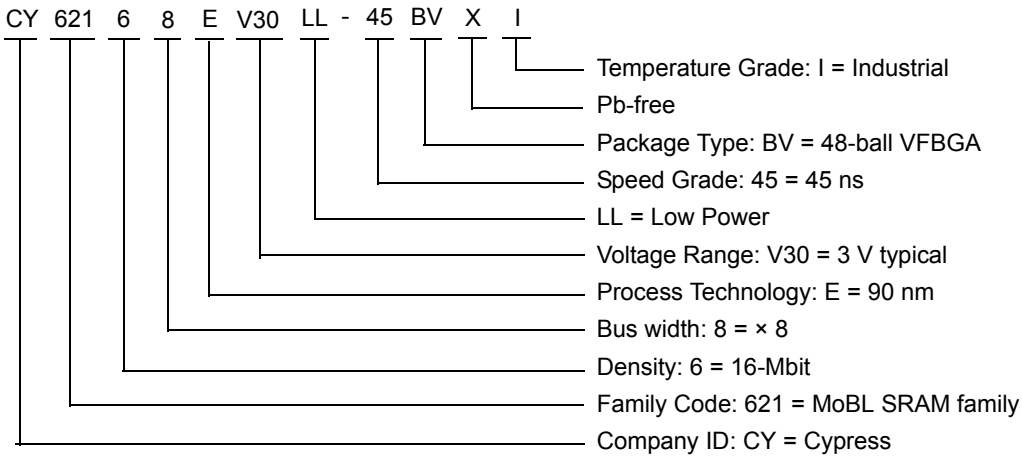
Note
30. The 'X' (Do not care) state for the chip enables in the truth table refers to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

The below table lists the CY62168EV30 MoBL key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at http://www.cypress.com/products.

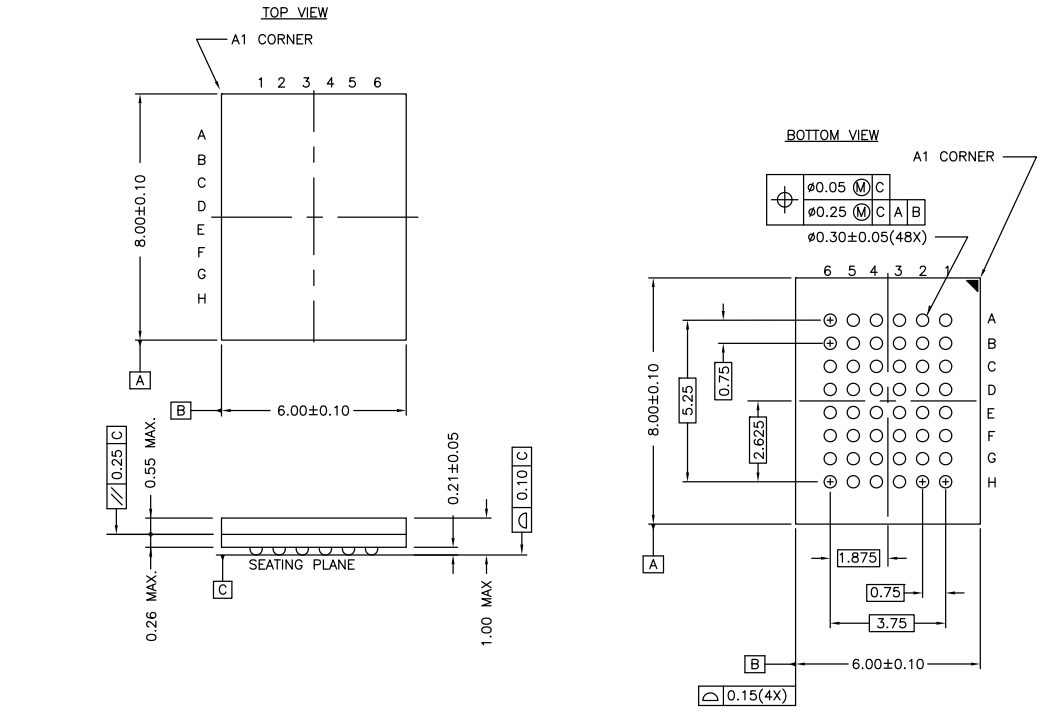
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62168EV30LL-45BVXI	51-85150	48-ball VFBGA (Pb-free)	Industrial

Ordering Code Definitions



Package Diagram

Figure 9. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48 Package Outline, 51-85150



NOTE:
PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 *H

Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
FBGA	Fine-Pitch Ball Grid Array
I/O	Input/Output
$\overline{OE}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small Outline Package
VFBGA	Very Fine-Pitch Ball Grid Array
$\overline{WE}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
µA	microampere
µs	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY62168EV30 MoBL®, 16-Mbit (2 M × 8) Static RAM Document Number: 001-07721				
Rev.	**ECN No.**	**Orig. of Change**	**Issue Date**	**Description of Change**
**	457686	NXR	See ECN	New data sheet.
*A	464509	NXR	See ECN	Removed TSOP I package related information in all instances across the document. Updated Features: Added Note “For 48-pin TSOP I pin configuration and ordering information, please refer to CY62167EV30 Data sheet.” and referred the same note in 48-pin TSOP I package. Updated DC Electrical Characteristics: Changed typical value of I_{CC} parameter from 15 mA to 22 mA corresponding to Test Condition “f = f_{max}”. Changed maximum value of I_{CC} parameter from 40 mA to 25 mA corresponding to Test Condition “f = f_{max}”. Changed typical value of I_{CC} parameter from 2 mA to 2.2 mA corresponding to Test Condition “f = 1 MHz”. Changed typical value of I_{SB2} parameter from 1.3 µA to 1.5 µA. Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 8.5 µA to 8 µA. Updated Ordering Information (Updated part numbers).
*B	1138883	VKN	See ECN	Changed status from Preliminary to Final. Updated Features: Removed Note “For 48-pin TSOP I pin configuration and ordering information, please refer to CY62167EV30 Data sheet.” and its reference. Added “For Pb-free 48-pin TSOP I package, refer to CY62167EV30 data sheet.” in the last bullet point. Updated DC Electrical Characteristics: Changed typical value of I_{CC} parameter from 22 mA to 25 mA corresponding to Test Condition “f = f_{max}”. Changed maximum value of I_{CC} parameter from 25 mA to 30 mA corresponding to Test Condition “f = f_{max}”. Changed maximum value of I_{CC} parameter from 2.8 mA to 4.0 mA corresponding to Test Condition “f = 1 MHz”. Changed maximum value of I_{SB1} and I_{SB2} parameters from 8.5 µA to 12 µA. Added Note 8 and referred the same note in I_{SB1} and I_{SB2} parameters. Updated Data Retention Characteristics: Changed maximum value of I_{CCDR} parameter from 8 µA to 10 µA. Added Note 11 and referred the same note in I_{CCDR} parameter.
*C	2934385	VKN	06/03/10	Updated Functional Description: Corrected typo in the section. Updated Operating Range: Updated Note 6 (Changed wait time after VCC stabilization from 100 µs to 200 µs). Updated Truth Table: Added Note 30 and referred the same note in “$\overline{CE}_1$” column and “CE_2” column. Updated Package Diagram. Updated to new template.
*D	3279426	RAME	06/10/2011	Updated Functional Description: Removed the Note “For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines.” in page 1 and its reference. Updated Package Diagram. Updated to new template.

Document History Page (continued)

Document Title: CY62168EV30 MoBL®, 16-Mbit (2 M × 8) Static RAM Document Number: 001-07721				
Rev.	**ECN No.**	**Orig. of Change**	**Issue Date**	**Description of Change**
*E	4100078	VINI	08/20/2013	Updated Switching Characteristics: Added Note 14 and referred the same note in “Parameter” column. Updated Package Diagram: spec 51-85150 – Changed revision from *F to *H. Updated to new template.
*F	4126351	NILE	09/17/2013	Updated Maximum Ratings: Updated Note 3.
*G	4434949	VINI	07/09/2014	Updated Switching Characteristics: Added Note 19 and referred the same note in “Write Cycle”. Updated Switching Waveforms: Added Note 28 and referred the same note in Figure 8. Completing Sunset Review.
*H	4576406	VINI	01/16/2015	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end. Updated to new template.
*I	4841338	VINI	07/20/2015	Updated Maximum Ratings: Referred Notes 3, 4 in “Supply Voltage to Ground Potential”. Updated Thermal Resistance: Replaced “two-layer” with “four-layer” in “Test Conditions” column. Changed value of Θ_{JA} parameter from 55 °C/W to 52.3 °C/W corresponding to 48-ball FBGA package. Changed value of Θ_{JC} parameter from 16 °C/W to 7.91 °C/W corresponding to 48-ball FBGA package. Completing Sunset Review.

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