

315/433MHz FSK/FM/ASK

Double-Conversion Superheterodyne Receiver

Features

- Double superhet architecture for high degree of image rejection
- FSK for digital data and FM reception for analog signal transmission
- FM/FSK demodulation either with phase-coincidence or PLL demodulator
- Low current consumption in active mode and very low standby current
- Switchable LNA gain for improved dynamic range
- RSSI allows signal strength indication and ASK detection
- Surface mount package LQFP32

Ordering Information

Part No.	Temperature Range	Package
TH71102	-40 °C to 85°C	LQFP32

Application Examples

- General digital and analog 315 MHz or 433 MHz ISM band usage
- Low-power telemetry
- Alarm and security systems
- Keyless car and central locking
- Pagers

Technical Data Overview

- Input frequency range: 300 MHz to 500 MHz
- Power supply range: 2.3 V to 5.5 V at ASK and 2.5 V to 5.5 V at FSK
- Temperature range: -40 °C to +85 °C
- Operating current: 6.5 mA at low gain and 7.8 mA at high gain mode
- Standby current: 50 nA
- Sensitivity: -111 dBm¹⁾ with 40 kHz second IF filter BW (incl. SAW front-end filter loss)
- Sensitivity: -104 dBm²⁾ with 150 kHz second IF filter BW (incl. SAW front-end filter loss)
- Range of first IF: 10 MHz to 80 MHz
- Range of second IF: 455 kHz to 21.4 MHz
- Maximum input level: -10 dBm at ASK and 0 dBm at FSK
- Input impedance: 50 Ω
- Image rejection: > 65 dB (e.g. with SAW front-end filter and at 10.7 MHz 2nd IF)
- Spurious emission: < -70 dBm
- RSSI range: 70 dB
- Frequency deviation range: ±5 kHz to ±120 kHz
- Maximum data rate: 80 kbit/s NRZ
- Maximum analog modulation frequency: 15 kHz

¹⁾ at ± 8 kHz FSK deviation, BER = 3·10⁻³ and phase-coincidence demodulation

²⁾ at ± 50 kHz FSK deviation, BER = 3·10⁻³ and phase-coincidence demodulation

General Description

The TH71102 receiver IC consists of the following building blocks:

- PLL synthesizer (PLL SYNTH) for generation of the first and second local oscillator signals LO1 and LO2
- Parts of the PLL SYNTH are the high-frequency VCO1, the feedback dividers DIV_8 and DIV_2, a phase-frequency detector (PFD) with charge pump (CP) and a crystal-based reference oscillator (RO)
- Low-noise amplifier (LNA) for high-sensitivity RF signal reception
- First mixer (MIX1) for down-conversion of the RF signal to the first IF (IF1)
- second mixer (MIX2) for down-conversion of the IF1 to the second IF (IF2)
- IF amplifier (IFA) to amplify and limit the IF2 signal and for RSSI generation
- Phase coincidence demodulator (DEMODO) with third mixer (MIX3) to demodulate the IF signal
- Operational amplifier (OA) for data slicing, filtering and ASK detection
- Bias circuitry for bandgap biasing and circuit shutdown

With the TH71102 receiver chip, various circuit configurations can be arranged in order to meet a number of different customer requirements. For FM/FSK reception the IF tank used in the phase coincidence demodulator can be constituted either by a ceramic resonator or an LC tank (optionally with a varactor diode to create an AFC circuit). In ASK configuration, the RSSI signal is feed to an ASK detector, which is constituted by the operational amplifier.

Demodulation	Type of receiver
FM / FSK	narrow-band RX with ceramic demodulation tank
FM / FSK	wide-band RX with LC demodulation tank
ASK	RX with RSSI-based demodulation

The superheterodyne configuration is double conversion where MIX1 and MIX2 are driven by the internal local oscillator signals LO1 and LO2, respectively. This allows a high degree of image rejection, achieved in conjunction with an RF frontend filter. Efficient RF frontend filtering is realized by using a SAW, ceramic or helix filter in front of the LNA and by adding an LC filter at the LNA output.

A single-conversion variant, called TH71101, is also available. Both RXICs have the same die. At the TH71101 the second mixer MIX2 operates as an amplifier.

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Block Diagram

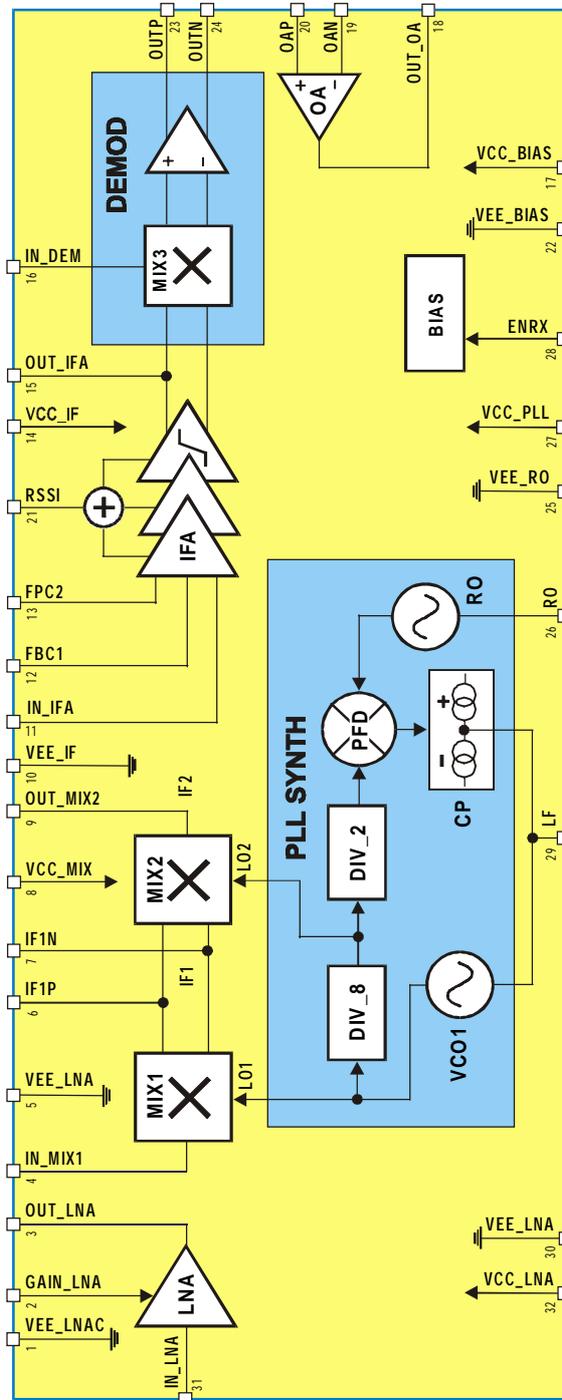


Fig. 1: TH71102 block diagram

Frequency Planning

Frequency planning is straightforward for single-conversion applications because there is only one IF that might be chosen, and then the only possible choice is low-side or high-side injection of the LO1 signal (which is now the one and only LO signal in the receiver).

The receiver's double-conversion architecture requires careful frequency planning. Besides the desired RF input signal, there are a number of spurious signals that may cause an undesired response at the output. Among them are the image of the RF signal (that must be suppressed by the RF front-end filter), spurious signals injected to the first IF (IF1) and their images which could be mixed down to the same second IF (IF2) as the desired RF signal (they must be suppressed by the LC filter at IF1 and/or by low-crosstalk design).

By configuring the TH71102 for double conversion and using its internal PLL synthesizer with fixed feedback divider ratios of $N1 = 8$ (DIV_8) and $N2 = 2$ (DIV_2), four types of down-conversion are possible: low-side injection of LO1 and LO2 (**low-low**), LO1 low-side and LO2 high-side (**low-high**), LO1 high-side and LO2 low-side (**high-low**) or LO1 and LO2 high-side (**high-high**). The following table summarizes some equations that are useful to calculate the crystal reference frequency (REF), the first IF (IF1) and the VCO1 or first LO frequency (LO1), respectively, for a given RF and second IF (IF2).

Injection type	high-high	low-low	high-low	low-high
REF	$(RF - IF2)/14$	$(RF - IF2)/18$	$(RF + IF2)/14$	$(RF + IF2)/18$
LO1	$16 \bullet REF$	$16 \bullet REF$	$16 \bullet REF$	$16 \bullet REF$
IF1	$LO1 - RF$	$RF - LO1$	$LO1 - RF$	$RF - LO1$
LO2	$2 \bullet REF$	$2 \bullet REF$	$2 \bullet REF$	$2 \bullet REF$
IF2	$LO2 - IF1$	$IF1 - LO2$	$IF1 - LO2$	$LO2 - IF1$

The following table depicts generated, desired, possible images and some undesired signals considering the examples of 315 MHz and 433.6 MHz RF reception at $IF2 = 10.7$ MHz.

Signal type	RF = 315 MHz	RF = 315 MHz	RF = 315 MHz	RF = 315 MHz	RF = 433.6 MHz	RF = 433.6 MHz	RF = 433.6 MHz	RF = 433.6 MHz
Injection type	high-high	low-low	high-low	low-high	high-high	low-low	high-low	low-high
REF / MHz	21.73571	16.90556	23.26429	18.09444	30.20714	23.49444	31.73571	24.68333
LO1 / MHz	347.77143	270.48889	372.22857	289.51111	483.31429	375.91111	507.77143	394.93333
IF1 / MHz	32.77143	44.51111	57.22857	25.48889	49.71429	57.68889	74.17143	38.66667
LO2 / MHz	43.47143	33.81111	46.52857	36.18889	60.41429	46.98889	63.47143	49.36667
RF image/MHz	380.54286	225.97778	429.45714	264.02222	533.02857	318.22222	581.94286	356.26667
IF1 image/MHz	54.17143	23.11111	35.82857	46.88889	71.11429	36.28889	52.77143	60.06667

The selection of the reference crystal frequency is based on some assumptions. As for example: the first IF and the image frequencies should not be in a radio band where strong interfering signals might occur (because they could represent parasitic receiving signals), the LO1 signal should be in the range of 300 MHz to 450 MHz (because this is the optimum frequency range of the VCO1). Furthermore the first IF should be as high as possible to achieve highest RF image rejection. The columns in bold depict the selected frequency plans to receive at 315 MHz and 433.6 MHz, respectively.

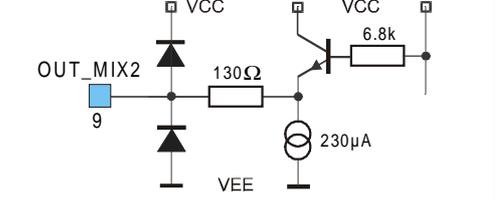
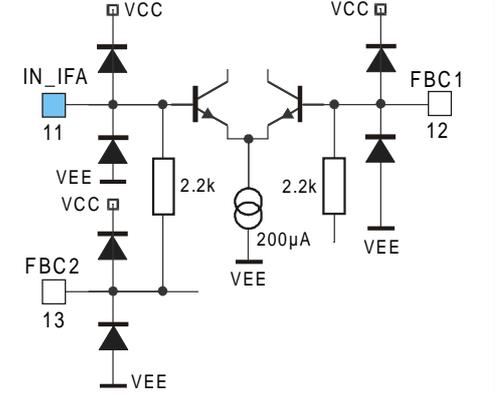
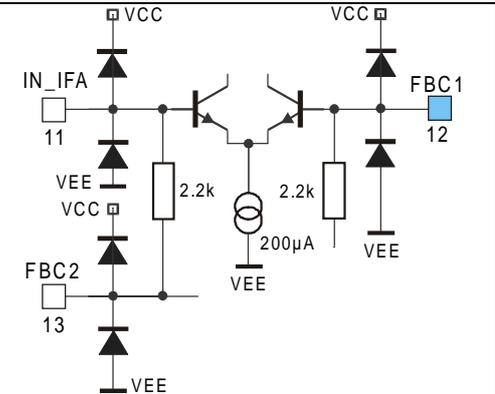
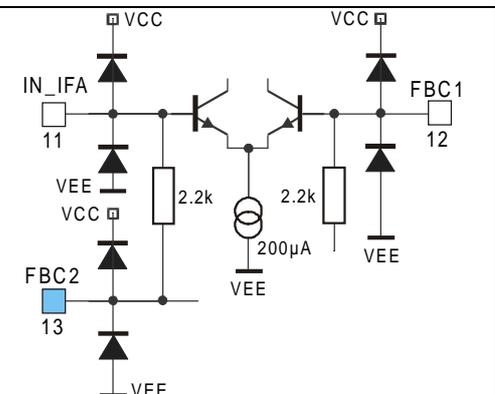
Pin Definition and Description

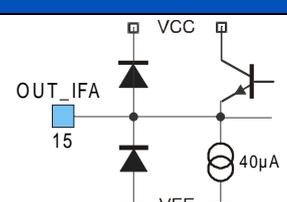
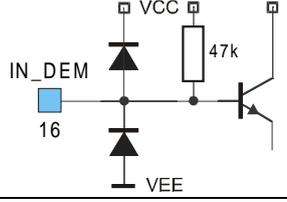
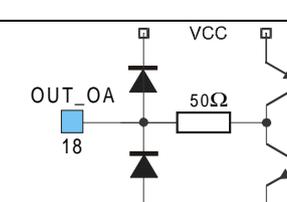
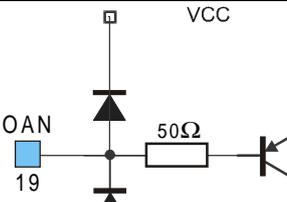
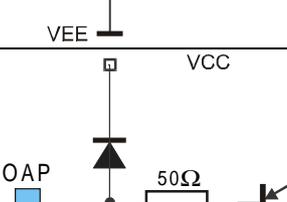
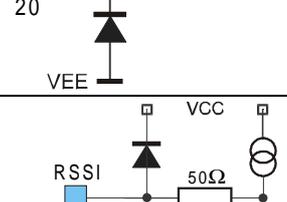
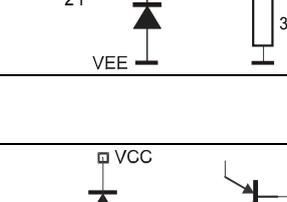
Pin No.	Name	I/O Type	Functional Schematic	Description
1	VEE_LNAC	ground		ground of LNA core (cascode)
2	GAIN_LNA	analog input		LNA gain control (CMOS input with hysteresis)
3	OUT_LNA	analog output		LNA open-collector, connection to external LC tank at RF
4	IN_MIX1	analog input		MIX1 input, approx. 33Ω single-ended
5	VEE_LNA	ground		LNA biasing ground
6	IF1P	analog I/O		open-collector output, connection to external LC tank at IF1
7	IF1N	analog I/O		open-collector output, connection to external LC tank at IF1
8	VCC_MIX	supply		MIX1 and MIX2 positive supply

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Pin No.	Name	I/O Type	Functional Schematic	Description
9	OUT_MIX2	analog output		MIX2 output, approx. 330Ω output impedance
10	VEE_IF	ground		ground for MIX2, IFA and DEMOD
11	IN_IFA	analog input		IFA input, approx. 2.2kΩ input impedance
12	FBC1	analog I/O		external IFA feedback capacitor
13	FBC2	analog I/O		external IFA feedback capacitor
14	VCC_IF	supply		positive supply for IFA, DEMOD

Pin No.	Name	I/O Type	Functional Schematic	Description
15	OUT_IFA	analog I/O		IFA output and MIX3 input (DEMOD)
16	IN_DEM	analog input		demodulator input, to MIX3 core
17	VCC_BIAS	supply		positive supply of general bias system and OA
18	OUT_OA	analog output		OA output, 40uA current drive capability
19	OAN	analog input		negative OA input
20	OAP	analog input		positive OA input
21	RSSI	analog output		RSSI output, for RSSI and ASK detection, approx. 36kΩ output impedance
22	VEE_BIAS	ground		ground for general bias system and OA
23	OUTP	analog output		FSK/FM positive output, high-impedance

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Pin No.	Name	I/O Type	Functional Schematic	Description
24	OUTN	analog		FSK/FM negative output, high-impedance
25	VEE_RO	ground		ground of dividers, PFD and RO
26	RO	analog input		RO input, colpitts type oscillator topology
27	VCC_PLL	supply		positive supply of RO, DIV, PFD and charge pump
28	ENRX	digital input		mode control input (CMOS Input)
29	LF	analog output		CP output and VCO1 control input
30	VEE_LNA	ground		LNA biasing ground
31	IN_LNA	analog input		LNA input, approx. 26Ω single-ended
32	VCC_LNA	supply		positive supply of LNA biasing

Technical Data

Mode Configurations

ENRX	Mode	Description
0	SBY	standby mode
1	ON	entire chip active

Note: ENRX are pulled down internally

LNA Gain Control

V_{GAIN_LNA}	Mode	Description
< 0.8 V	HIGH GAIN	LNA set to high gain by voltage at GAIN_LNA
> 1.4 V	LOW GAIN	LNA set to low gain by voltage at GAIN_LNA

Note: hysteresis between gain modes to ensure stability

Absolute Maximum Ratings

Parameter	Symbol	Condition / Note	Min	Max	Unit
Supply voltage	V_{CC}		0	7.0	V
Analog/digital control voltage	V_{CTRL}		-0.3	$V_{CC}+0.3$	V
Input RF level	P_{imax}	no damage		10	dBm
Storage temperature	T_{STG}		-40	+125	°C
Electrostatic discharge	ESD	human body model, MIL STD 883D method 3015.7	1.0		kV

Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage at ASK	$V_{CC, ASK}$		2.3	5.5	V
Supply voltage at FSK/FM	$V_{CC, FSK}$		2.5	5.5	V
Operating temperature	T_a		-40	+85	°C
Input frequency	f_i		300	500	MHz
Frequency deviation	Δf	at FM or FSK	± 5	± 120	kHz
FSK data rate	R_{FSK}	NRZ		40	kbit/s
FM bandwidth	f_m			15	kHz
ASK data rate	R_{ASK}	NRZ		80	kbit/s

DC Characteristics

all parameters under normal operating conditions, unless otherwise stated

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Standby current	I_{SBY}	ENRX=0			50	nA
Total supply current at low gain	$I_{\text{cc, tot}}$	ENRX=1, $V_{\text{GAIN_LNA}} > 1.4 \text{ V}$	6.2	6.5	6.8	mA
Total supply current at high gain	$I_{\text{cc, tot}}$	ENRX=1, $V_{\text{GAIN_LNA}} < 0.8 \text{ V}$	7.4	7.8	8.2	mA
Opamp input offset voltage	V_{offs}		-5		5	mV
Opamp input offset current	I_{offs}		-30		30	nA
Opamp input bias current	I_{bias}		-80		80	nA

AC System Characteristics

all parameters under normal operating conditions, unless otherwise stated;

all parameters based on test circuits for FSK (Fig. 2), FM (Fig. 3) and ASK (Fig. 4), respectively;
RF at 433.6 MHz, second IF at 10.7 MHz

Parameter	Symbol	Condition	Min	Typ	Max	Unit
start-up time – FSK/FM	T_{FSK}	ENRX from 0 to 1, valid data at output		1.0		ms
start-up time – ASK	T_{ASK}	depends on ASK detector time constant, valid data at output			$R3 \cdot C1$ $4 +$ T_{FSK}	s
input sensitivity – FSK (narrow band)	$P_{\text{min, n}}$	$B_{\text{IF2}} = 40\text{kHz}$ $\Delta f = \pm 15\text{kHz}$ (FSK/FM) note 1		-111		dBm
input sensitivity – FSK (wide band)	$P_{\text{min, w}}$	$B_{\text{IF2}} = 150\text{kHz}$ $\Delta f = \pm 50\text{kHz}$ (FSK/FM) note 1		-104		dBm
input sensitivity – ASK (narrow band)	$P_{\text{minA, n}}$	$B_{\text{IF2}} = 40\text{kHz}$ note 1		-109		dBm
input sensitivity – ASK (wide band)	$P_{\text{minA, w}}$	$B_{\text{IF2}} = 150\text{kHz}$ note 1		-106		dBm
maximum input signal – FSK/FM	$P_{\text{max, FM}}$	note 1 LNA at LOW GAIN		0		dBm
maximum input signal – ASK	$P_{\text{max, ASK}}$	note 1 LNA at LOW GAIN		-10		dBm
spurious emission	P_{spur}				-70	dBm
image rejection	ΔP_{imag}			65		dB
blocking immunity	ΔP_{block}	$\Delta f_{\text{block}} > \pm 2\text{MHz}$ note 2		57		dB

Notes: 1. $\text{BER} \leq 3 \cdot 10^{-3}$

2. desired signal with FSK/FM or ASK modulation at TBD, CW blocking signal

FSK test circuit component list to Fig. 2

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C2	0805	NIP	±10%	loop filter capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	NIP	±5%	capacitor to match to SAW filter input
C5	0603	NIP	±5%	capacitor to match to SAW filter output
C6	0603	4.7 pf	±5%	LNA output tank capacitor
C7	0603	2.2 pf	±5%	MIX1 input matching capacitor
C8	0603	27 pF	±5%	IF1 tank capacitor
C9	0805	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1.5 pF	±5%	DEMODO phase-shift capacitor
C13	0603	680 pF	±10%	DEMODO coupling capacitor
CP	0805	10 pF	±5%	CERRES parallel capacitor
C14	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C15	0805	10 – 47 pF	±5%	demodulator output low-pass capacitor, depending on data rate
C16	0603	330 pF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
R2	0805	330 Ω	±5%	CERFIL output matching resistor
L1	0603	33 nH	±5%	inductor to match to SAW filter input
L2	0603	33 nH	±5%	inductor to match to SAW filter output
L3	0603	15 nH	±5%	LNA output tank inductor
L4	0805	100 nH	±5%	IF1 tank inductor
L5	0805	100 nH	±5%	IF1 tank inductor
XTAL	HC49 SMD	23.26429 MHz @ RF = 315 MHz 23.49444 MHz @ RF = 433.6 MHz	±25ppm calibration ±30ppm temp.	fundamental-mode crystal, C _{load} = 10 pF
SAWFIL	QCC8C	B3551 @ RF = 315 MHz B3555 @ RF = 433.6 MHz	±175 kHz B _{3dB} = 900kHz ±100 kHz B _{3dB} = 860kHz (f ₀ = 433.92MHz)	low-loss SAW filters from EPCOS
CERFIL	leaded type SMD type	SFE10.7MV @ B _{IF2} = 40 kHz SFECV10.7MJA @ B _{IF2} = 150 kHz	TBD ±40 kHz	ceramic filters from Murata
CERRES	SMD type	CDACV10.7MG18-A		ceramic demodulator tank from Murata

NIP – not in place, may be used optionally

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FM Reception

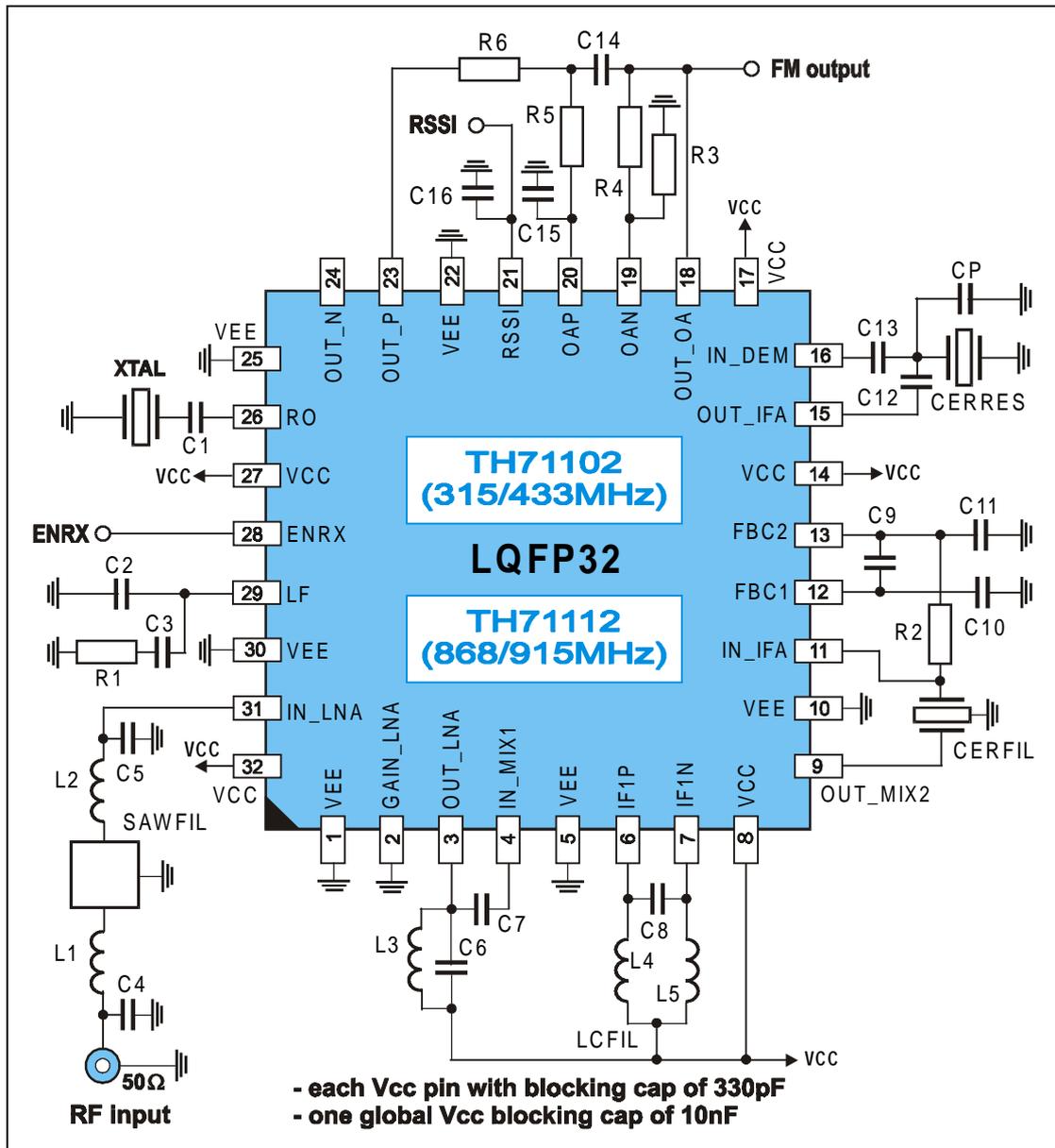


Fig. 3: Test circuit for FM reception

FM test circuit component list to Fig. 3

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C2	0805	NIP	±10%	loop filter capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	NIP	±5%	capacitor to match to SAW filter input
C5	0603	NIP	±5%	capacitor to match to SAW filter output
C6	0603	4.7 pF	±5%	LNA output tank capacitor
C7	0603	2.2 pF	±5%	MIX1 input matching capacitor
C8	0603	27 pF	±5%	IF1 tank capacitor
C9	0805	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0603	1.5 pF	±5%	DEMODO phase-shift capacitor
C13	0603	680 pF	±10%	DEMODO coupling capacitor
CP	0805	10 pF	±5%	CERRES parallel capacitor
C14	0805	100 pF	±5%	Sallen-Key low-pass filter capacitor, to set cut-off frequency
C15	0805	100 pF	±5%	Sallen-Key low-pass filter capacitor, to set cut-off frequency
C16	0603	330 pF	±10%	RSSI output low-pass capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
R2	0805	330 Ω	±5%	CERFIL output matching resistor
R3	0805	12 kΩ	±5%	Sallen-Key filter resistor, to set desired filter characteristic
R4	0805	6.8 kΩ	±5%	Sallen-Key filter resistor, to set desired filter characteristic
R5	0805	33 kΩ	±5%	Sallen-Key filter resistor, to set cut-off frequency
R6	0805	33 kΩ	±5%	Sallen-Key filter resistor, to set cut-off frequency
L1	0603	33 nH	±5%	inductor to match to SAW filter input
L2	0603	33 nH	±5%	inductor to match to SAW filter output
L3	0603	15 nH	±5%	LNA output tank inductor
L4	0603	100 nH	±5%	IF1 tank inductor
L5	0603	100 nH	±5%	IF1 tank inductor
XTAL	HC49 SMD	23.26429 MHz @ RF = 315 MHz 23.49444 MHz @ RF = 433.6 MHz	±25ppm calibration ±30ppm temp.	fundamental-mode crystal, C _{load} = 10 pF
SAWFIL	QCC8C	B3551 @ RF = 315 MHz B3555 @ RF = 433.6 MHz	±175 kHz B _{3dB} = 900kHz ±100 kHz B _{3dB} = 860kHz (f ₀ = 433.92MHz)	low-loss SAW filters from EPCOS
CERFIL	leaded type SMD type	SFE10.7MV @ B _{IF2} = 40 kHz SFECV10.7MJA @ B _{IF2} = 150 kHz	TBD ±40 kHz	ceramic filters from Murata
CERRES	SMD type	CDACV10.7MG18-A		ceramic demodulator tank from Murata

NIP – not in place, may be used optionally

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ASK Reception

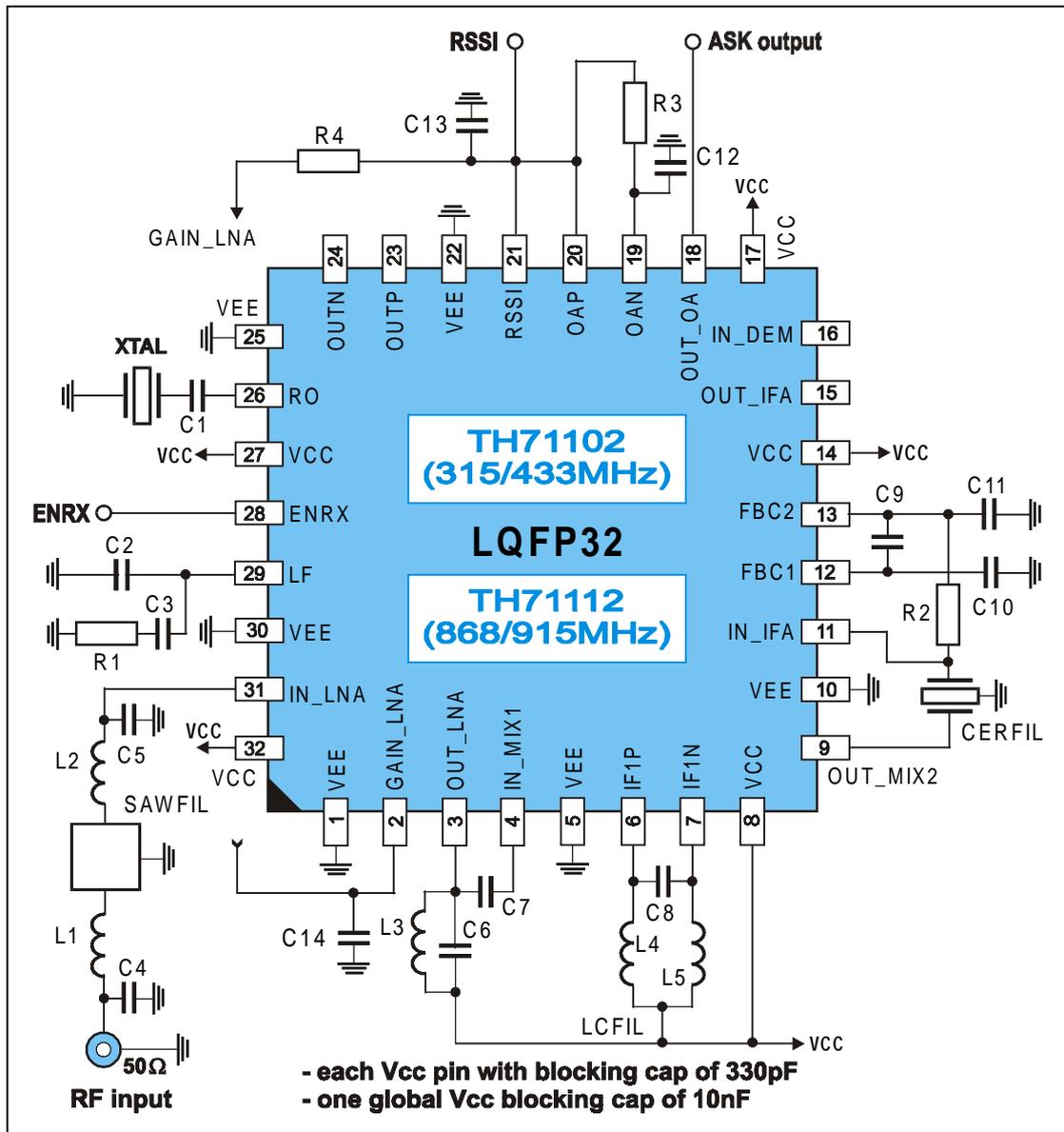


Fig. 4: Test circuit for ASK reception

ASK test circuit component list to Fig. 4

Part	Size	Value / Type	Tolerance	Description
C1	0805	15 pF	±10%	crystal series capacitor
C2	0805	NIP	±10%	loop filter capacitor
C3	0805	1 nF	±10%	loop filter capacitor
C4	0603	NIP	±5%	capacitor to match to SAW filter input
C5	0603	NIP	±5%	capacitor to match to SAW filter output
C6	0603	4.7 pF	±5%	LNA output tank capacitor
C7	0603	2.2 pF	±5%	MIX1 input matching capacitor
C8	0805	27 pF	±5%	IF1 tank capacitor
C9	0805	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0805	1 nF	±10%	ASK data slicer capacitor, depending on data rate
C13	0603	330 pF	±10%	RSSI output low-pass capacitor
C14	0603	330 pF	±10%	AGC time constant capacitor
R1	0805	10 kΩ	±10%	loop filter resistor
R2	0805	330 Ω	±5%	CERFIL output matching resistor
R3	0603	1 MΩ	±5%	ASK data slicer resistor, depending on data rate
R4	0603	15 kΩ	±5%	AGC time constant resistor
L1	0603	33 nH	±5%	inductor to match to SAW filter input
L2	0603	33 nH	±5%	inductor to match to SAW filter output
L3	0603	15 nH	±5%	LNA output tank inductor
L4	0603	100 nH	±5%	IF1 tank inductor
L5	0603	100 nH	±5%	IF1 tank inductor
XTAL	HC49-SMD	23.26429 MHz @ RF = 315 MHz 23.49444 MHz @ RF = 433.6 MHz	±25ppm calibration ±30ppm temp.	fundamental-mode crystal, C _{load} = 10 pF
SAWFIL	QCC8C	B3551 @ RF = 315 MHz B3555 @ RF = 433.6 MHz	±175 kHz B _{3dB} = 900kHz ±100 kHz B _{3dB} = 860kHz (f ₀ = 433.92MHz)	low-loss SAW filters from EPCOS
CERFIL	leaded type SMD type	SFE10.7MV @ B _{IF2} = 40 kHz SFECV10.7MJA @ B _{IF2} = 150 kHz	TBD ±40 kHz	ceramic filters from Murata

NIP – not in place, may be used optionally

Package Dimensions

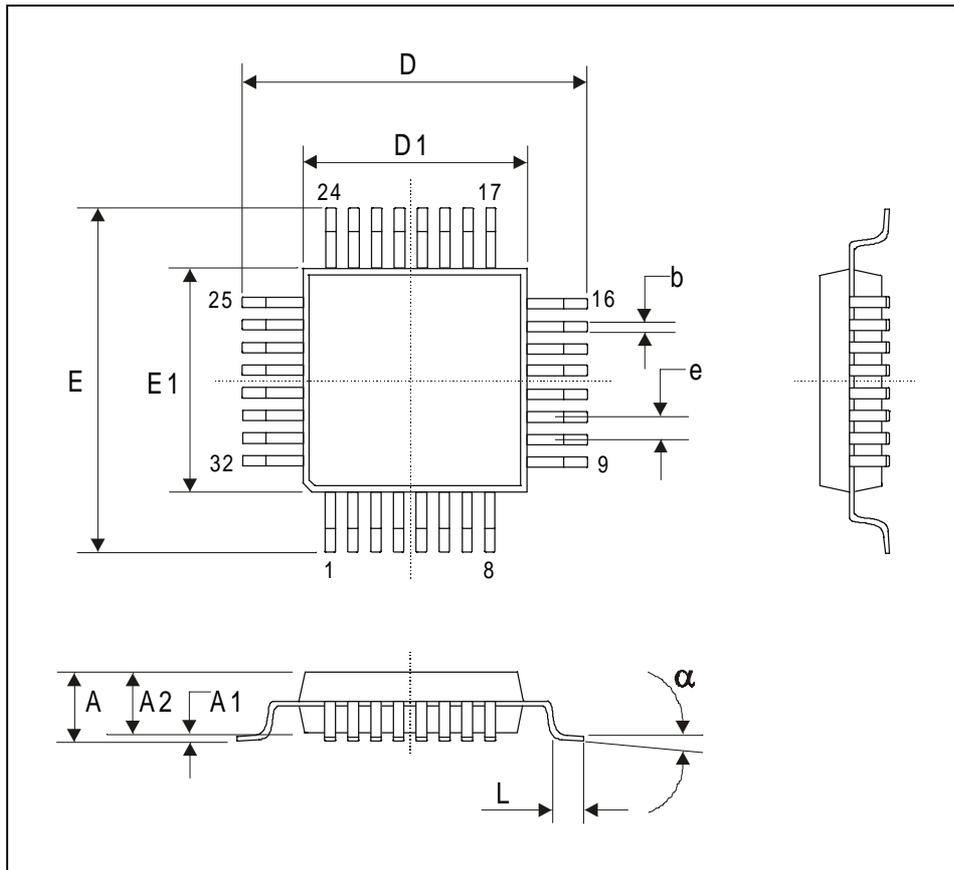


Fig. 5: LQFP32 (Low Quad Flat Package)

All Dimension in mm, coplanarity < 0.1mm									
	E1, D1	A	A1	A2	e	b	L	E, D	α
min	7.00	1.60	0.05	1.35	0.8	0.30	0.45	9.00	0°
max			0.15	1.45		0.45	0.75		7°
All Dimension in inch, coplanarity < 0.004"									
	E1, D1	A	A1	A2	e	b	L	E, D	α
min	0.276	0.630	0.002	0.053	0.031	0.012	0.018	0.354	0°
max			0.006	0.057		0.018	0.030		7°

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