



Bluetooth™ EDR Single Chip

DATA BRIEF

Features

- The lowest power consumption by design and technology (see [Table 1](#))
- World best EDR throughput (see [Table 1](#))
- World most performing BT-WLAN coexistence support for several BT/WLAN coexistence algorithms (i.e. 2/3/4-wire PTA, in a very flexible and parametrical way to optimize voice and data quality over Bluetooth and WLAN)
- Superior voice quality
 - Pitch-Period Error Concealment (PPEC) for improved speech quality (in the vicinity of interference)
- Extended range
 - Tx output power up to 8 dBm
- Pre-calibrated RF
 - Auto calibration (VCO, filters), no RF calibration required in production
- Bluetooth™V2.0 + EDR compliant
 - Full EDR support and all BT1.2 errata
 - All EDR data rates and packet types
- Backward compatibility with legacy devices through extended V1.2 feature support
 - Adaptive Frequency Hopping (AFH)
 - Faster connections through interlaced scan
 - Extended SCO (eSCO) links
- Point-to-point, point-to-multi-point (up to 7 slaves) and scatternet capability
- Asynchronous Connection-Less (ACL) logical transport link
- Synchronous Connection Oriented (SCO) link for 2 simultaneous SCO channels at 64Kbps
- Clock support for all cellular standards: system clock input and low power clock
- ARM7TDMI CPU with 32-bit core and AMBA (AHB-APB) bus configuration
- Patch RAM capability



WFBGA48 (4.5mm x 4.5 mm x 0.8 mm)

- On-chip RAM, on-chip ROM
- Communication interfaces
 - Fast UART up to 4Mbps for HCI
 - SPI interface up to 6 Mbps for HCI
 - PCM interface for voice
 - WirelessLAN coexistence with 2, 3, 4 wires
 - 19 programmable GPIOs
 - Fast master I2C interface
- Ciphering support up to 128-bit keys
- Software support up to HCI stack
 - H4 and H5 HCI transport layer
 - HCI proprietary commands and single HCI command for patch/upgrade download
- Internal power management
- Supports 1.65V to 2.85 Volts IO systems
- Seven external components: six decoupling capacitors and one single antenna interface
- Ultra low power architecture with 3 different low power modes: sleep, deep sleep and complete power down

Description

The STLC2500C is a single chip ROM-based Bluetooth solution implemented in 0.13 μ m ultra low power, ultra low leakage CMOS technology for mobile terminal applications requiring integration up to HCI level. Patch RAM is available, enabling multiple patches/upgrades. The STLC2500C offers multiple interface options. The radio has been designed specifically for single chip requirements for minimal consumption and BOM count.

Applications

- Mobile terminal platforms

Order codes

Part Number	Package	Packing
E-STLC2500C	WFBGA48	Tray
E-STLC2500CTR	WFBGA48	Tape-on-reel

Figure 1. Block diagram

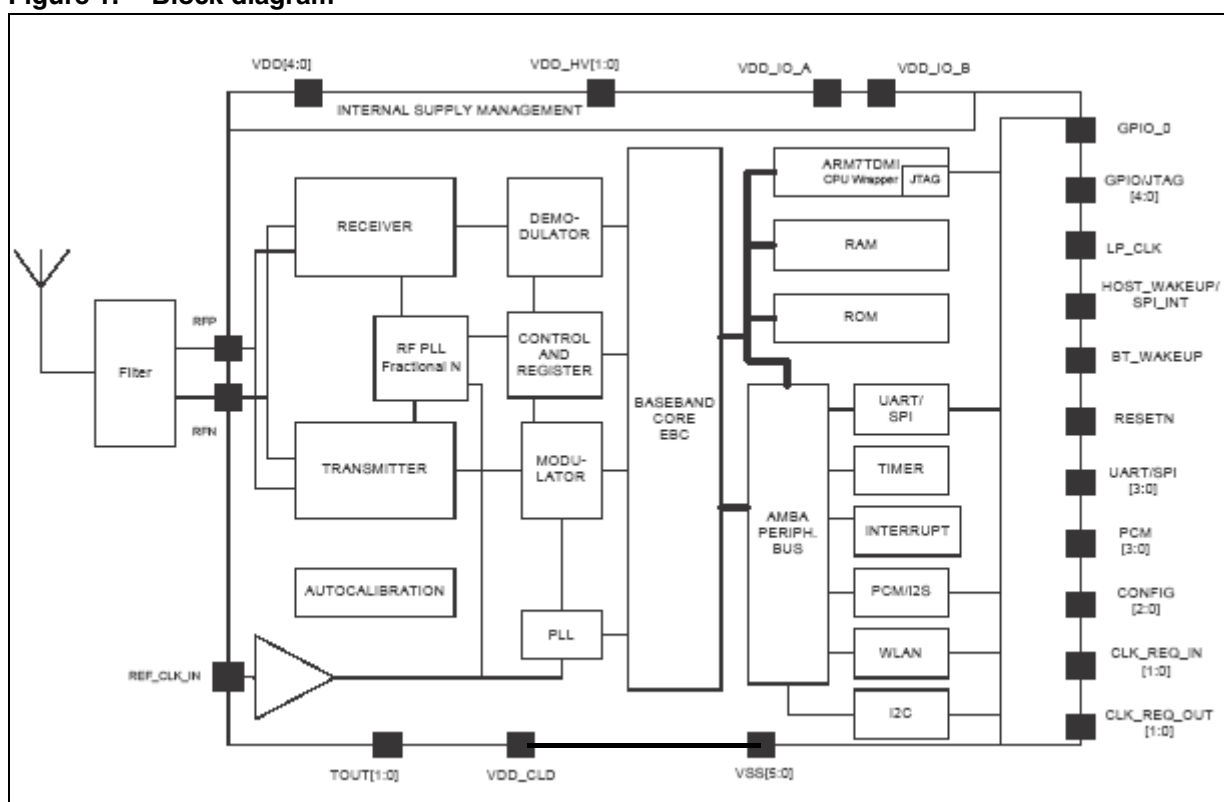


Table 1. Technical specifications

Parameter	Values
Power consumption	
Audio communication	HV3: 10.9mA, 3-EV3: 6.2mA
Data communication at maximum throughput	DH1: 22mA, 3-DH5: 35.4mA
Complete power down	1 μ A
Data rate throughput at host interface in EDR mode	2.178 Mbps

Revision history

Table 2. Document revision history

Date	Revision	Changes
29-Jan-2006	1	Initial release.

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