

Low Power Zero-Drift Operational Amplifier with Internal Capacitors

FEATURES

- Low Supply Current: 200 μ A
- No External Components Required
- Maximum Offset Voltage: 10 μ V
- Maximum Offset Voltage Drift: 0.1 μ V/ $^{\circ}$ C
- Single Supply Operation: 4.75V to 16V
- Input Common Mode Range Includes Ground
- Output Swings to Ground
- Typical Overload Recovery Time: 6ms
- Available in 8-Pin SO and PDIP Packages

APPLICATIONS

- 4mA to 20mA Current Loops
- Thermocouple Amplifiers
- Electronic Scales
- Medical Instrumentation
- Strain Gauge Amplifiers
- High Resolution Data Acquisition

DESCRIPTION

The LTC[®]1049 is a high performance, low power zero-drift operational amplifier. The two sample-and-hold capacitors usually required externally by other chopper stabilized amplifiers are integrated on the chip. Further, the LTC1049 offers superior DC and AC performance with a nominal supply current of only 200 μ A.

The LTC1049 has a typical offset voltage of 2 μ V, drift of 0.02 μ V/ $^{\circ}$ C, 0.1Hz to 10Hz input noise voltage of 3 μ V_{P-P} and typical voltage gain of 160dB. The slew rate is 0.8V/ μ s with a gain bandwidth product of 0.8MHz.

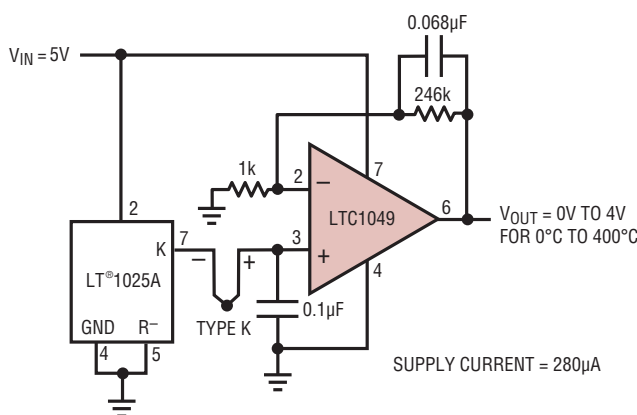
Overload recovery time from a saturation condition is 6ms, a significant improvement over chopper amplifiers using external capacitors.

The LTC1049 is available in a standard 8-pin plastic dual in line, as well as an 8-pin SO package. The LTC1049 can be a plug-in replacement for most standard op amps with improved DC performance and substantial power savings.

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TYPICAL APPLICATION

Single Supply Thermocouple Amplifier



LTC1049 • TA01

LTC1049

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (V^+ to V^-)	18V	Operating Temperature Range	-40°C to 85°C
Input Voltage (Note 2).....($V^+ + 0.3V$) to ($V^- - 0.3V$)		Storage Temperature Range	-65°C to 150°C
Output Short-Circuit Duration	Indefinite	Lead Temperature (Soldering, 10 sec).....	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW N8 PACKAGE 8-LEAD PDIP $T_{JMAX} = 110^{\circ}\text{C}$, $\theta_{JA} = 130^{\circ}\text{C/W}$ J8 PACKAGE 8-LEAD Cerdip $T_{JMAX} = 150^{\circ}\text{C}$, $\theta_{JA} = 100^{\circ}\text{C/W}$ OBSELETE PACKAGE Consider the N8 Package as an Alternate Source	ORDER PART NUMBER	TOP VIEW S8 PACKAGE 8-LEAD PLASTIC SO $T_{JMAX} = 110^{\circ}\text{C}$, $\theta_{JA} = 200^{\circ}\text{C/W}$	ORDER PART NUMBER
	LTC1049CN8		LTC1049CS8
	LTC1049CJ8		S8 PART MARKING
			1049

Order Options Tape and Reel: Add #TR
 Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
 Lead Free Part Marking: <http://www.linear.com/leadfree/>

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^{\circ}\text{C}$. $V_S = \pm 5V$, unless noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	(Note 3)		±2	±10	μV
Average Input Offset Drift	(Note 3)	●	±0.02	±0.1	μV/°C
Long Term Offset Voltage Drift			50		nV/√mo
Input Offset Current		●	±30	±100 ±150	pA pA
Input Bias Current		●	±15	±50 ±150	pA pA
Input Noise Voltage	0.1Hz to 10Hz 0.1Hz to 1Hz		3 1		μV _{P-P} μV _{P-P}
Input Noise Current	f = 10Hz (Note 4)		2		fA/√Hz
Common Mode Rejection Ratio	$V_{CM} = V^-$ to 2.7V	●	110	130	dB
Power Supply Rejection Ratio	$V_S = \pm 2.375V$ to ±8V	●	110	130	dB
Large-Signal Voltage Gain	$R_L = 100k\Omega$, $V_{OUT} = \pm 4.75V$	●	130	160	dB
Maximum Output Voltage Swing	$R_L = 10k\Omega$	●	-4.6/3.2		V V
	$R_L = 100k\Omega$	●	±4.9	±4.97	V
Slew Rate	$R_L = 10k\Omega$, $C_L = 50pF$		0.8		V/μs
Gain Bandwidth Product			0.8		MHz
Supply Current	No Load	●	200	330 495	μA μA
Internal Sampling Frequency			700		Hz

1049fb

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive latch-up. It is recommended that no sources operating from external supplies be applied prior to power-up of the LTC1049.

Note 3: These parameters are guaranteed by design. Thermocouple effects preclude measurement of these voltage levels in high speed automatic test systems. V_{OS} is measured to a limit determined by test equipment capability.

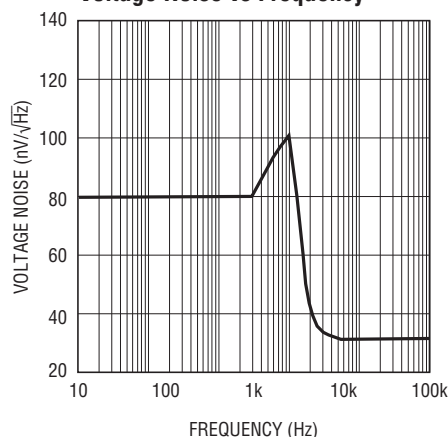
Note 4: Current Noise is calculated from the formula:

$$I_N = \sqrt{(2q \cdot I_b)}$$

where $q = 1.6 \cdot 10^{-19}$ Coulomb.

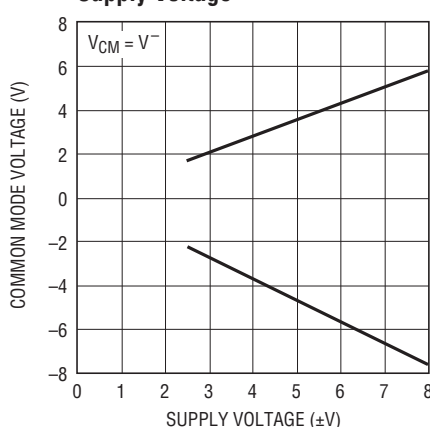
TYPICAL PERFORMANCE CHARACTERISTICS

Voltage Noise vs Frequency



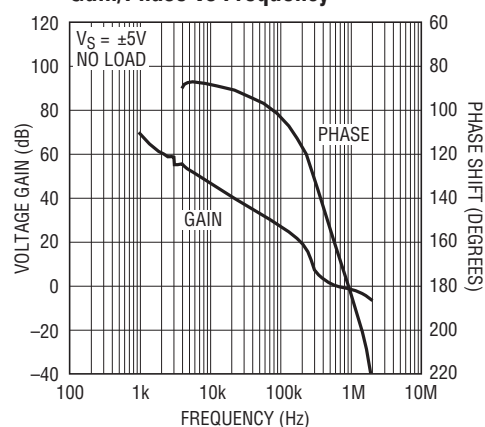
LTC1049 • TP001

Common Mode Input Range vs Supply Voltage



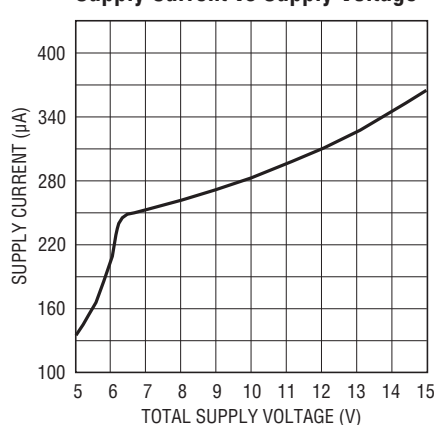
LTC1049 • TPC02

Gain/Phase vs Frequency



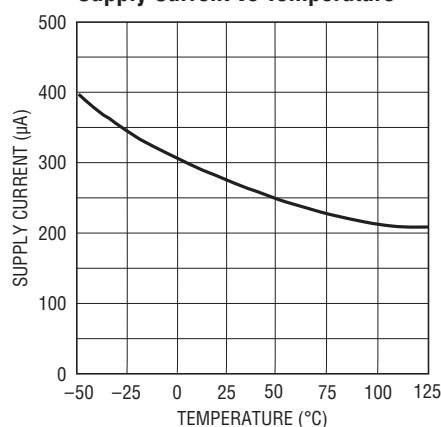
LTC1049 • TPC03

Supply Current vs Supply Voltage



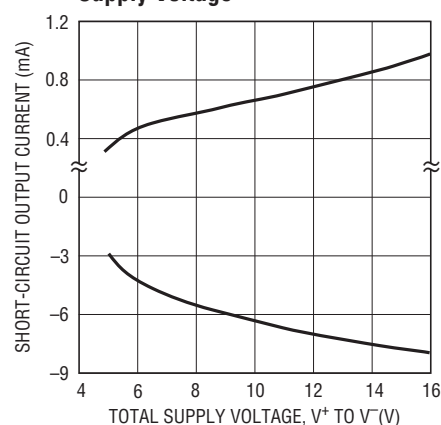
LTC1049 • TPC04

Supply Current vs Temperature



LTC1049 • TPC05

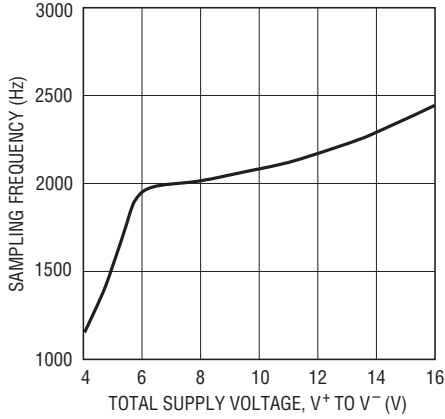
Output Short-Circuit Current vs Supply Voltage



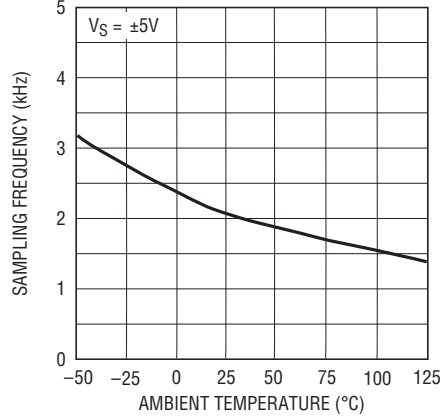
LTC1049 • TPC06

TYPICAL PERFORMANCE CHARACTERISTICS

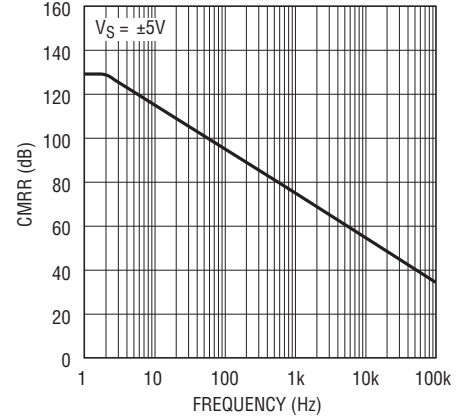
Sampling Frequency vs Supply Voltage



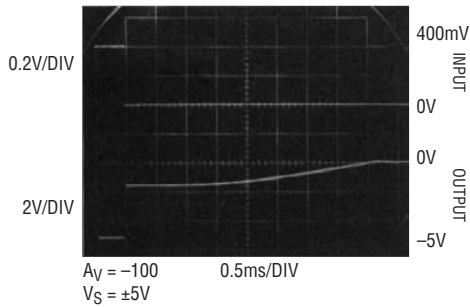
Sampling Frequency vs Temperature



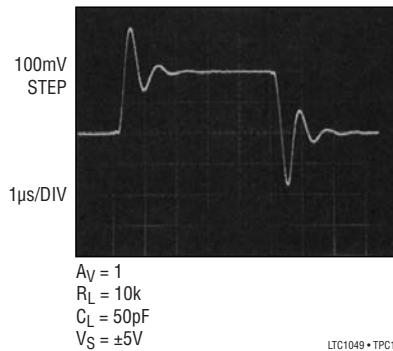
CMRR vs Frequency



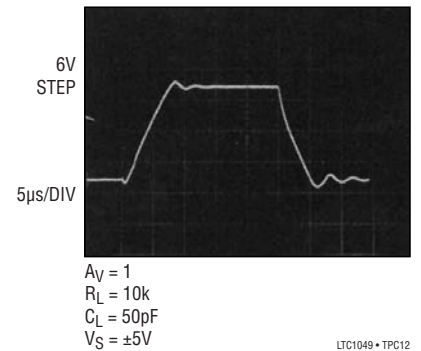
Overload Recovery



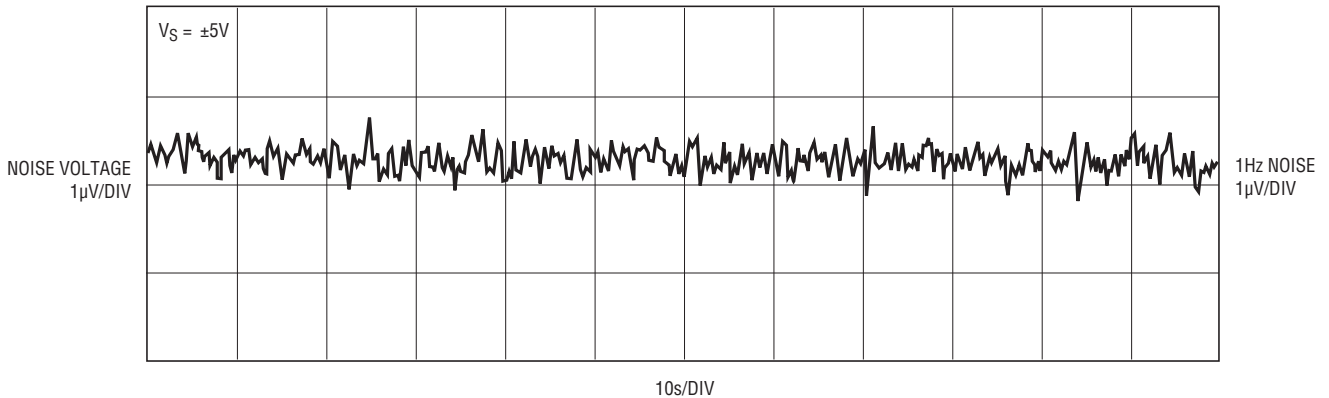
Small-Signal Transient Response



Large-Signal Transient Response

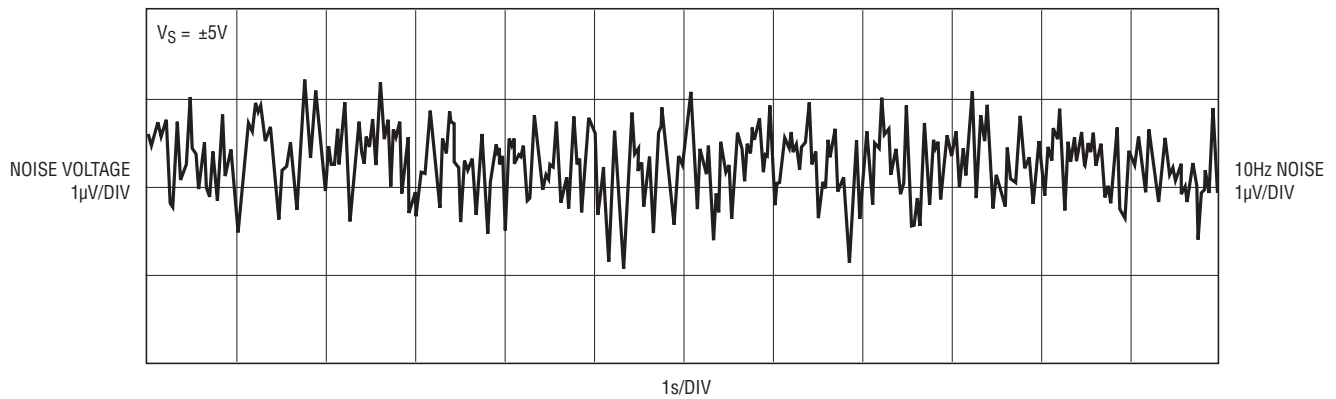


LTC1049 DC to 1Hz Noise



TYPICAL PERFORMANCE CHARACTERISTICS

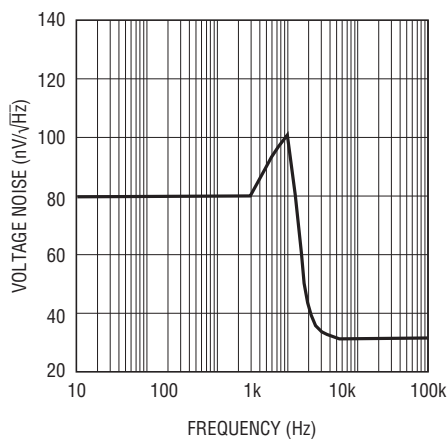
LTC1049 DC to 10Hz Noise



LTC1049•TPC14

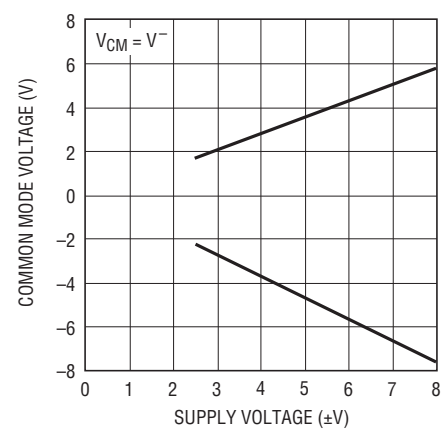
TEST CIRCUITS

Electrical Characteristics Test Circuit



LTC1049•TP01

DC to 10Hz and DC to 1Hz Noise Test Circuit



LTC1049•TPC02

APPLICATIONS INFORMATION

ACHIEVING PICOAMPERE/MICROVOLT PERFORMANCE

Picoamperes

In order to realize the picoampere level of accuracy of the LTC1049, proper care must be exercised. Leakage currents in circuitry external to the amplifier can significantly degrade performance. High quality insulation should be used (e.g., Teflon™, Kel-F); cleaning of all insulating surfaces to remove fluxes and other residues will probably be necessary—particularly for high temperature performance. Surface coating may be necessary to provide a moisture barrier in high humidity environments.

Board leakage can be minimized by encircling the input connections with a guard ring operated at a potential close to that of the inputs: in inverting configurations, the guard ring should be tied to ground; in noninverting connections, to the inverting input. Guarding both sides of the printed circuit board is required. Bulk leakage reduction depends on the guard ring width.

Microvolts

Thermocouple effects must be considered if the LTC1049's ultralow drift is to be fully utilized. Any connection of dissimilar metals forms a thermoelectric junction producing an electric potential which varies with temperature (Seebeck effect). As temperature sensors, thermocouples exploit this phenomenon to produce useful information. In low drift amplifier circuits the effect is a primary source of error.

Connectors, switches, relay contacts, sockets, resistors, solder, and even copper wire are all candidates for thermal EMF generation. Junctions of copper wire from different manufacturers can generate thermal EMFs of 200nV/°C—twice the maximum drift specification of the LTC1049. The copper/kovar junction, formed when wire or printed circuit traces contact a package lead, has a thermal EMF of approximately 35μV/°C—300 times the maximum drift specification of the LTC1049.

Minimizing thermal EMF-induced errors is possible if judicious attention is given to circuit board layout and component selection. It is good practice to minimize the number of junctions in the amplifier's input signal path. Avoid connectors, sockets, switches, and relays where possible. In instances where this is not possible, attempt to balance the number and type of junctions so that differential cancellation occurs. Doing this may involve deliberately introducing junctions to offset unavoidable junctions.

PACKAGE-INDUCED OFFSET VOLTAGE

Package-induced thermal EMF effects are another important source of errors. It arises at the copper/kovar junctions formed when wire or printed circuit traces contact a package lead. Like all the previously mentioned thermal EMF effects, it is outside the LTC1049's offset nulling loop and cannot be cancelled. The input offset voltage specification of the LTC1049 is actually set by the package-induced warm-up drift rather than by the circuit itself. The thermal time constant ranges from 0.5 to 3 minutes, depending on package type.

LOW SUPPLY OPERATION

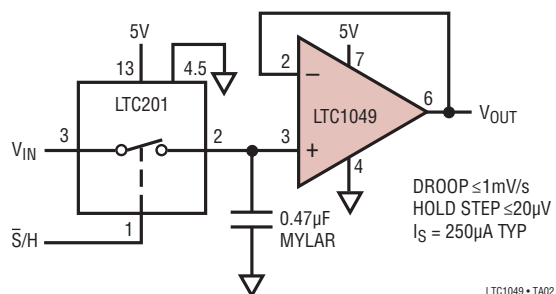
The minimum supply for proper operation of the LTC1049 is typically below 4.0V ($\pm 2.0V$). In single supply applications, PSRR is guaranteed down to 4.7V ($\pm 2.35V$) to ensure proper operation down to the minimum TTL specified voltage of 4.75V.

PIN COMPATIBILITY

The LTC1049 is pin compatible with the 8-pin versions of 7650, 7652 and other chopper-stabilized amplifiers. The 7650 and 7652 require the use of two external capacitors connected to Pins 1 and 8 which are not needed for the LTC1049. Pins 1, 5, and 8 of the LTC1049 are not connected internally; thus, the LTC1049 can be a direct plug-in for the 7650 and 7652, even if the two capacitors are left on the circuit board.

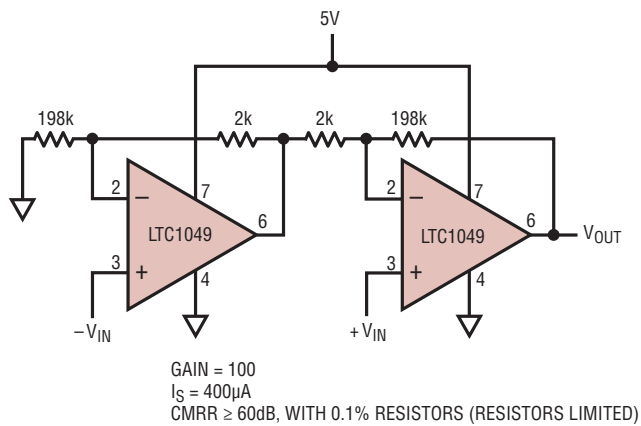
TYPICAL APPLICATIONS

Low Power, Low Hold Step Sample-and-Hold



TYPICAL APPLICATIONS

Low Power, Single Supply, Low Offset Instrumentation Amp



LTC1049 • TA03

CORNER LEADS OPTION (4 PLCS)

Top View Dimensions:

- Overall Width: $.405$ (10.287) MAX
- Pin 1 to Pin 8 Distance: $.005$ (0.127) MIN
- Pin 5 to Pin 8 Distance: $.023 - .045$ (0.584 - 1.143) HALF LEAD OPTION
- Pin 1 to Pin 4 Distance: $.025$ (0.635) RAD TYP
- Pin 1 to Pin 5 Distance: $.220 - .310$ (5.588 - 7.874)
- Pin 1 to Pin 8 Distance: $.200$ (5.080) MAX

Side View Dimensions:

- Overall Height: $.045 - .068$ (1.143 - 1.650) FULL LEAD OPTION
- Lead Angle: $0^\circ - 15^\circ$
- Lead Thickness: $.008 - .018$ (0.203 - 0.457)
- Lead Spacing: $.300$ BSC (7.62 BSC)

End View Dimensions:

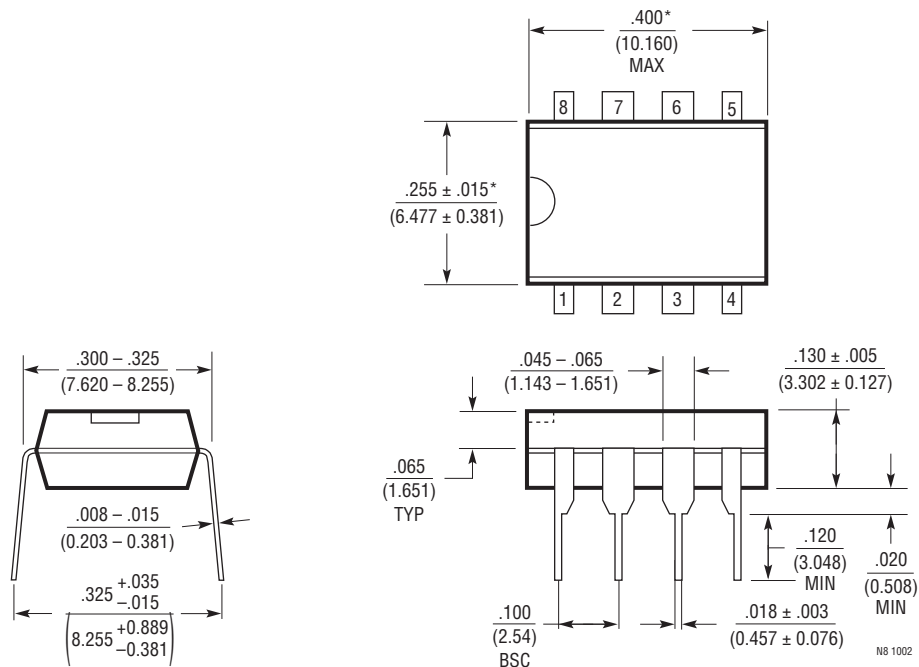
- Lead Spacing: $.015 - .060$ (0.381 - 1.524)
- Lead Thickness: $.125$ 3.175 MIN
- Lead Spacing: $.045 - .065$ (1.143 - 1.651)
- Lead Thickness: $.014 - .026$ (0.360 - 0.660)
- Lead Spacing: $.100$ (2.54) BSC

NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

OBSOLETE PACKAGE

PACKAGE DESCRIPTION

N8 Package
8-Lead PDIP (Narrow .300 Inch)
 (Reference LTC DWG # 05-08-1510)



NOTE:
 1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
 MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

PACKAGE DESCRIPTION

S8 Package 8-Lead Plastic Small Outline (Narrow .150 Inch) (Reference LTC DWG # 05-08-1610)

