Complementary Darlington Power Transistors

DPAK For Surface Mount Applications

NPN
MJD112*
PNP
MJD117*

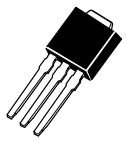
*ON Semiconductor Preferred Device

SILICON
POWER TRANSISTORS
2 AMPERES
100 VOLTS
20 WATTS

Designed for general purpose power and switching such as output or driver stages in applications such as switching regulators, converters, and power amplifiers.

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Straight Lead Version in Plastic Sleeves (“1” Suffix)
- Lead Formed Version in 16 mm Tape and Reel (“T4” Suffix)
- Surface Mount Replacements for TIP110–TIP117 Series
- Monolithic Construction With Built–in Base–Emitter Shunt Resistors
- High DC Current Gain — h_{FE} = 2500 (Typ) @ I_C = 2.0 Adc
- Complementary Pairs Simplifies Designs

CASE 369A–13

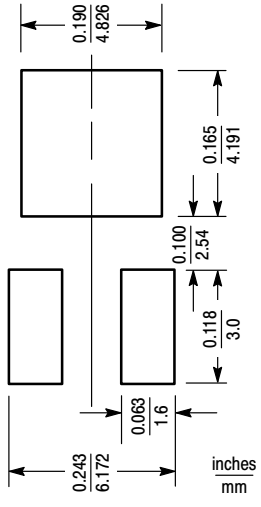


CASE 369–07

MAXIMUM RATINGS

Rating	Symbol	MJD112 MJD117	Unit
Collector–Emitter Voltage	V_{CEO}	100	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	5	Vdc
Collector Current — Continuous Peak	I_C	2 4	Adc
Base Current	I_B	50	mAdc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	20 0.16	Watts W/°C
Total Power Dissipation* @ T_A = 25°C Derate above 25°C	P_D	1.75 0.014	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +150	°C

MINIMUM PAD SIZES RECOMMENDED FOR SURFACE MOUNTED APPLICATIONS



Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	6.25	°C/W
Thermal Resistance, Junction to Ambient*	$R_{\theta JA}$	71.4	°C/W

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 30 mAdc, I_B = 0)	$V_{CEO(sus)}$	100	—	Vdc
Collector Cutoff Current (V_{CE} = 50 Vdc, I_B = 0)	I_{CEO}	—	20	μAdc
Collector Cutoff Current (V_{CB} = 100 Vdc, I_E = 0)	I_{CBO}	—	20	μAdc
Emitter Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc
Collector–Cutoff Current (V_{CB} = 80 Vdc, I_E = 0)	I_{CBO}	—	10	μAdc
Emitter–Cutoff Current (V_{BE} = 5 Vdc, I_C = 0)	I_{EBO}	—	2	mAdc
ON CHARACTERISTICS				
DC Current Gain (I_C = 0.5 Adc, V_{CE} = 3 Vdc) (I_C = 2 Adc, V_{CE} = 3 Vdc) (I_C = 4 Adc, V_{CE} = 3 Vdc)	h_{FE}	 500 1000 200	 — 12,000 —	—
Collector–Emitter Saturation Voltage (I_C = 2 Adc, I_B = 8 mAdc) (I_C = 4 Adc, I_B = 40 mAdc)	$V_{CE(sat)}$	 — —	 2 3	Vdc
Base–Emitter Saturation Voltage (I_C = 4 Adc, I_B = 40 mAdc)	$V_{BE(sat)}$	—	4	Vdc
Base–Emitter On Voltage (I_C = 2 Adc, V_{CE} = 3 Vdc)	$V_{BE(on)}$	—	2.8	Vdc
DYNAMIC CHARACTERISTICS				
Current–Gain — Bandwidth Product (I_C = 0.75 Adc, V_{CE} = 10 Vdc, f = 1 MHz)	f_T	25	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, I_E = 0, f = 0.1 MHz) MJD117 MJD112	C_{ob}	 — —	 200 100	pF

(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

*These ratings are applicable when surface mounted on the minimum pad sizes recommended.

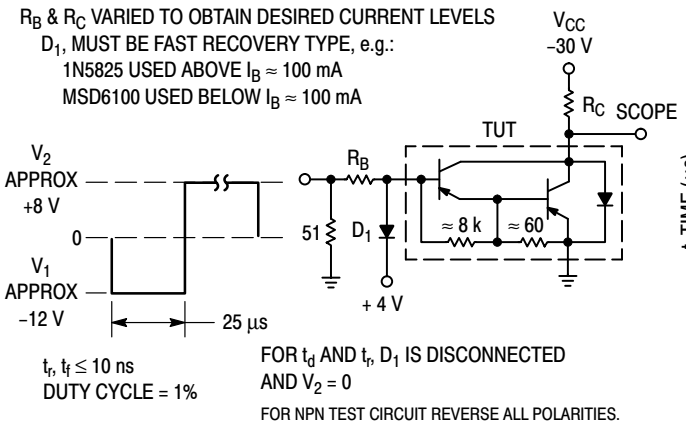


Figure 1. Switching Times Test Circuit

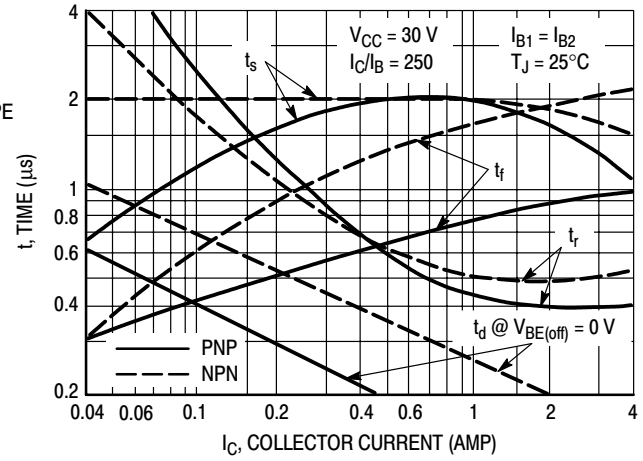


Figure 2. Switching Times

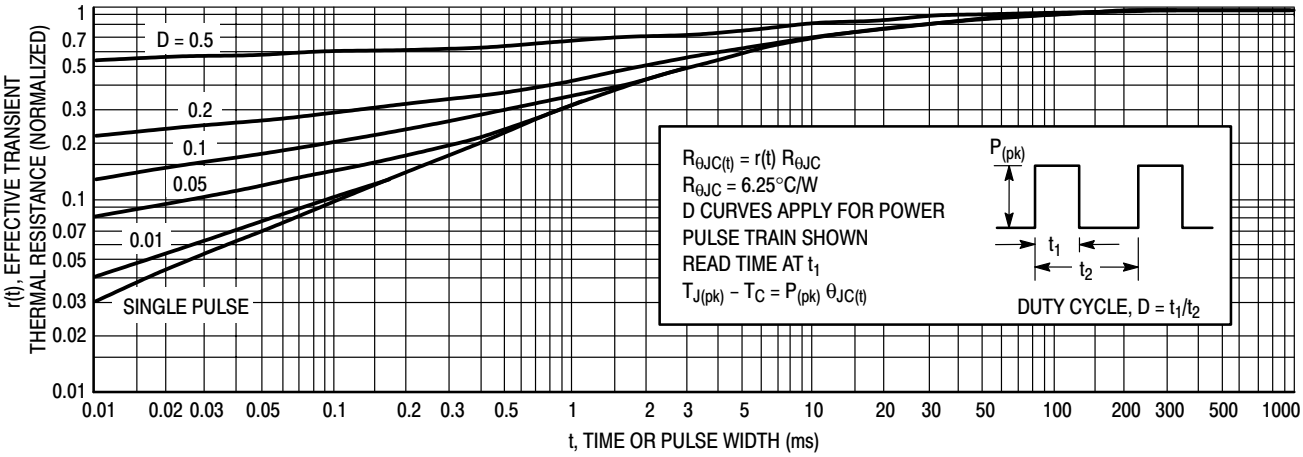


Figure 3. Thermal Response

ACTIVE–REGION SAFE–OPERATING AREA

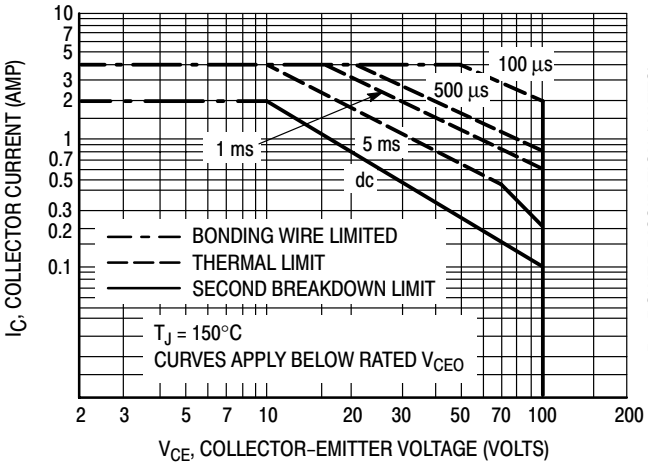


Figure 4. Maximum Rated Forward Biased Safe Operating Area

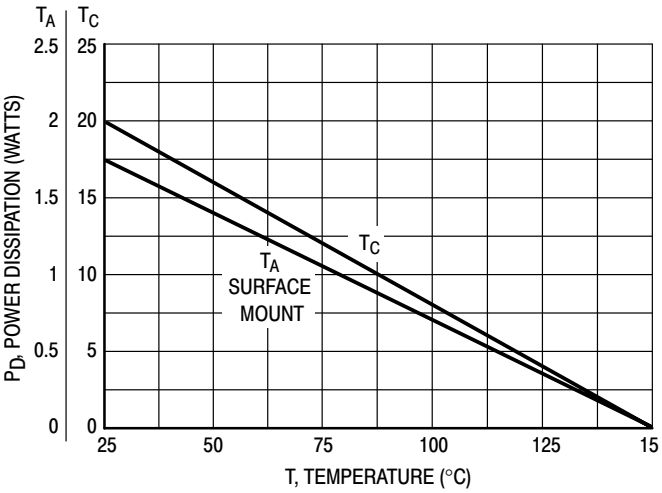


Figure 5. Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figures 5 and 6 is based on $T_{J(pk)}$ = 150°C; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)}$ < 150°C. $T_{J(pk)}$ may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

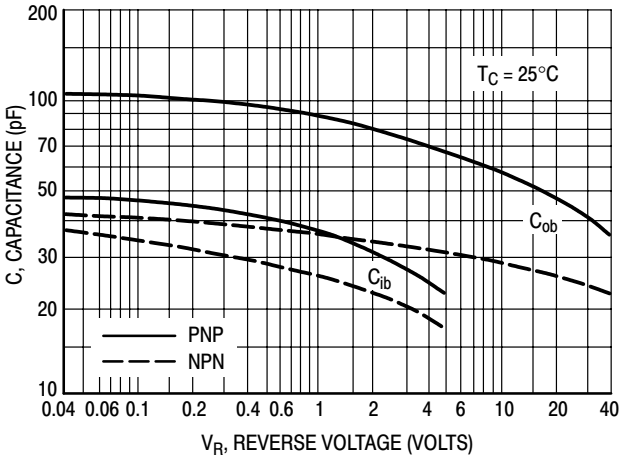


Figure 6. Capacitance

TYPICAL ELECTRICAL CHARACTERISTICS

NPN MJD112 **PNP MJD117**

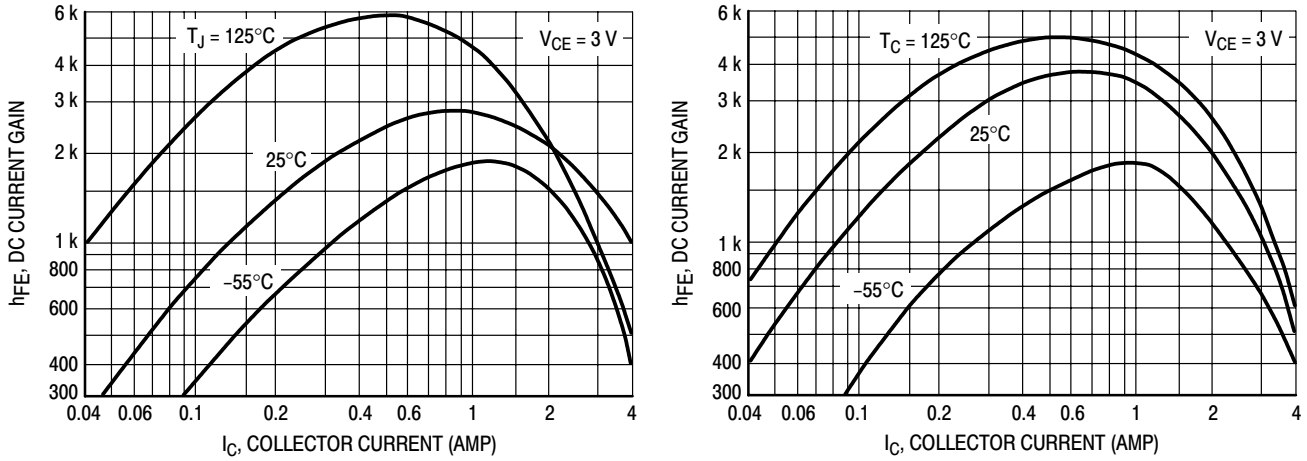


Figure 7. DC Current Gain

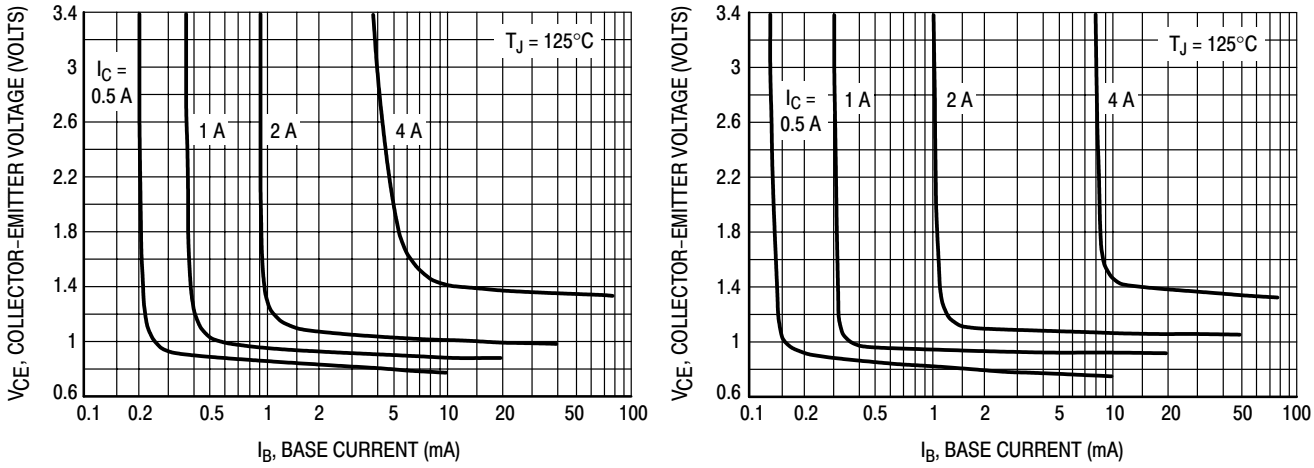


Figure 8. Collector Saturation Region

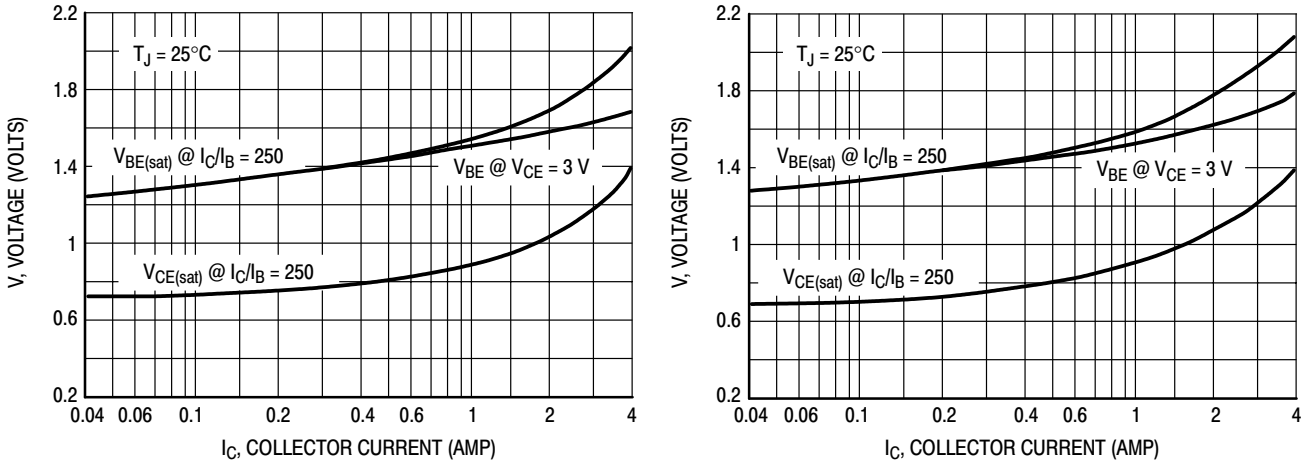


Figure 9. “On Voltages

NPN MJD112 **PNP MJD117**

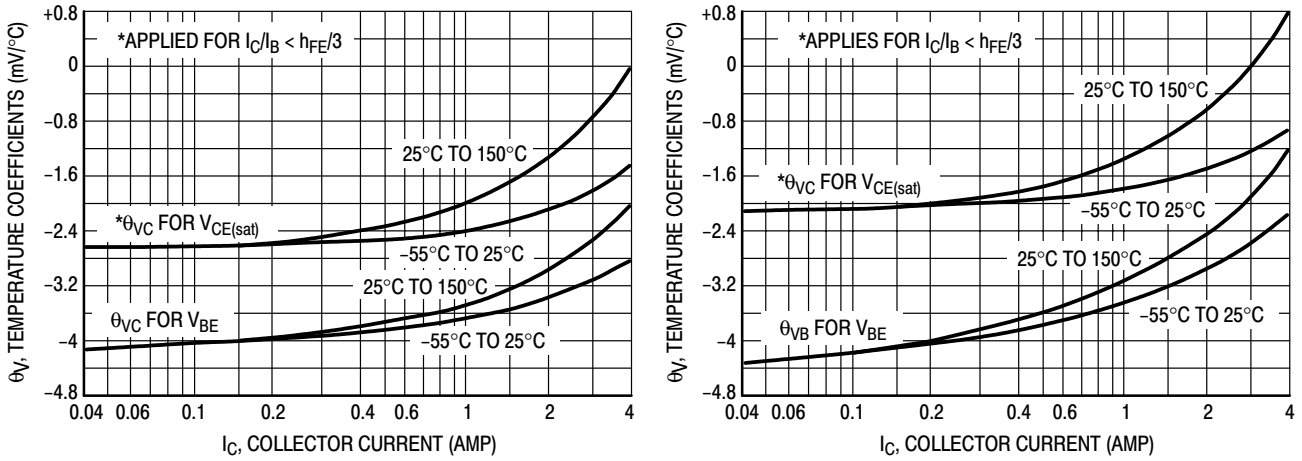


Figure 10. Temperature Coefficients

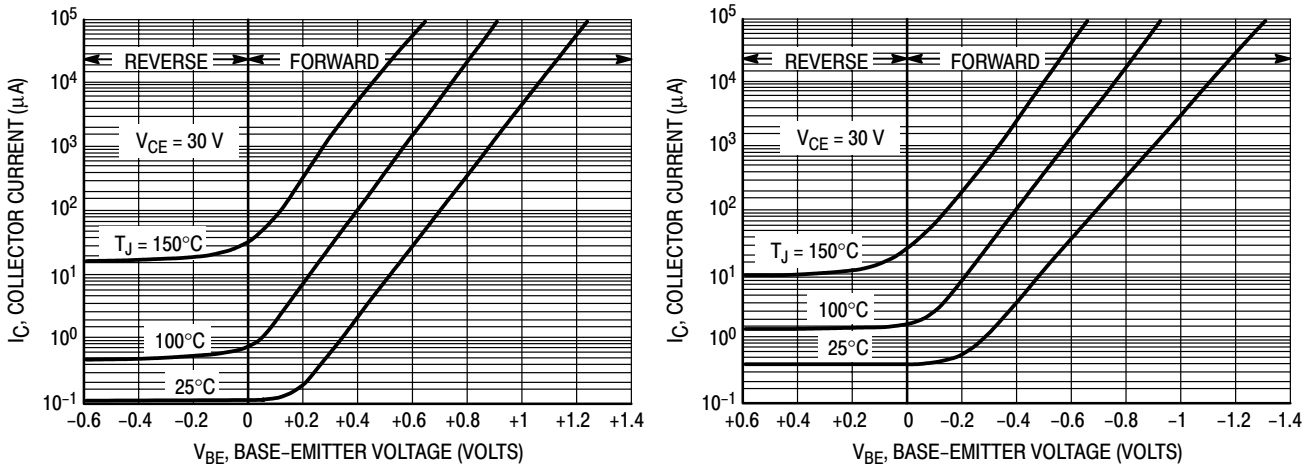


Figure 11. Collector Cut−Off Region

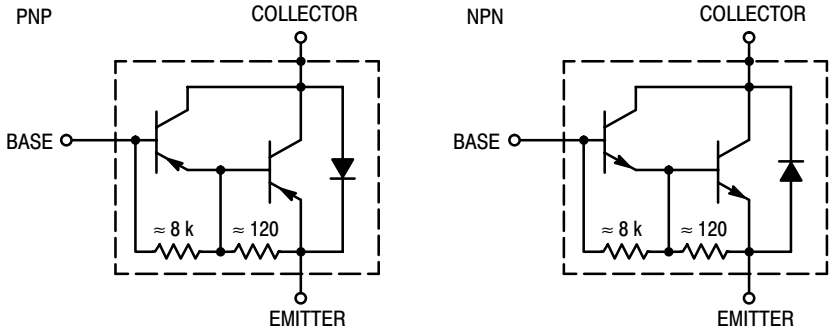
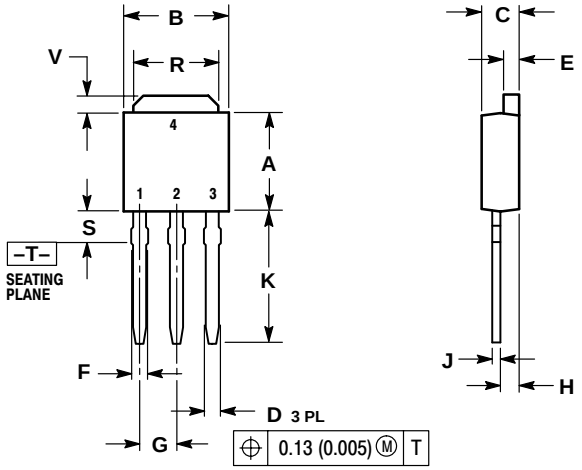


Figure 12. Darlington Schematic

PACKAGE DIMENSIONS

DPAK
CASE 369–07
ISSUE M

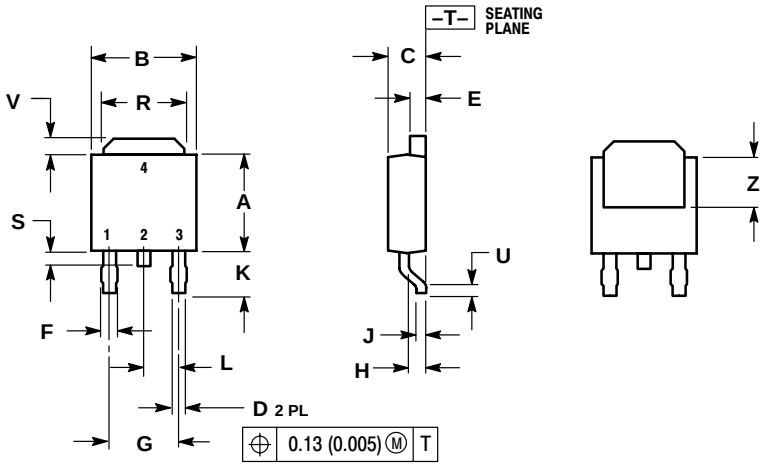


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.235	0.250	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.090 BSC		2.29 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.175	0.215	4.45	5.46
S	0.050	0.090	1.27	2.28
V	0.030	0.050	0.77	1.27

PACKAGE DIMENSIONS

DPAK
CASE 369A–13
ISSUE AA



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D	0.027	0.035	0.69	0.88
E	0.033	0.040	0.84	1.01
F	0.037	0.047	0.94	1.19
G	0.180 BSC		4.58 BSC	
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.090 BSC		2.29 BSC	
R	0.175	0.215	4.45	5.46
S	0.020	0.050	0.51	1.27
U	0.020	---	0.51	---
V	0.030	0.050	0.77	1.27
Z	0.138	---	3.51	---

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