



1M X 8 BIT HIGH SPEED CMOS SRAM

FEATURES

- Fast access time : 10ns
 - **Very low power consumption:**
 - Operating current:
80mA(TYP. 10ns)
 - Standby current (Normal version):
3mA(TYP.)
 - Single 3.3V power supply
 - All inputs and outputs TTL compatible
 - Fully static operation
 - Tri-state output
 - Data retention voltage : 1.5V (MIN.)
 - **Green package available**
- Package: 44-pin 400 mil TSOP-II
48-ball 6mmx8mm TFBGA

GENERAL DESCRIPTION

The AS7C38096A is a 8M-bit high speed CMOS static random access memory organized as 1,024K words by 8 bits. It is fabricated using very high performance, high reliability CMOS technology. Its standby current is stable within the range of operating temperature.

The AS7C38096A operates from a single power supply of 3.3V and all inputs and outputs are fully TTL compatible

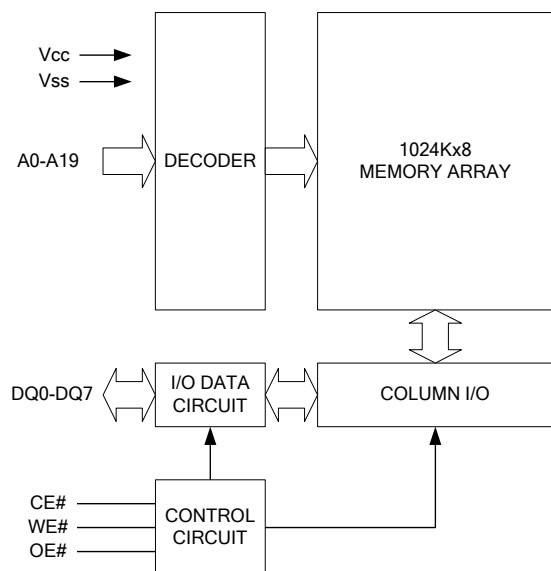
PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation	
				Standby(I_{SB1} , TYP.)	Operating(I_{CC1} , TYP.)
AS7C38096A	-40 ~ 85°C	2.7 ~ 3.6V	10ns	3mA	80/70mA



1M X 8 BIT HIGH SPEED CMOS SRAM

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

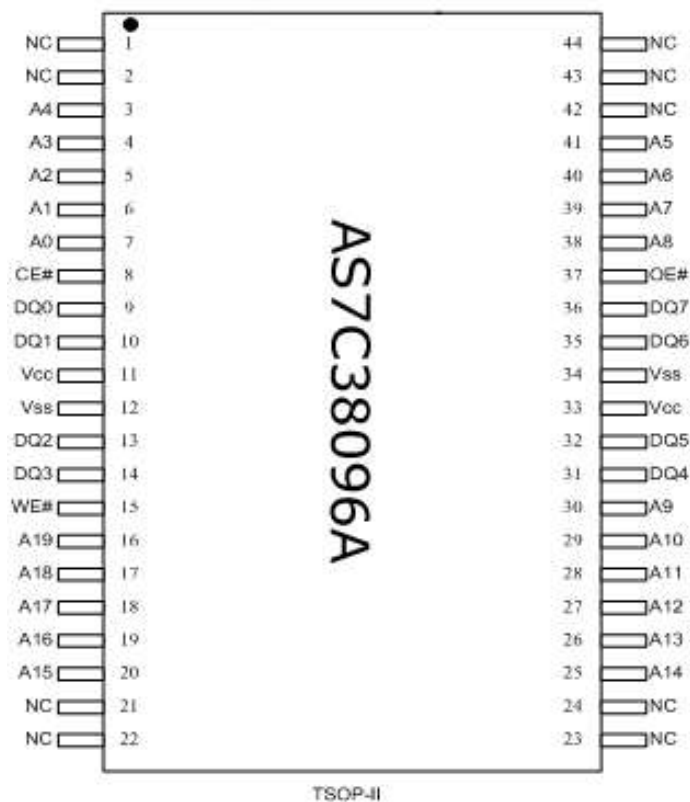
SYMBOL	DESCRIPTION
A0 - A19	Address Inputs
DQ0 - DQ7	Data Inputs/Outputs
CE#	Chip Enable Inputs
WE#	Write Enable Input
OE#	Output Enable Input
Vcc	Power Supply
Vss	Ground
NC	No Connection



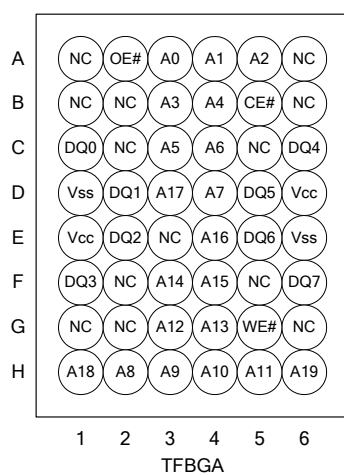
1M X 8 BIT HIGH SPEED CMOS SRAM

PIN CONFIGURATION

44-pin TSOP(Type II)



48-ball 6mmx8mm TFBGA





1M X 8 BIT HIGH SPEED CMOS SRAM

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{CC} relative to V_{SS}	V_{T1}	-0.5 to 4.6	V
Voltage on any other pin relative to V_{SS}	V_{T2}	-0.5 to $V_{CC}+0.5$	V
Operating Temperature	T_A	-40 to 85	°C
Storage Temperature	T_{STG}	-65 to 150	°C

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to the absolute maximum rating conditions for extended period may affect device reliability.

TRUTH TABLE

MODE	CE#	OE#	WE#	I/O OPERATION	SUPPLY CURRENT
Standby	H	X	X	High-Z	I_{SB1}
Output Disable	L	H	H	High-Z	I_{CC}
Read	L	L	H	D _{OUT}	I_{CC}
Write	L	X	L	D _{IN}	I_{CC}

Note: H = V_{IH} , L = V_{IL} , X = Don't care.

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP. ^{*4}	MAX.	UNIT
Supply Voltage	V _{CC}		-10	2.7	3.3	3.6	V
Input High Voltage	V _{IH} ^{*1}			2.2	-	V _{CC} +0.3	V
Input Low Voltage	V _{IL} ^{*2}			- 0.3	-	0.8	V
Input Leakage Current	I _{LI}	V _{CC} ≥ V _{IN} ≥ V _{SS}		- 1	-	1	μA
Output Leakage Current	I _{LO}	V _{CC} ≥ V _{OUT} ≥ V _{SS} , Output Disabled		- 1	-	1	μA
Output High Voltage	V _{OH}	I _{OH} = -8mA		2.4	-	-	V
Output Low Voltage	V _{OL}	I _{OL} =4mA		-	-	0.4	V
Average Operating Power supply Current	I _{CC}	CE# = V _{IL} , I _{I/O} = 0mA ;f=max	-10	-	100	130	mA
	I _{CC1}	CE# ≥V _{CC} - 0.2V, Other pin is at 0.2V or V _{CC} -0.2V I _{I/O} = 0mA;f=max	-10		80	110	mA
Standby Power Supply Current	I _{sb}	CE# ≥V _{Ih} Other pin is at V _{il} or V _{Ih}				40	mA
Standby Power Supply Current	I _{SB1}	CE# ≥V _{CC} - 0.2V; Other pin is at 0.2V or V _{CC} -0.2V			3	25	mA

Notes:

- $V_{IH}(\max) = V_{CC} + 3.0V$ for pulse width less than 10ns.
- $V_{IL}(\min) = V_{SS} - 3.0V$ for pulse width less than 10ns.
- Over/Undershoot specifications are characterized, not 100% tested.



1M X 8 BIT HIGH SPEED CMOS SRAM

4. Typical values are included for reference only and are not guaranteed or tested.

Typical values are measured at $V_{CC} = V_{CC}(TYP.)$ and $T_A = 25^\circ\text{C}$

CAPACITANCE ($T_A = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

PARAMETER	SYMBOL	MIN.	MAX	UNIT
Input Capacitance	C_{IN}	-	8	pF
Input/Output Capacitance	$C_{I/O}$	-	10	pF

Note : These parameters are guaranteed by device characterization, but not production tested.

AC TEST CONDITIONS

speed	10ns
Input Pulse Levels	0.2V to $V_{CC}-0.2\text{V}$
Input Rise and Fall Times	3ns
Input and Output Timing Reference Levels	1.5V
Output Load	$C_L = 30\text{pF} + 1\text{TTL}$, $I_{OH}/I_{OL} = -4\text{mA}/8\text{mA}$

AC ELECTRICAL CHARACTERISTICS

(1) READ CYCLE

PARAMETER	SYM.	AS7C38096A-10		UNIT
		MIN.	MAX.	
Read Cycle Time	t_{RC}	10	-	ns
Address Access Time	t_{AA}	-	10	ns
Chip Enable Access Time	t_{ACE}	-	10	ns
Output Enable Access Time	t_{OE}	-	4.5	ns
Chip Enable to Output in Low-Z	t_{CLZ}^*	2	-	ns
Output Enable to Output in Low-Z	t_{OLZ}^*	0	-	ns
Chip Disable to Output in High-Z	t_{CHZ}^*	-	4	ns
Output Disable to Output in High-Z	t_{OHZ}^*	-	4	ns
Output Hold from Address Change	t_{OH}	2	-	ns

(2) WRITE CYCLE

PARAMETER	SYM.	AS7C38096A-10		UNIT
		MIN.	MAX.	
Write Cycle Time	t_{WC}	10	-	ns
Address Valid to End of Write	t_{AW}	8	-	ns
Chip Enable to End of Write	t_{CW}	8	-	ns
Address Set-up Time	t_{AS}	0	-	ns
Write Pulse Width	t_{WP}	8	-	ns
Write Recovery Time	t_{WR}	0	-	ns
Data to Write Time Overlap	t_{DW}	6	-	ns
Data Hold from End of Write Time	t_{DH}	0	-	ns
Output Active from End of Write	t_{OW}^*	2	-	ns
Write to Output in High-Z	t_{WHZ}^*	-	4	ns

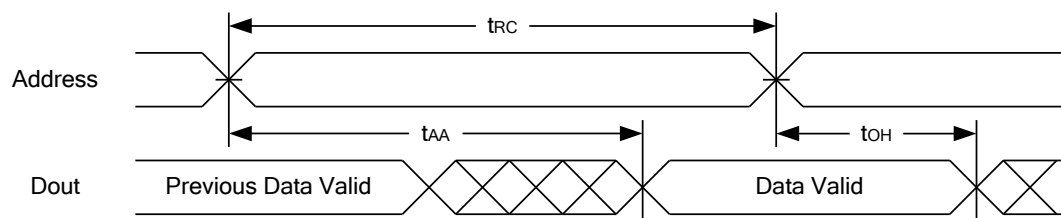
*These parameters are guaranteed by device characterization, but not production tested.



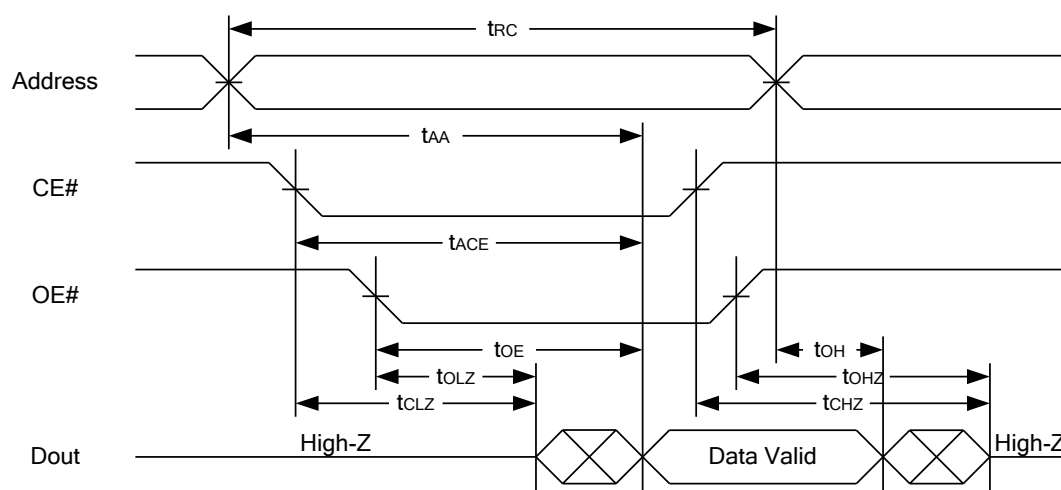
1M X 8 BIT HIGH SPEED CMOS SRAM

TIMING WAVEFORMS

READ CYCLE 1 (Address Controlled) (1,2)



READ CYCLE 2 (CE# and OE# Controlled) (1,3,4,5)



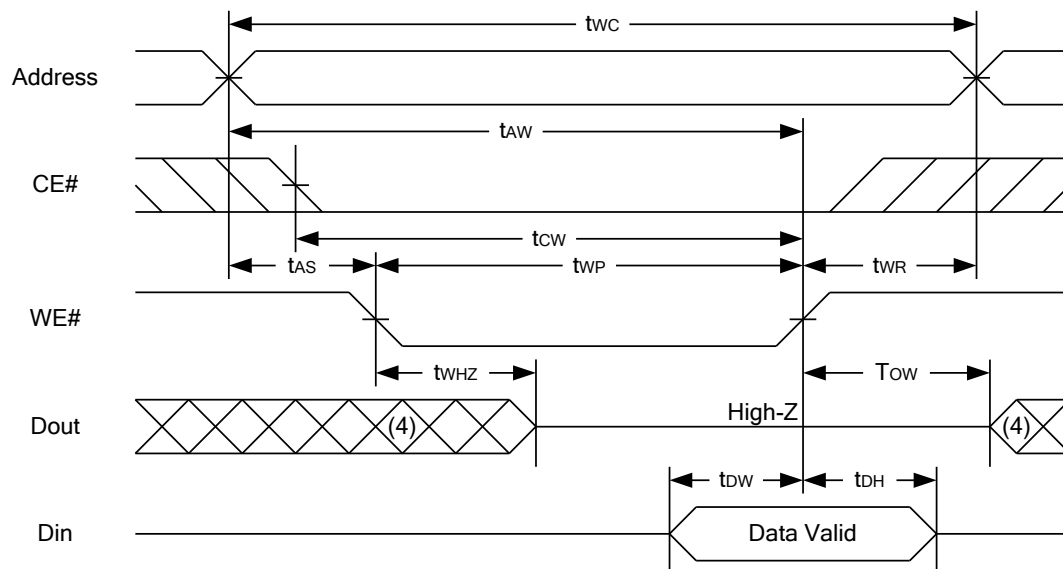
Notes :

1. WE# is high for read cycle.
2. Device is continuously selected OE# = low, CE# = low.
3. Address must be valid prior to or coincident with CE# = low; otherwise tAA is the limiting parameter.
4. tCLZ, tOLZ, tCHZ and tOHZ are specified with CL = 5pF. Transition is measured $\pm 500\text{mV}$ from steady state.
5. At any given temperature and voltage condition, tCHZ is less than tCLZ, tOHZ is less than tOLZ.

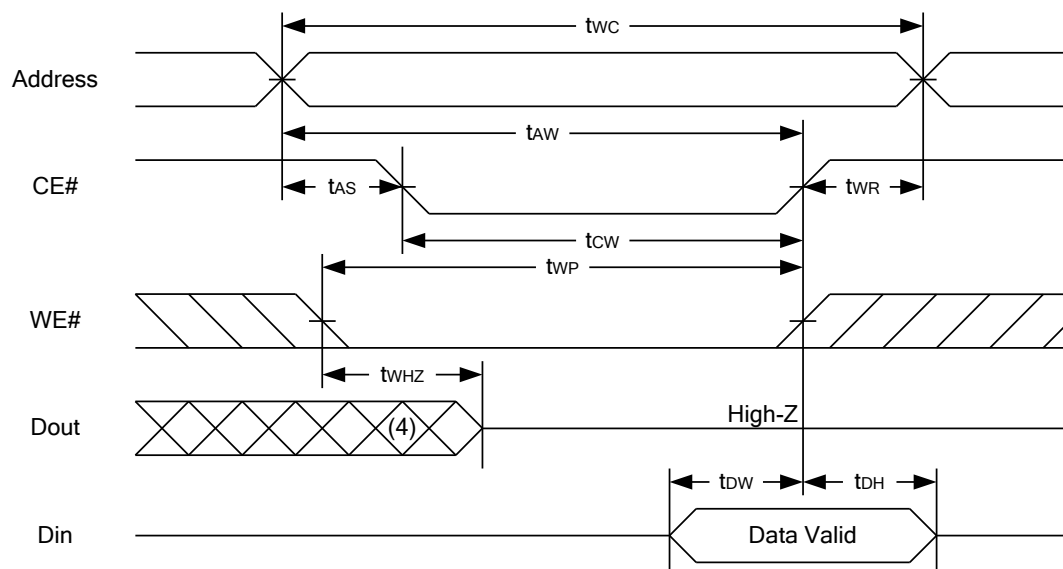


1M X 8 BIT HIGH SPEED CMOS SRAM

WRITE CYCLE 1 (WE# Controlled) (1,2,3,5,6)



WRITE CYCLE 2 (CE# Controlled) (1,2,5,6)



Notes :

1. WE#, CE# must be high during all address transitions.
2. A write occurs during the overlap of a low CE#, low WE#.
3. During a WE# controlled write cycle with OE# low, t_{WP} must be greater than $t_{WHZ} + t_{DW}$ to allow the drivers to turn off and data to be placed on the bus.
4. During this period, I/O pins are in the output state, and input signals must not be applied.
5. If the CE# low transition occurs simultaneously with or after WE# low transition, the outputs remain in a high impedance state.
6. t_{OW} and t_{WHZ} are specified with $C_L = 5\text{pF}$. Transition is measured $\pm 500\text{mV}$ from steady state.



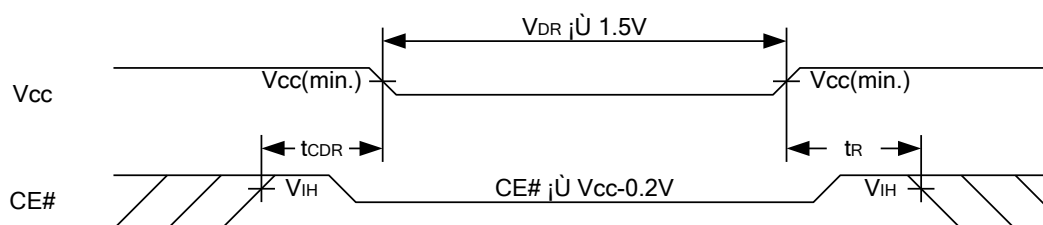
1M X 8 BIT HIGH SPEED CMOS SRAM

DATA RETENTION CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V _{CC} for Data Retention	V _{DR}	CE# $\geq$ V _{CC} - 0.2V	1.5	-	3.6	V
Data Retention Current	I _{DR}	V _{CC} = 1.5V CE# $\geq$ V _{CC} - 0.2V; Other pin is at 0.2V or V _{CC} -0.2V	-	3	25	mA
Chip Disable to Data Retention Time	t _{CDR}	See Data Retention Waveforms (below)	0	-	-	ns
Recovery Time	t _R		t _{RC*}	-	-	ns

t_{RC*} = Read Cycle Time

DATA RETENTION WAVEFORM

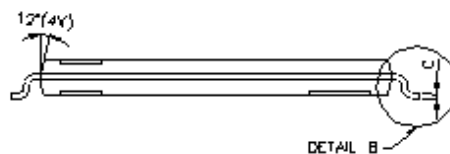
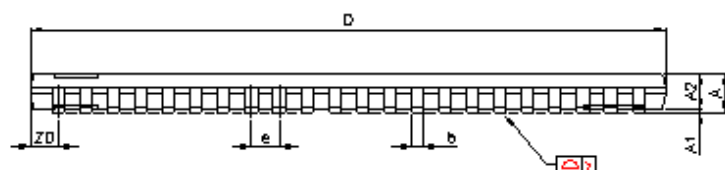
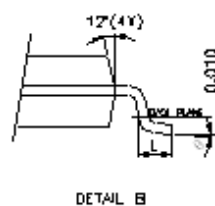
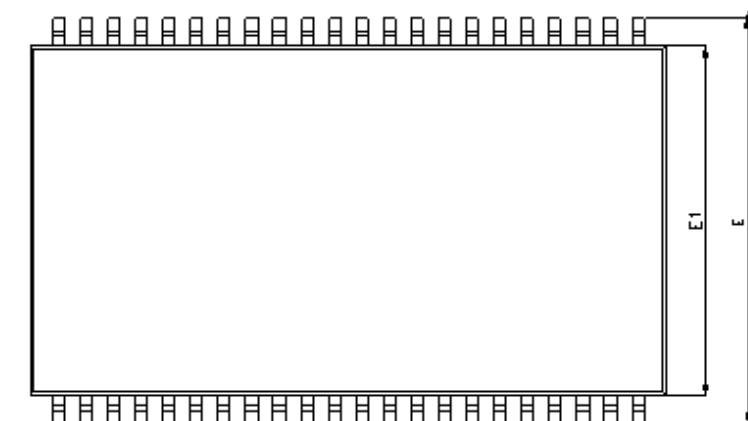




1M X 8 BIT HIGH SPEED CMOS SRAM

PACKAGE OUTLINE DIMENSION

44-pin 400mil TSOP-II Package Outline Dimension

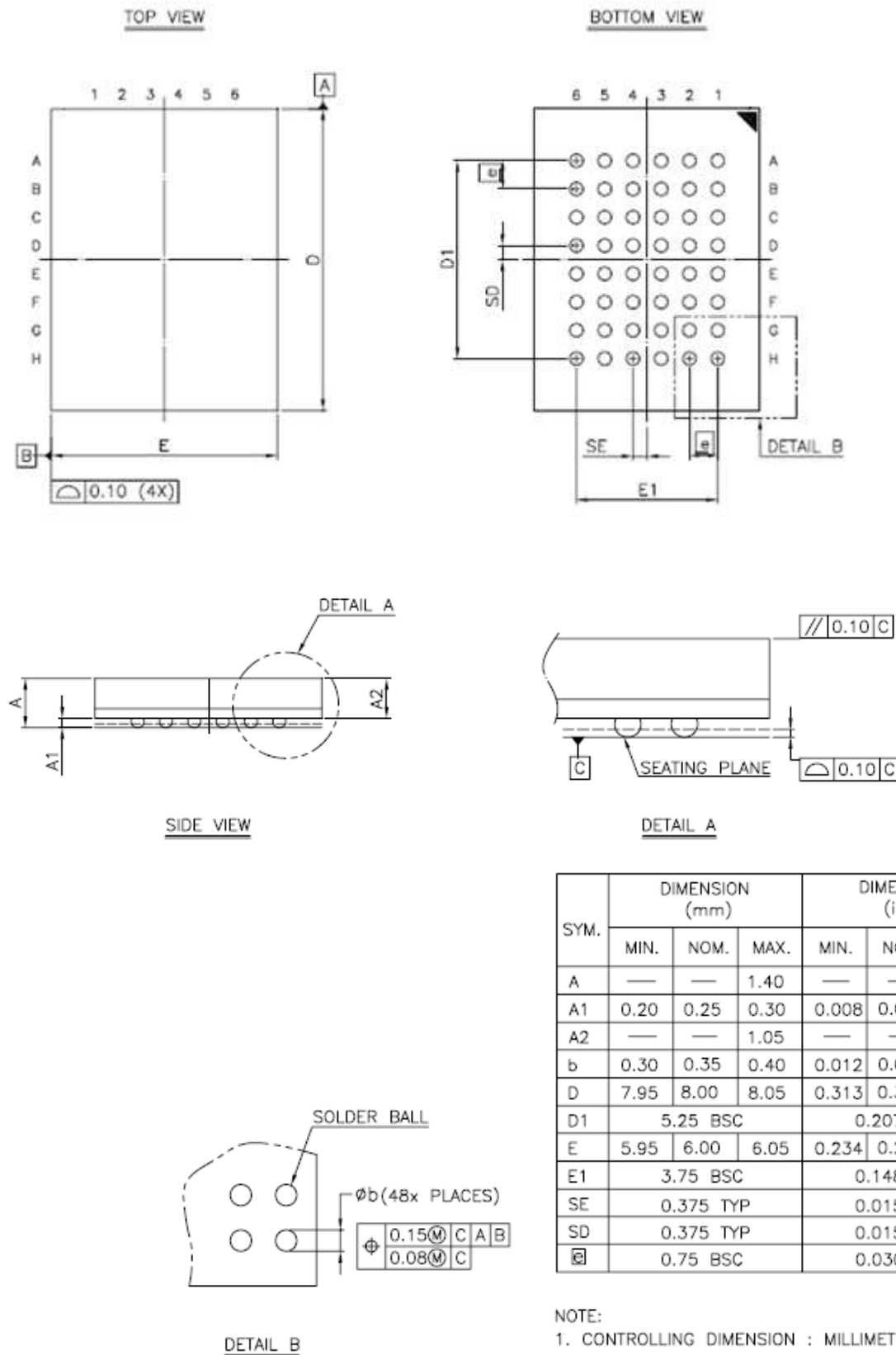


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN MILS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	47.2
A1	0.05	0.10	0.15	2.0	3.9	5.9
A2	0.95	1.00	1.05	37.4	39.4	41.3
b	0.30	-	0.45	11.8	-	17.7
c	0.12	-	0.21	4.7	-	8.3
D	18.212	18.415	18.618	717	725	733
E	11.506	11.760	12.014	453	463	473
E1	9.957	10.160	10.363	392	400	408
e	-	0.800	-	-	31.5	-
L	0.40	0.50	0.60	15.7	19.7	23.6
ZD	-	0.805	-	-	31.7	-
y	-	-	0.076	-	-	3
θ	0°	3°	6°	0°	3°	6°



1M X 8 BIT HIGH SPEED CMOS SRAM

48-ball 6mm × 8mm TFBGA Package Outline Dimension

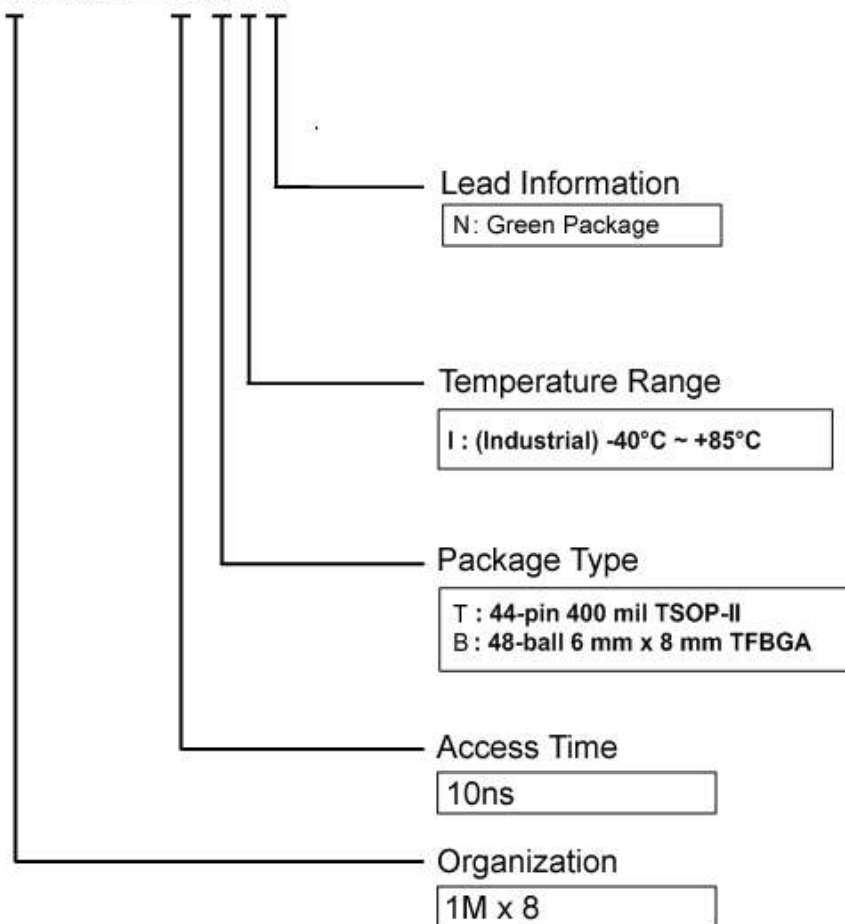




1M X 8 BIT HIGH SPEED CMOS SRAM

ORDERING INFORMATION

AS7C38096A - 10 x I N



BGA : 48-ball 6 mm x 8 mm TFBGA	Industrial -40°C ~ +85°C	AS7C38096A-10BIN
TSOP II : 44-pin 400 mil TSOP II	Industrial -40°C ~ +85°C	AS7C38096A-10TIN

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

Alliance Memory:

[AS7C38096A-10BIN](#) [AS7C38096A-10BINTR](#) [AS7C38096A-10TIN](#) [AS7C38096A-10TINTR](#)