

Evaluation Board EPC90120 Quick Start Guide

60 V Half-Bridge with Gate Drive using EPC2152

Revised September 24, 2025

Version 4.0



DESCRIPTION

The EPC90120 evaluation board is a 60 V maximum device voltage, 11 A maximum output current, half bridge featuring the EPC2152 Integrated ePower™ Stage. The purpose of this evaluation board is to simplify the evaluation process of the EPC2152 by including all the critical components on a single board that can be easily connected into the majority of existing converter topologies.

The EPC90120 evaluation board measures 2" x 2" and contains one EPC2152 Integrated ePower™ Stage. The board also contains all critical components and the layout supports optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A block diagram of the circuit is given in figure 1.

For more information on the EPC2152 please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary ($T_A = 25^\circ\text{C}$) EPC90120

Symbol	Parameter	Conditions	Min	Nominal	Max	Units
V_{DD}	Gate Drive Input Supply Range		11	12	13	V
V_{IN}	Bus Input Voltage Range				60 ⁽¹⁾	
I_{OUT}	Switch Node Output Current	At 750 kHz, no heatsink, 400 LFM			11 ⁽²⁾	A
V_{PWM}	PWM Logic Input Voltage Threshold ⁽³⁾	Input 'High' Input 'Low'	3.5 0		5.5 1.5	V
	Minimum 'High' State Input Pulse Width	V_{PWM} rise and fall time < 10ns	50			ns
	Minimum 'Low' State Input Pulse Width ⁽⁴⁾	V_{PWM} rise and fall time < 10ns	200			

(1) Maximum input voltage depends on inductive loading, maximum switch node ringing must be kept under 60 V for EPC2152.

(2) Maximum current depends on die temperature – actual maximum current is affected by switching frequency, bus voltage and thermal cooling.

(3) When using the on board logic buffers, refer to the EPC2152 datasheet when bypassing the logic buffers.

(4) Limited by time needed to 'refresh' high side bootstrap supply voltage.



Front view

Back view

EPC90120 evaluation board

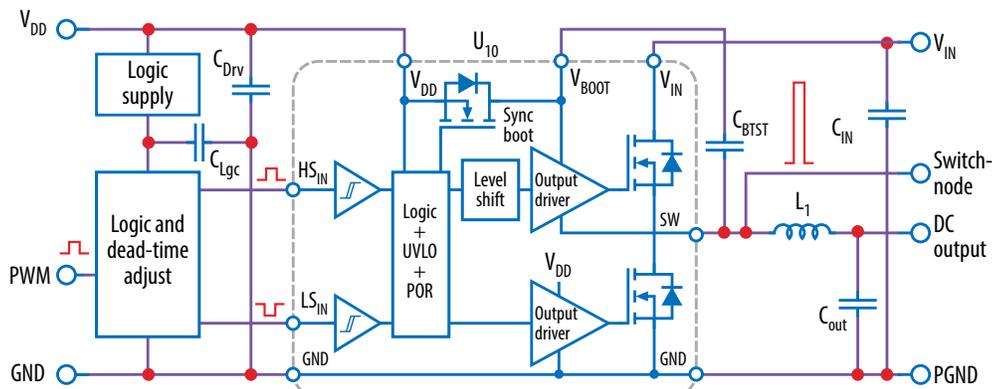


Figure 1: Block diagram of EPC90120 evaluation board

In **no-bypass mode**, figure 5(a) (red jumper across pins 5 & 6 of J640), both the on-board polarity and dead-time circuits are fully utilized. In **dead-time bypass mode**, figure 5(b) (red jumpers across pins 3 & 4 of J640), only the on-board polarity changer circuit is utilized, effectively bypassing the dead-time circuit. In **full bypass mode**, Figure 5(c) (red jumper across pins 1 & 2 of J640), the inputs to the gate driver are directly connected to the PWM1 and PWM2 pins and the on-board polarity and dead-time circuits are not utilized.

Buck converter configuration

To operate the board as a buck converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select **Single Input Buck Mode**, the bypass jumper J640 **must** be set to the **no-bypass mode**, the **buck mode** J630 **must** be selected as shown in figure 6(a).

To select **Dual Input Buck Mode**, the bypass jumper J640 **may** be configured to any of the valid settings, the dual-input mode J630 **must** be selected as shown in figure 6(b).

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass configurations have been chosen and set, then the boards can be operated.

1. With power off, connect the input power supply bus to VIN and ground / return to GND.
2. With power off, connect the switch node (SW) of the half bridge to your circuit as required (half bridge configuration). Or use the provided pads for inductor (L1) and output capacitors (Cout), as shown in figure 6.
3. With power off, connect the gate drive supply to VDD (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J2 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is set between 7.5 V and 12 V.
6. Turn on the controller / PWM input source.
7. Making sure the initial input supply voltage is 0 V, turn on the power and slowly increase the voltage to the required value (**do not exceed the absolute maximum voltage**). Probe switch-node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters.
9. For shutdown, please follow steps in reverse.

Bypass mode warnings

- **It is important to provide the correct PWM signals that includes dead-time and polarity for either buck or boost operation when making use of bypass modes.**
- When operating in **full bypass mode**, the input signal specifications revert to that of the EPC2152. Refer to the **EPC2152 datasheet** for details.

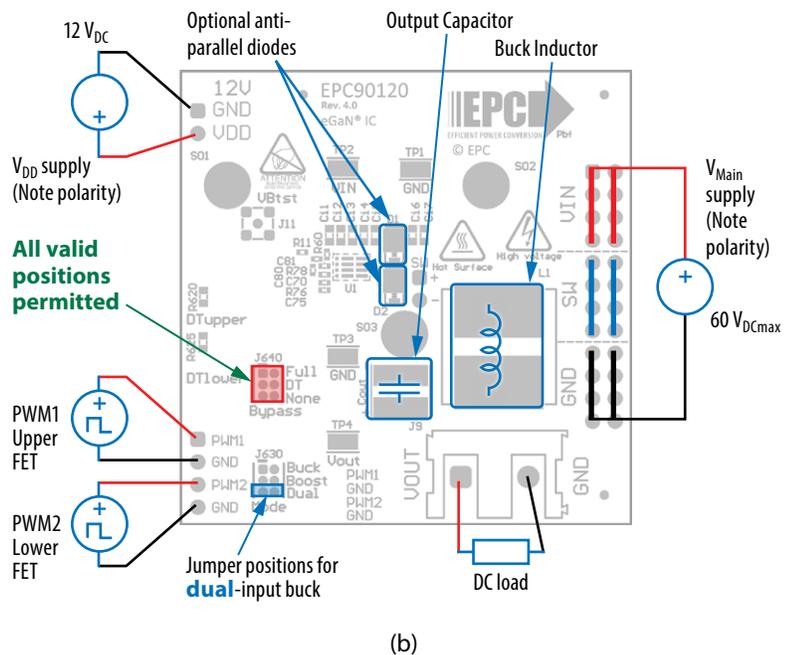
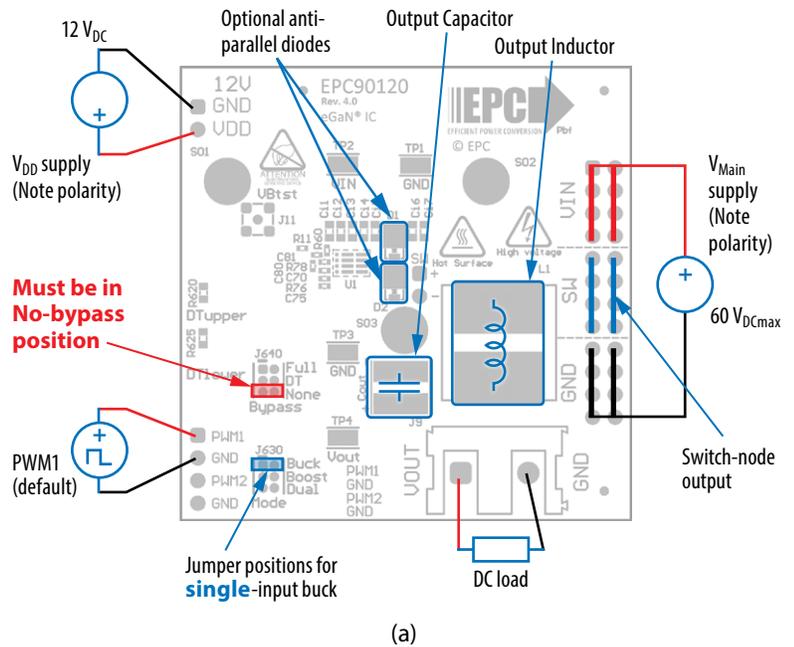


Figure 6: (a) Single-PWM input buck converter (b) Dual-PWM input buck converter configurations showing the supply, anti-parallel diodes, output capacitor, inductor, PWM, and load connections with corresponding jumper positions.

Boost Converter configuration

Warning: Never operate the boost converter mode without a load, as the output voltage can increase beyond the maximum ratings.

To operate the board as a boost converter, either a single or dual PWM inputs can be chosen using the appropriate jumper settings on J630 (mode).

To select **Single Input Boost Mode**, the bypass jumper J640 **must** be set to the **no-bypass mode**, the boost mode J630 **must** be selected as shown in figure.7(a).

To select **Dual Input Boost Mode**, the bypass jumper J640 **may** be configured to any of the valid settings, the **dual-input mode** J630 **must** be selected as shown in figure 7(b).

Note: It is important to provide the correct PWM signals that includes dead-time and polarity when operating in bypass mode.

Once the input source, dead-time settings and bypass configurations have been chosen and set, then the boards can be operated.

1. The inductor (L1) and input capacitors (labeled as Cout) can either be soldered onto the board, as shown in figure 7, or provided off board. Anti-parallel diodes can also be installed using the additional pads on the right side of the EPC2152 device.
2. With power off, connect the input power supply bus to V_{OUT} and ground / return to GND, or externally across the capacitor if the inductor L1 and Cout are provided externally. Connect the output voltage (labeled as VIN) to your circuit as required, e.g., resistive load.
3. With power off, connect the gate drive supply to VDD (J1, Pin-1) and ground return to GND (J1, Pin-2 indicated on the bottom side of the board).
4. With power off, connect the input PWM control signal to PWM1 and/or PWM2 according to the input mode setting chosen and ground return to any of GND J2 pins indicated on the bottom side of the board.
5. Turn on the gate drive supply – make sure the supply is between 7.5 V and 12 V.
6. Turn on the controller / PWM input source.
7. **Making sure the output is not open circuit**, and the input supply voltage is initially 0 V, turn on the power and slowly increase the voltage to the required value (**do not exceed the absolute maximum voltage**). Probe switch-node to see switching operation.
8. Once operational, adjust the PWM control, bus voltage, and load within the operating range and observe the output switching behavior, efficiency, and other parameters. Observe device temperature for operational limits.
9. For shutdown, please follow steps in reverse.

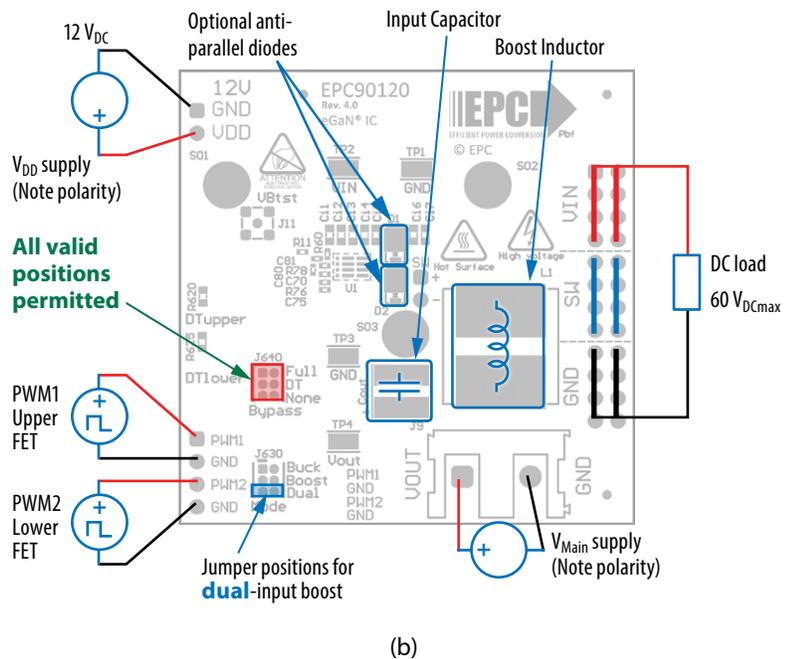
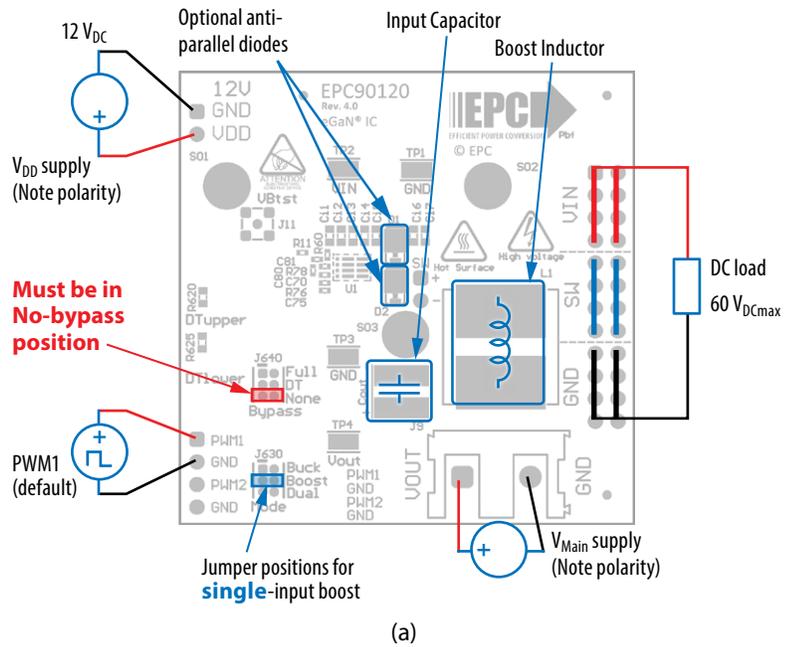


Figure 7: (a) Single-PWM input boost converter (b) Dual-PWM input boost converter configurations showing the supply, inductor, anti-parallel diodes, input capacitor, PWM, and load connections with corresponding jumper settings.

MEASUREMENT CONSIDERATIONS

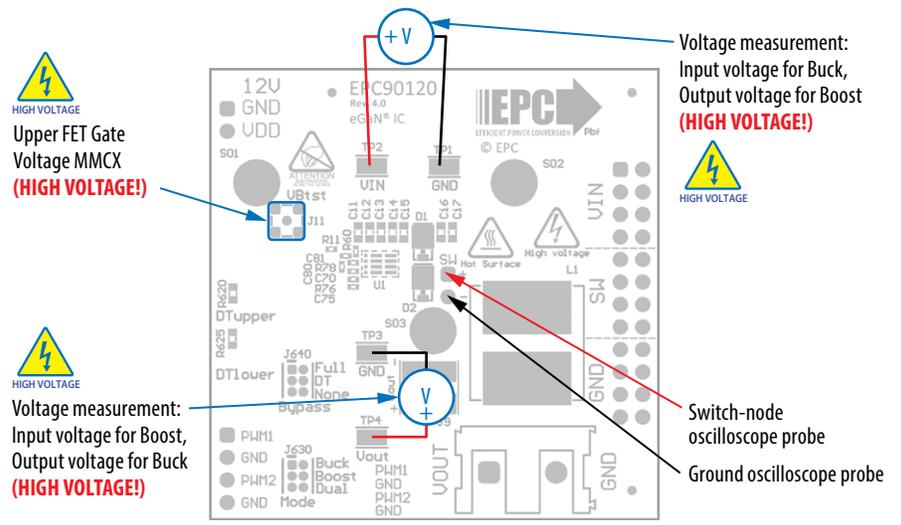
Measurement connections are shown in figure 8. Figure 12 shows an actual switch-node voltage measurement when operating the board as a buck converter.

When measuring the switch node voltage containing high-frequency content, care must be taken to provide an accurate high-speed measurement. An optional two pin header (J33) and an MMCX connector (J15) are provided for switch-node measurement.

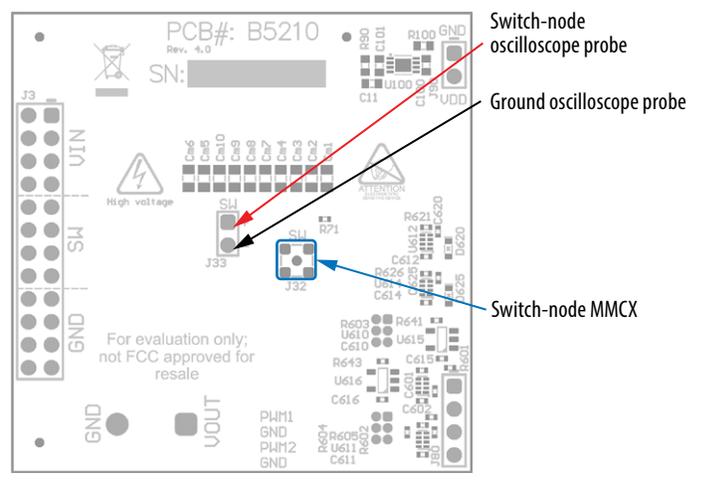
Differential probe is recommended for measuring the high-side bootstrap voltage. IsoVu probes from Tektronix has mating MMCX connector.

For regular passive voltage probes (e.g. TPP1000) measuring switch node using MMCX connector, probe adaptor is available. PN: 206-0663-xx

NOTE. For information about measurement techniques, the EPC website offers: [“AN023 Accurately Measuring High Speed GaN Transistors”](#) and the How to GaN educational video series, including: [HTG09- Measurement](#)



(a)



(b)

Figure 8: Measurement points (a) front side, (b) Back side

THERMAL CONSIDERATIONS

The EPC90120 board is equipped with three mechanical spacers that can be used to easily attach a heat-spreader or heatsink as shown in figure 9(a), and only requires a thermal interface material (TIM), a custom shape heat-spreader/heatsink, and screws. Prior to attaching a heat-spreader, any component exceeding 1 mm in thickness under the heat-spreader area will need to be removed from the board as shown in figure 9 (b).

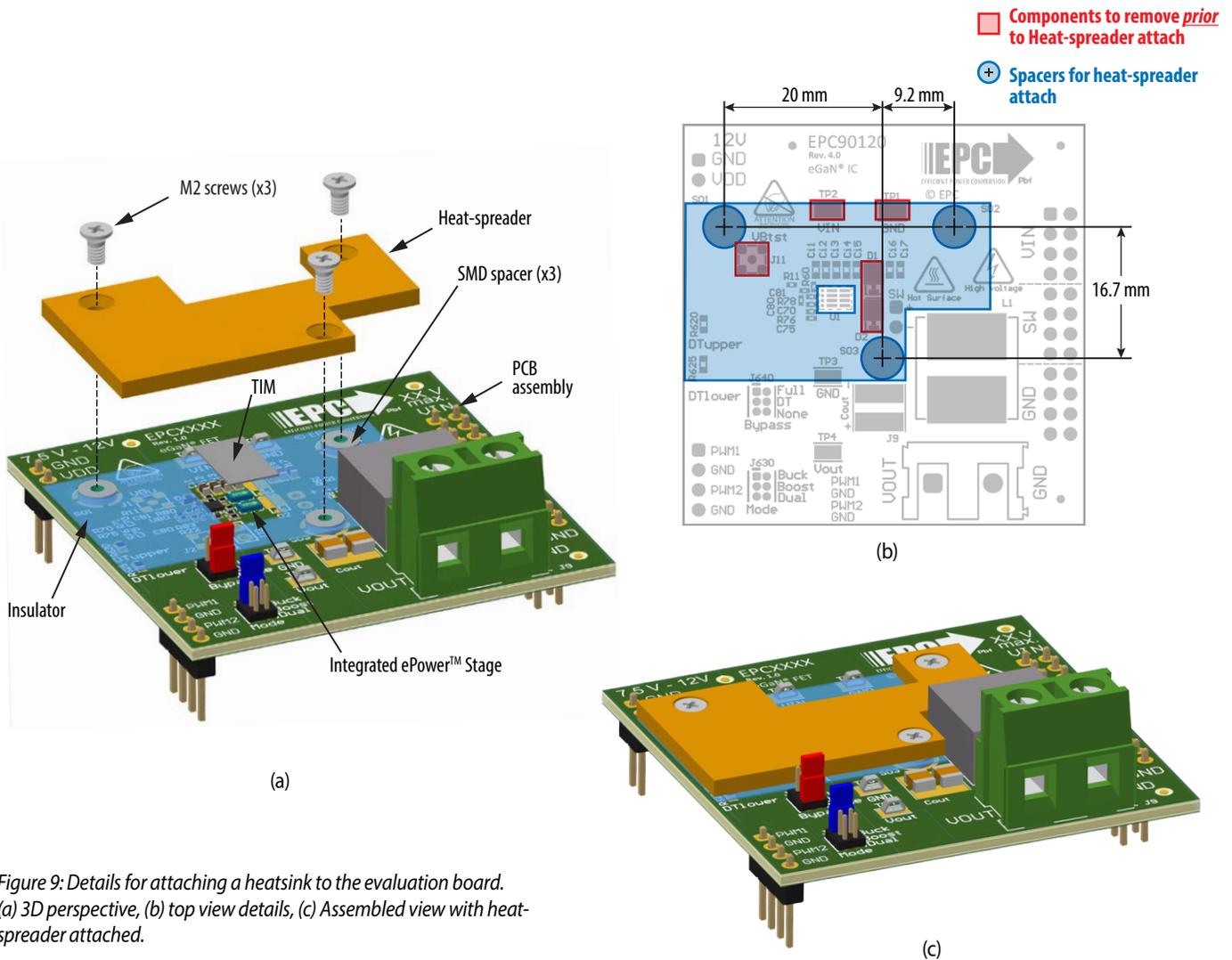


Figure 9: Details for attaching a heatsink to the evaluation board. (a) 3D perspective, (b) top view details, (c) Assembled view with heat-spreader attached.

The design of the heat-spreader is shown in figure 11 and can be made using **aluminum** or **tellurium copper** for higher performance.

The heat-spreader is held in place using countersunk screws that fasten to the mechanical spacers which will accept M2 x 0.4 mm thread screws such as McMasterCarr 91294A002.

When assembling the heatsink, it may be necessary add a thin insulation layer to prevent the heat-spreader from short circuiting with components that have exposed conductors such as capacitors and resistors, as shown in figure 11. **Note that the heat-spreader is ground connected by the lower most mounting post.** A rectangular opening in the insulator must be provided to allow the **TIM to be placed over the FETs to be cooled with a minimum clearance of 3 mm on each side of the rectangle encompassing the FETs.** The TIM will then be similar in size or slightly smaller than the opening in the insulator shown by the red dashed outline in figure 11.

EPC recommends Laird P/N: A14692-30, Tgard™ K52 with thickness of 0.051 mm the for the insulating material.

A TIM is added to improve the interface thermal conductance between the FETs and the attached heat exchanger. The choice of TIM needs to consider the following characteristics:

- **Mechanical compliance** – During the attachment of the heat spreader, the TIM underneath is compressed from its original thickness to the vertical gap distance between the spacers and the FETs. This volume compression exerts a force on the FETs. A maximum compression of 2:1 is recommended for maximum thermal performance and to constrain the mechanical force which maximizes thermal mechanical reliability.
- **Electrical insulation** – The backside of the Integrated ePower™ Stage is a silicon substrate that is connected to source and thus the upper FET in a half-bridge configuration is connected to the switch-node. To prevent short-circuiting the switch-node to the grounded thermal solution, the TIM must be of high dielectric strength to provide adequate electrical insulation in addition to its thermal properties.
- **Thermal performance** – The choice of thermal interface material will affect the thermal performance of the thermal solution. Higher thermal conductivity materials is preferred to provide higher thermal conductance at the interface.

EPC recommends the following thermal interface materials:

- **t-Global** P/N: TG-A1780 X 0.5 mm (highest conductivity of 17.8 W/m·K)
- **t-Global** P/N: TG-A6200 X 0.5 mm (moderate conductivity of 6.2 W/m·K)
- **Bergquist** P/N: GP5000-0.02 (~0.5 mm with conductivity of 5 W/m·K)
- **Bergquist** P/N: GPTGP7000ULM-0.020 (conductivity of 7 W/m·K)

NOTE. The EPC90120 evaluation board does not have any current or thermal protection on board. For more information regarding the thermal performance of EPC eGaN® FETs, please consult: D. Reusch and J. Glaser, *DC-DC Converter Handbook, a supplement to GaN Transistors for Efficient Power Conversion*, First Edition, Power Conversion Publications, 2015.

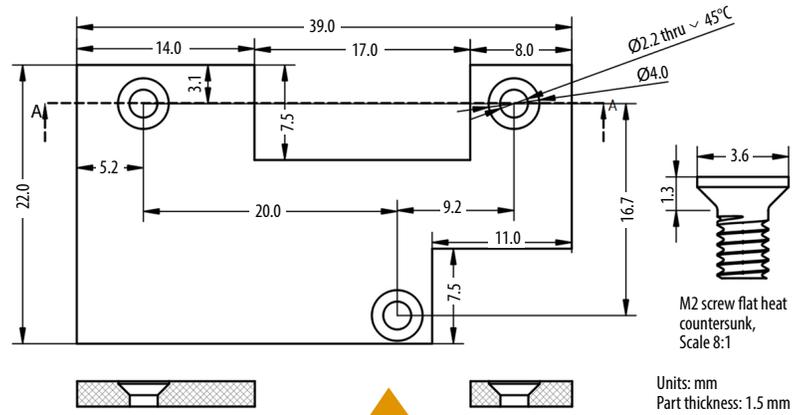


Figure 10: Heat-spreader details

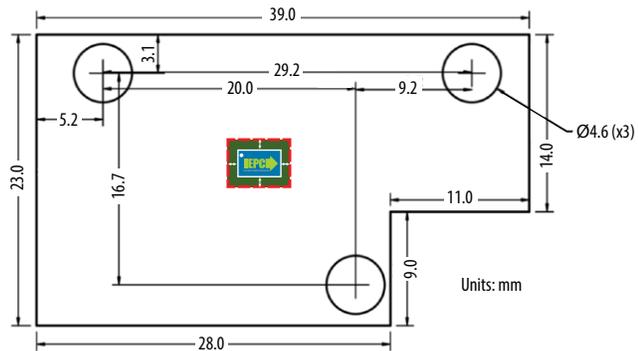
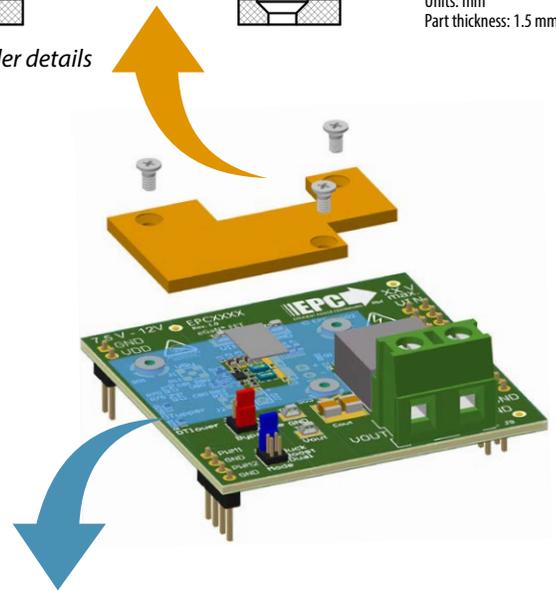


Figure 11: Insulator sheet details with opening for the TIM with location of the FETs

EXPERIMENTAL VALIDATION

The performance of EPC90120 was tested under the operating conditions given in table 2 unless otherwise specified.

No heatsink and moderate airflow (400 LFM) were used during the tests. For higher output current, a heat-spreader and TIM can be added as shown in figures 10 and 11. Then, a heatsink such as Wakefield Vette 567-24AB can be added on top of the heat-spreader.

Additional input and output capacitance are added to suppress input and output voltage ripple at high output current as shown in Table 2.

Table 2: Test conditions

Parameter	Max	Units
Regulated Input voltage	48	V
Regulated Output voltage	12	V
Switching frequency (f_s)	750 1000	kHz
Inductor (mounted on motherboard)	2.2	$\mu\text{H}^{[1]}$
Additional Input capacitance (min.)	23.5	$\mu\text{F}^{[2]}$
Additional Output capacitance (min.)	70.5	$\mu\text{F}^{[3]}$
Maximum case temperature	110	$^{\circ}\text{C}$
Dead time	10	ns

[1] 2.2 μH inductor from Vishay, P/N IHTH1125KZEB2R2M5A.

[2] Capacitors used:
4.7 μF , 100 V, x5 (P/N: GMC32X7R475K100NT)

[3] Capacitors used:
4.7 μF , 100 V, x5 (P/N: GMC32X7R475K100NT)
47 μF , 80 V, x1 (P/N: 80SXV47M)

ELECTRICAL PERFORMANCE

Measured Waveforms

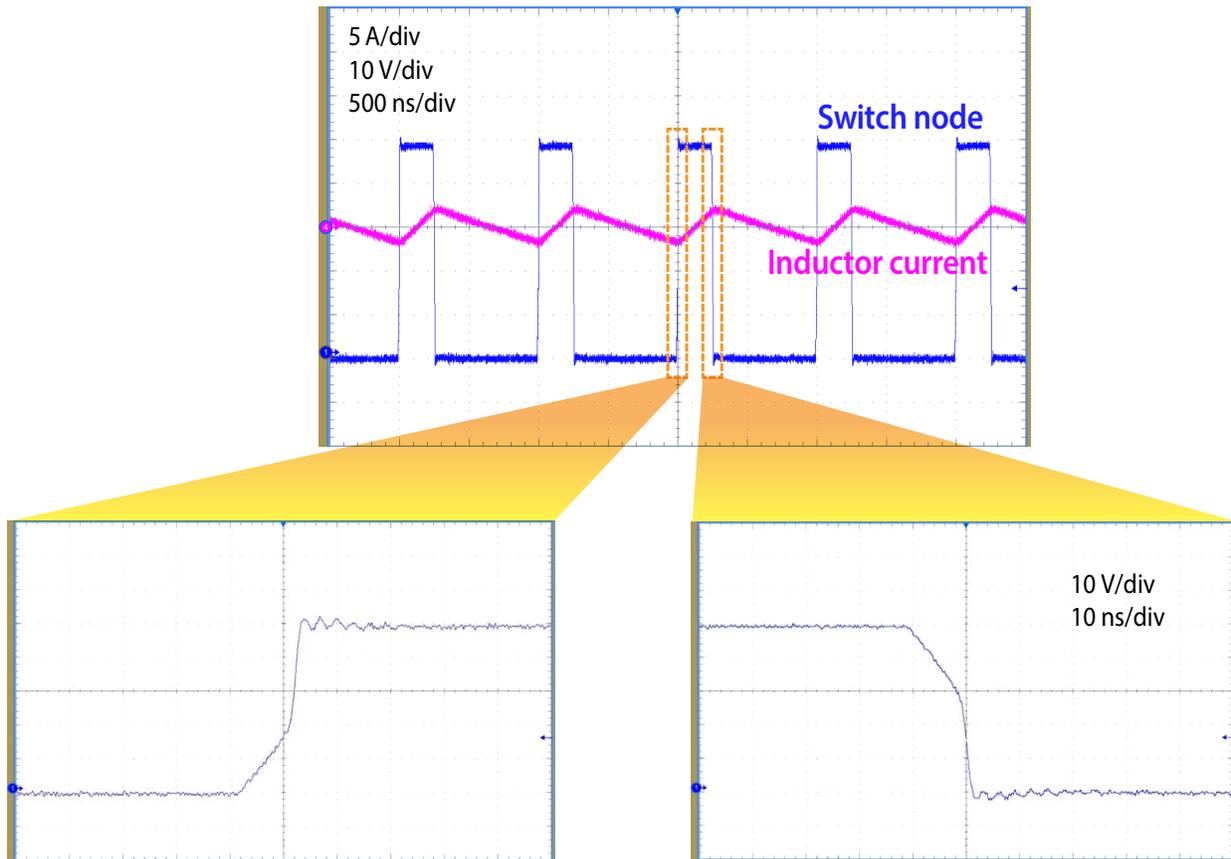


Figure 12: Measured inductor current and switch node waveforms when operating from 48 V at 1 MHz and delivering 0 A into a 12 V load

Measured Waveforms (continued)

Figure 13: Measured inductor current and switch node waveforms when operating from 48 V at 1 MHz and delivering 10 A into a 12 V load

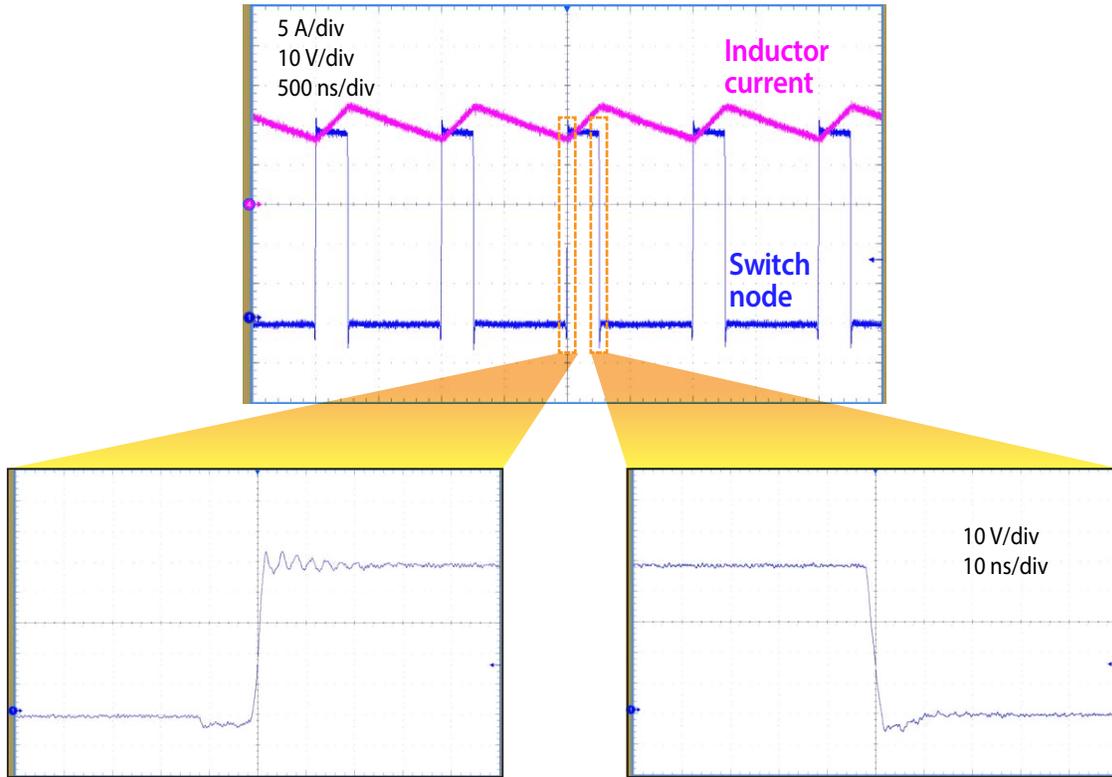


Figure 13: Measured inductor current and switch node waveforms when operating from 48 V at 1 MHz and delivering 10 A into a 12 V load

EFFICIENCY and POWER LOSSES

Figure 14 shows the efficiency and power loss results when operating from 48 V to 12 V at various switching frequencies using a 2.2 μ H inductor.

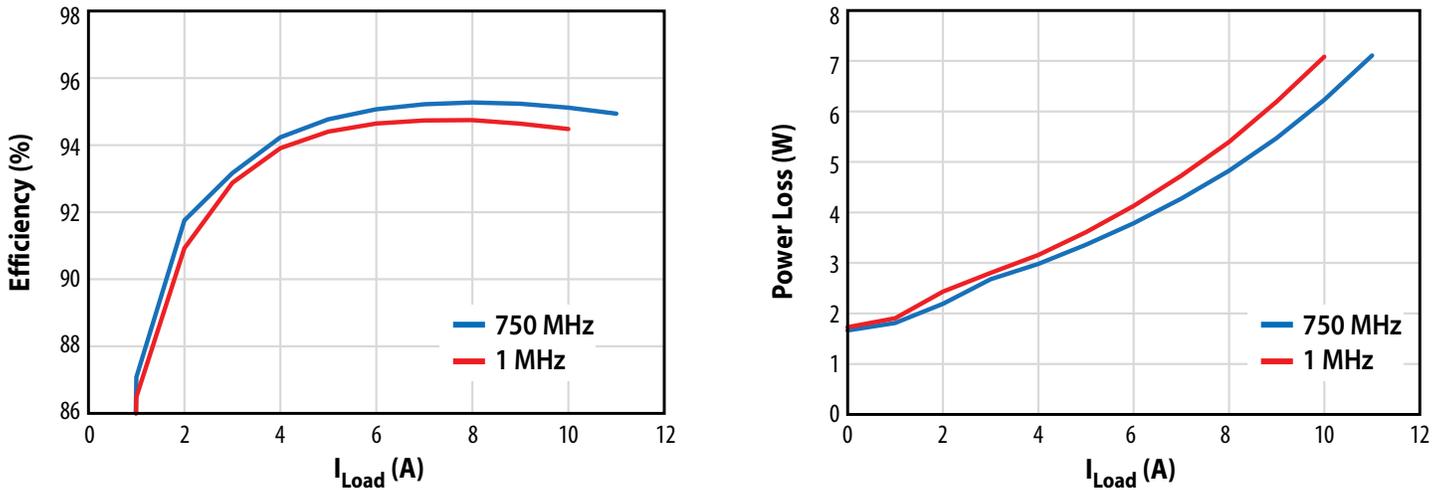


Figure 14: Measured efficiency and power loss operating at various switching frequencies and using $L = 2.2 \mu H$

THERMAL PERFORMANCE

Figure 15 shows the thermal performance of the board when operating at 48 V delivering 12 V and 10 A into the load with 400 LFM (moderate) airflow.

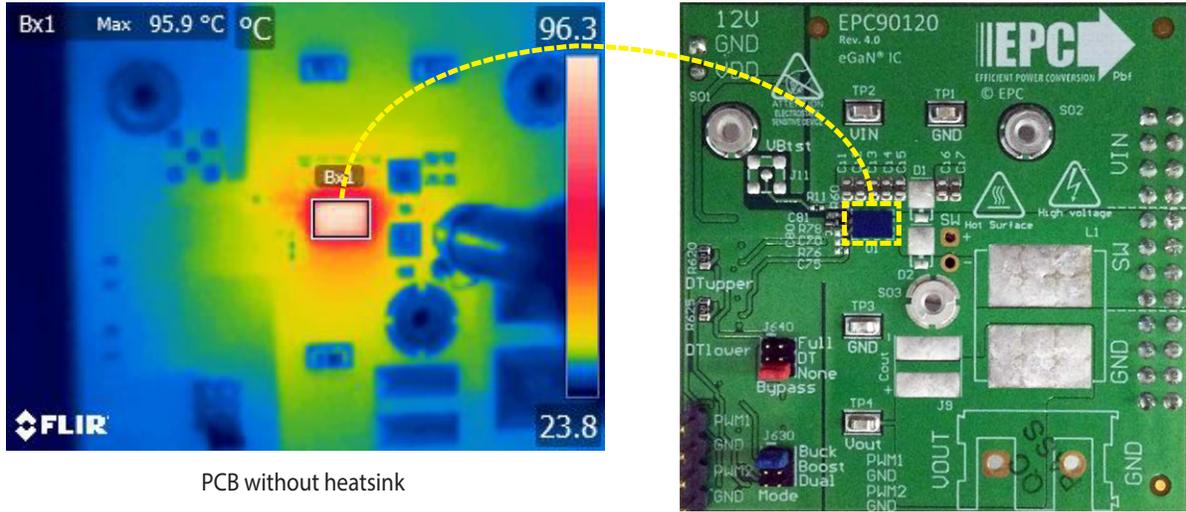


Figure 15: Measured thermal image showing the case temperature when operating under the following conditions: $f_s = 1 \text{ MHz}$, $I_{OUT} = 10 \text{ A}$ output, 25°C ambient and 400 LFM of airflow

THERMAL DERATING

Using the thermal setup for the board, additional testing at 500 LFM and 1000 LFM was conducted to determine the ambient temperature derating for the board with and without a heatsink attached. The temperature rise as function of load current is measured and the derating curves generated for a maximum case temperature of 110°C and shown in figure 16 for various switching frequencies.

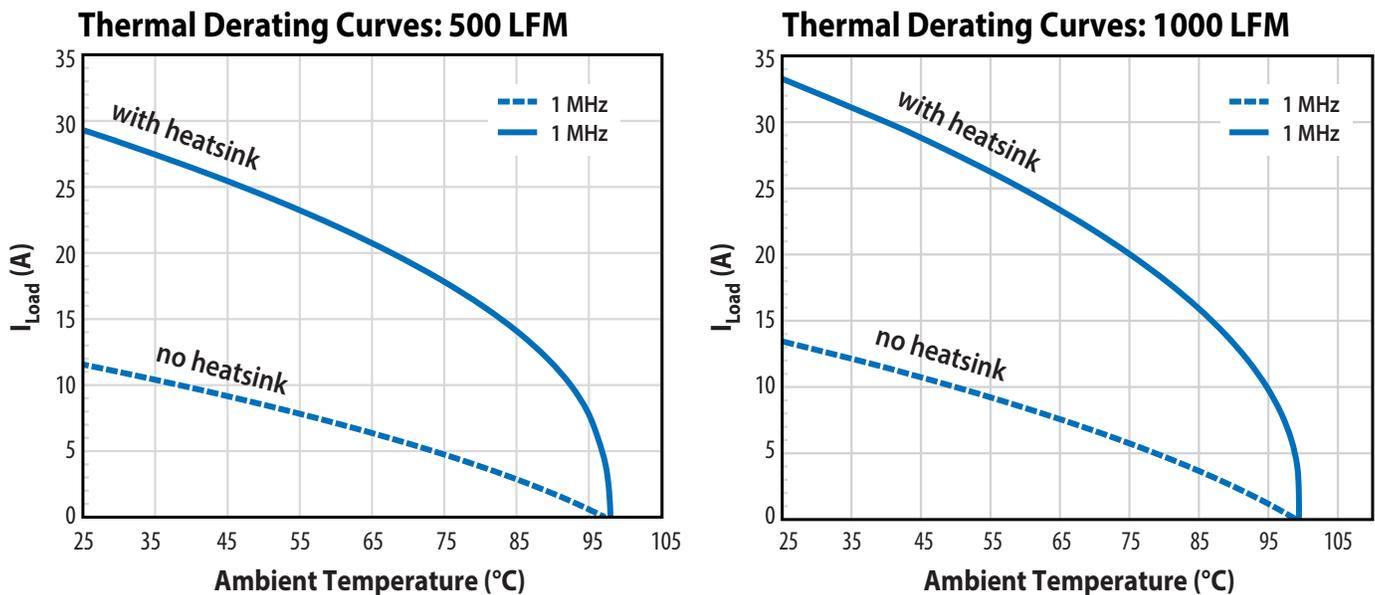


Figure 16: Typical thermal derating curves for two air flow rates, with and without a heatsink attached, measured with the board operating at 1 MHz and using a $2.2 \mu\text{H}$ inductor

For support files including schematic, Bill of Materials (BOM), and gerber files please visit the EPC90120 landing page at: <https://epc-co.com/epc/products/evaluation-boards/epc90120>

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