

High Performance, 3.2 GHz, 14-Output Jitter Attenuator with JESD204B and JESD204C Support

FEATURES

- ▶ Ultralow rms jitter: 44 fs typical (12 kHz to 20 MHz) at 2457.6 MHz
- ▶ Noise floor: -156 dBc/Hz at 2457.6 MHz
- ▶ Low phase noise: -141.7 dBc/Hz at 800 kHz, 983.04 MHz output
- ▶ Up to 14 LVDS, LVPECL, or CML type device clocks (DCLKs) from PLL2
 - ▶ Maximum CLKOUTx/CLKOUTx and SCLKOUTx/SCLKOUTx frequency up to 3200 MHz
- ▶ JESD204B- and JESD204C-compatible system reference (SYSREF) pulses
- ▶ 25 ps analog, and ½ VCO cycle digital delay independently programmable on each of 14 clock output channels
- ▶ SYSREF valid interrupt to simplify JESD204B and JESD204C synchronization
- ▶ Narrow-band, dual core VCOs
- ▶ Up to 2 buffered voltage controlled oscillator (VCXO) outputs
- ▶ Up to 4 input clocks in LVDS, LVPECL, CMOS, and CML modes
- ▶ Frequency holdover mode to maintain output frequency
- ▶ Loss of signal (LOS) detection and hitless reference switching
- ▶ 4× GPIOs alarms/status indicators to determine the health of the system
- ▶ External VCO input to support up to 6000 MHz
- ▶ On-board regulators for excellent PSRR
- ▶ 68-lead, 10 mm × 10 mm LFCSP package

APPLICATIONS

- ▶ JESD204B and JESD204C clock generation
- ▶ Cellular infrastructure (multicarrier GSM, LTE, W-CDMA)
- ▶ Data converter clocking
- ▶ Microwave baseband cards
- ▶ Phase array reference distribution

GENERAL DESCRIPTION

The HMC7044 is a high performance, dual-loop, integer-N jitter attenuator capable of performing reference selection and generation of ultralow phase noise frequencies for high speed data converters with either parallel or serial (JESD204B and JESD204C type) interfaces. The HMC7044 features two integer mode PLLs and overlapping on-chip VCOs that are SPI-selectable with wide tuning ranges around 2.5 GHz and 3 GHz, respectively. The device is designed to meet the requirements of GSM and LTE base station designs and offers a wide range of clock management and distribution features to simplify baseband and radio card clock tree designs. The HMC7044 provides 14 low noise and configurable outputs to offer flexibility in interfacing with many different components including data converters, field-programmable gate arrays (FPGAs), and mixer local oscillators (LOs).

The DCLK and SYSREF clock outputs of the HMC7044 can be configured to support signaling standards, such as CML, LVDS, LVPECL, and LVCMOS, and different bias settings to offset varying board insertion losses.

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REVISION HISTORY

10/2024—Rev. D to Rev. E

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FUNCTIONAL BLOCK DIAGRAM

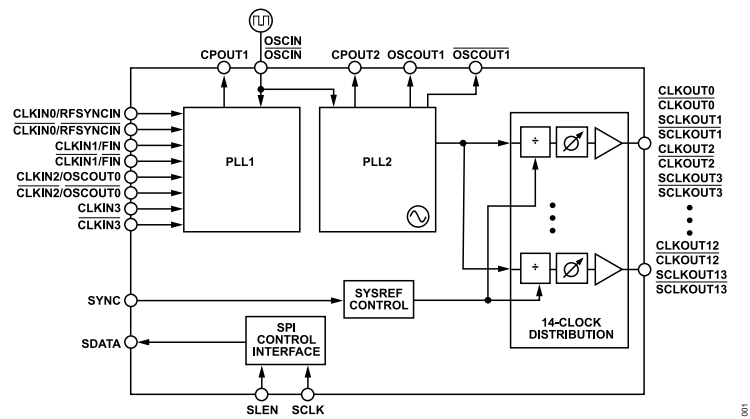


Figure 1.

SPECIFICATIONS

Unless otherwise noted, $f_{VCO} = 122.88$ MHz single-ended; CLKIN0/CLKIN0, CLKIN1/CLKIN1, CLKIN2/CLKIN2, and CLKIN3/CLKIN3 differential at 122.88 MHz; $f_{VCO} = 2949.12$ MHz; doubler is on; typical value is given for $V_{CC} = 3.3$ V; and $T_A = 25^\circ\text{C}$. Minimum and maximum values are given over the full V_{CC} and T_A (-40°C to $+85^\circ\text{C}$) variation, as listed in Table 1. Note that multifunction pins, such as CLKIN0/RFSYNCIN, are referred to either by the entire pin name or by a single function of the pin, for example, CLKIN0, when only that function is relevant.

CONDITIONS

Table 1.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|----------------------------------|-------|-------|-------|------------------|--|
| SUPPLY VOLTAGE, V_{CC} | | | | | |
| VCC1_VCO | 3.135 | 3.3 | 3.465 | V | $3.3\text{ V} \pm 5\%$, supply voltage for VCO and VCO distribution |
| VCC2_OUT | 3.135 | 3.3 | 3.465 | V | $3.3\text{ V} \pm 5\%$, supply voltage for Output Channel 2 and Output Channel 3 |
| VCC3_SYSREF | 3.135 | 3.3 | 3.465 | V | $3.3\text{ V} \pm 5\%$, supply voltage for common SYSREF divider |
| VCC4_OUT | 3.135 | 3.3 | 3.465 | V | $3.3\text{ V} \pm 5\%$, supply voltage for Output Channel 4, Output Channel 5, Output Channel 6, Output Channel 7 |
| VCC5_PLL1 | 3.135 | 3.3 | 3.465 | V | $3.3\text{ V} \pm 5\%$, supply voltage for the LDO used in PLL1 |
| VCC6_OSCOUT | 3.135 | 3.3 | 3.465 | V | $3.3\text{ V} \pm 5\%$, supply voltage for oscillator output path |
| VCC7_PLL2 | 3.135 | 3.3 | 3.465 | V | $3.3\text{ V} \pm 5\%$, supply voltage for the LDO used in PLL2 |
| VCC8_OUT | 3.135 | 3.3 | 3.465 | V | $3.3\text{ V} \pm 5\%$, supply voltage for Output Channel 8, Output Channel 9, Output Channel 10, and Output Channel 11 |
| VCC9_OUT | 3.135 | 3.3 | 3.465 | V | $3.3\text{ V} \pm 5\%$, supply voltage for Output Channel 0, Output Channel 1, Output Channel 12, and Output Channel 13 |
| TEMPERATURE | | | | | |
| Ambient Temperature Range, T_A | -40 | $+25$ | $+85$ | $^\circ\text{C}$ | |

SUPPLY CURRENT

For detailed test conditions, see Table 23 and Table 24.

Table 2.

| Parameter ^{1,2} | Min | Typ | Max | Unit | Test Conditions/Comments |
|----------------------------------|-----|-----|-----|------|--|
| CURRENT CONSUMPTION ³ | | | | | |
| VCC1_VCO | 157 | 225 | | mA | Typical value is given at $T_A = 25^\circ\text{C}$ with two LVDS clocks at divide by 8 |
| VCC2_OUT ⁴ | 65 | 250 | | mA | |
| VCC3_SYSREF | 12 | 37 | | mA | |
| VCC4_OUT ⁴ | 78 | 500 | | mA | Typical value is given at 25°C with two LVPECL high performance clocks, fundamental frequency of internal VCO (f_0), 2 SYSREF clocks (off) |
| VCC5_PLL1 | 39 | 125 | | mA | |
| VCC6_OSCOUT | 0 | 80 | | mA | |
| VCC7_PLL2 | 46 | 80 | | mA | |
| VCC8_OUT ⁴ | 124 | 500 | | mA | Typical value is given at 25°C with two LVPECL high performance clocks at divide by 2, 2 SYSREF clocks (off) |
| VCC9_OUT ⁴ | 65 | 500 | | mA | |
| Total Current | 586 | | | mA | Typical value is given at 25°C with two LVDS clocks at divide by 8, 2 SYSREF clocks (off) |

¹ Maximum values are guaranteed by design and characterization.

² Currents include LVPECL termination currents.

³ Maximum values are for all circuits enabled in their worst case power consumption mode, PVT variations, and accounting for peak current draw during temporary synchronization events.

⁴ Typical specification applies to a normal usage profile (Profile 1 in Table 24), where PLL1 and PLL2 are locked, but very low duty cycle currents (sync events) and some optional features are disabled. This specification assumes output configurations as described in the test conditions/comments column.

SPECIFICATIONS

DIGITAL INPUT/OUTPUT (I/O) ELECTRICAL SPECIFICATIONS

Table 3.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|------|----------------------------|----------|----------|--|
| DIGITAL INPUT SIGNALS (RESET, SYNC, SLEN, SCLK) | | | | | |
| Safe Input Voltage Range ¹ | -0.1 | | +3.6 | V | |
| Input Load | | 0.3 | | pF | |
| Input Voltage | | | | | |
| Input Logic High (V_{IH}) | 1.2 | | V_{CC} | V | |
| Input Logic Low (V_{IL}) | 0 | | 0.5 | V | |
| SPI Bus Frequency | | | 10 | MHz | |
| DIGITAL BIDIRECTIONAL SIGNALS CONFIGURED AS INPUTS (SDATA, GPIO4, GPIO3, GPIO2, GPIO1) | | | | | |
| Safe Input Voltage Range ¹ | -0.1 | | +3.6 | V | |
| Input Capacitance | | 0.4 | | pF | |
| Input Resistance | | 50G | | Ω | |
| Input Voltage | | | | | |
| Input Logic High (V_{IH}) | 1.22 | | V_{CC} | V | |
| Input Logic Low (V_{IL}) | 0 | | 0.24 | V | |
| Input Hysteresis | | 0.2 | | V | Occurs around 0.85 V |
| GPIO1 TO GPIO4 ALARM MUXING/DELAY | | | | | |
| Delay from Internal Alarm/Signal to General-Purpose Output (GPO) Driver | | 2 | | ns | Does not include t_{DGPO} |
| DIGITAL BIDIRECTIONAL SIGNALS CONFIGURED AS OUTPUTS (SDATA, GPIO4, GPIO3, GPIO2, GPIO1) | | | | | |
| CMOS MODE | | | | | |
| Logic 1 Level | 1.6 | 1.9 | 2.2 | V | |
| Logic 0 Level | | 0 | 0.1 | V | |
| Output Drive Resistance (R_{DRIVE}) | | 50 | | Ω | |
| Output Driver Delay (t_{DGPO}) | | $1.5 + 42 \times C_{LOAD}$ | | ns | Approximately $1.5 \text{ ns} + 0.69 \times R_{DRIVE} \times C_{LOAD}$ (C_{LOAD} in nF) |
| Maximum Supported DC Current ¹ | | | 0.6 | mA | |
| OPEN-DRAIN MODE ¹ | | | | | |
| Logic 1 Level | | | 3.6 | V | External 1 k Ω pull-up resistor 3.6 V maximum permitted; specifications set by external supply |
| Logic 0 Level | | 0.13 | 0.28 | V | Against a 1 k Ω external pull-up resistor to 3.3 V |
| Pull-Down Impedance | | 60 | | Ω | |
| Maximum Supported Sink Current | | | 5 | mA | |

¹ Guaranteed by design and characterization.

PLL1 CHARACTERISTICS

Table 4.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-------|-----|-----|-------|--|
| PLL1 REFERENCE INPUTS (CLKIN0/CLKIN0, CLKIN1/CLKIN1, CLKIN2/CLKIN2, CLKIN3/CLKIN3) | | | | | |
| Reliable Signal Swing | | | | | |
| Differential | 0.375 | | 1.4 | V p-p | Differential, keep signal at reference input pin <2.8 V, measured at 800 MHz |
| Single-Ended ¹ | 0.375 | | 1.4 | V p-p | <250 MHz; keep signal at reference input pin <2.8 V |

SPECIFICATIONS

Table 4. (Continued)

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|------------------|------------------------------------|----------------------|--------------|---|
| Common-Mode Range | 0.4 | | 2.4 | V | If user supplied, on-chip V_{CM} is approximately 2.1 V |
| Input Impedance | | 100 to 2000 | | Ω | User selectable; differential |
| Return Loss | | -12 | | dB | When terminated with 100 Ω differentially |
| PLL1 REFERENCE DIVIDER | | | | | |
| 8-Bit Lowest Common Multiple (LCM) Dividers | 1 | | 255 | | |
| 16-Bit R Divider (R1) | 1 | | 65,535 | | |
| PLL1 FEEDBACK DIVIDER | | | | | |
| 16-Bit N Divider (N1) | 1 | | 65,535 | | |
| PLL1 FREQUENCY LIMITATIONS | | | | | |
| PLL1 REF Input Frequency (f_{REF}) | 0.00015 | | 800 | MHz | Minimum specification set by Phase Detector 1 (PD1) low limit |
| Digital LOS/LCM Frequency (f_{LCM}) | 0.00015 | | 123 | MHz | Typically run at about 38.4 MHz |
| PD1 Frequency (f_{PD1}) | 0.00015 | | 50 | MHz | Minimum specification = VCXO minimum frequency \div 65,535; 9.76 MHz typical |
| PLL1 CHARGE PUMP | | | | | |
| Charge Pump Current Range (I_{CP1}) | | 120 to 1920 | | μA | I_{CP1} from 0 to 15, VCXO control voltage (V_{TUNE}) = 1.4 V |
| I_{CP1} Variation over Process Voltage Temperature (PVT) | | ± 15 | | % | $V_{TUNE} = 1.4$ V |
| Source/Sink Current Mismatch | | 2 | | % | Source/sink mismatch at 1.4 V |
| Charge Pump Current Step Size | | 120 | | μA | |
| Charge Pump Compliance Range ¹ | | 0.4 to 2.5 | | V | I_{CP} variation less than 10% |
| | | 0.1 to 2.7 | | V | Maintain lock in test environment |
| PLL1 NOISE PROFILE ¹ | | | | | |
| Floor Figure of Merit (FOM) | | -222 | | dBc/Hz | Normalized to 1 Hz |
| Flicker FOM | | -252 | | dBc/Hz | Normalized to 1 Hz |
| Flicker Noise | | Determined by formula ² | | dBc/Hz | At f_{OUT} , f_{OFFSET} |
| Noise Floor | | Determined by formula ³ | | dBc/Hz | At f_{OUT} , f_{PD1} |
| Total Phase Noise (Unfiltered) | | Determined by formula ⁴ | | dBc/Hz | |
| PLL1 BANDWIDTH AND ACQUISITION TIMES ¹ | | | | | |
| Supported Loop Bandwidths (PLL1_BW) ⁵ | $f_{LCM}/2^{25}$ | | $f_{PD1}/10$ | Hz | Typically PLL1 low BW is set by the application and ranges between 5 Hz and 2 kHz |
| PLL1 Slew Time ⁶ | | | $N1/f_{DELTA_VCXO}$ | sec | $N1 = 10$ (typical) and $f_{DELTA_VCXO} = 10$ kHz (typical) results in 1 ms of slew time |
| PLL1 Linear Acquisition Time | | $5/PLL1_BW$ | | sec | When VCXO has stopped slewing to steady state (within 5°) |
| PLL1 Phase Error at PD1 Invalidates Lock | | ± 2.9 | | ns | |
| PLL1 Lock Detect Timer Period (t_{LKD}) ⁷ | | 4 to 2^{26} | | t_{LCM} | User-selectable low phase error counts to declare lock |
| PLL1 BEHAVIOR ON REFERENCE FAILURE ¹ | | | | | |
| LOS Assertion Delay ⁷ | $2 + t_{DGPO}$ | | $3 + t_{DGPO}$ | t_{LCM} | From missing signal edge to alarm on GPO |
| Erroneously Active I_{CP1} Time on Reference Failure ⁸ | 0 | | 8 | ns | |
| Temporary Frequency Glitch Due to Reference Failure | | 0.03 | | ppm | $I_{CP1} = 1$ mA, $C12 = 4.6$ nF, Crystek CVPD-952 VCXO |
| Integrated Frequency Error Due to Reference Failure | | 0.016 | | ppm | $I_{CP1} = 1$ mA, $C13 = 1$ μF , Crystek CVPD-952 VCXO |
| Signal Valid Time to Clear LOS ⁹ | 2 | | 3 | t_{LOSVAL} | |
| PLL1 V_{TUNE} LEAKAGE SOURCES | | | | | |
| Charge Pump Tristate Leakage Current | | 0.2 | | nA | |
| Board Level XTAL Tune Input Port | | 0.5 | | nA | Crystek CVPD-952 VCXO |

SPECIFICATIONS

Table 4. (Continued)

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|---------|--------------------------|------------------------|--|
| Board Level Loop Filter Components | | 2 | | nA | C12 = 4.6 nF, C13 = 1 μ F, R9 = 11 k Ω , C15 = unpopulated |
| HOLDOVER CHARACTERISTICS | | | | | |
| V _{TUNE} Drift Over 1 sec in Tristate Mode Holdover | | 2 | | mV | C12 = 4.6 nF, C13 = 1 μ F, R9 = 11 k Ω , CVPD-950 VCXO |
| Analog-to-Digital Converter (ADC)/Digital-to-Analog Converter (DAC) Resolution | | 19 | | mV | 7-bit, monotonic, no missing code |
| ADC/DAC Code 0 Voltage | | 0.28 | | V | |
| ADC/DAC Code 127 Voltage | | 2.71 | | V | |
| DAC Temperature Stability | | 0.07 | | mV/°C | At maximum code |
| ADC/DAC Integral Nonlinearity (INL) | | -0.11 | | LSBs | Worst case across codes |
| Holdoff Timer Period ^{1, 10} | 1 | | 2 ²⁶ | t _{LCM} | |
| HOLDOVER EXIT—INITIAL PHASE OFFSETS ¹ | | | | | |
| Exit Criteria = Wait for Low Phase Error | | | | | The phase offset to make up after a transition from holdover to acquisition when using this feature |
| Exit Action = None | | ± 4 | | ns | |
| Exit Criteria = Any ¹¹ | | | | | |
| Exit Action = Reset Dividers | 1 | | 2 | t _{VCXO} | Assumes N2 > 3 and dividers are reset upon exit; note that VCXO lags at start; value applies as the starting phase error if DAC assisted release is used |
| Exit Action = None | | | $\pm N1$ | t _{VCXO} | Dividers are not reset upon exit |
| HOLDOVER EXIT CHARACTERISTICS ^{1, 12} | | | | | |
| DAC Assisted Release Period per Step (t _{DACASSIST}) | 1/2 | | 1/16 | t _{LKD} | Based on lock detect timer setpoint |
| DAC Assisted Release Time | | | 9 | t _{DACASSIST} | Time from decision to leave holdover until in fully natural acquisition; assumes no interruption by LOS or user |
| Delay of Exit Criteria ¹³ = Wait for Low Phase Error ¹⁴ | | | N1/f _{ERR_VCXO} | sec | |
| HOLDOVER EXIT—FREQUENCY TRANSIENTS vs. MODE | | | | | |
| Peak Frequency Transient | | | | | |
| DAC Assisted Release | | 2 | | ppm | Only available if using DAC-based holdover |

¹ Guaranteed by design and characterization.² See the [PLL1 Noise Calculations](#) section for more information on how to calculate the flicker noise for PLL1.³ See the [PLL1 Noise Calculations](#) section for more information on how to calculate the noise floor for PLL1.⁴ See the [PLL1 Noise Calculations](#) section for more information on how to calculate the total phase noise (unfiltered) for PLL1.⁵ Set by external components. Set the lock detect thresholds (PLL1 Lock Detect Timer[4:0] in Register 0x0028) appropriately in the SPI.⁶ Depends on initial phase offset (worst case is proportional to N1) and VCXO excess tuning range available over the target (f_{DELTA_VCXO}). For PFD rates typical of PLL1, cycle slipping is normally insignificant.⁷ t_{LCM} is the least common multiple (LCM) of PLL1 clock input frequencies. The specification is given in multiples of t_{LCM}.⁸ If LOS triggers before the PFD edge is normally detected (more likely with high R1 values), the charge pump is more likely to disable before the next invalid comparison occurs. Otherwise, the fast tristate circuit disables the charge pump after about 4 ns (8 ns worst case) of phase error.⁹ t_{LOSVAL} is a register value that is programmable from 1, 2, 4, ..., 64 t_{LCM}.¹⁰ If the holdoff timer is used, the finite state machine (FSM) stays in holdover after LOS of the active reference before switching clocks, giving the original clock a chance to return.¹¹ t_{VCXO} is the VCXO clock period.¹² See the [PLL1 Holdover Exit](#) section.

SPECIFICATIONS

¹³ The time required for the phases to intersect is inversely proportional to the holdover frequency error. Note that the frequency error during holdover is expected to be much smaller than is available from the tuning range of the VCXO.

¹⁴ f_{ERR_VCXO} is the error frequency of the VCXO.

PLL2 CHARACTERISTICS

Table 5.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--------------------------------------|---------|-------------|--------|----------|---|
| PLL2 VCXO INPUT | | | | | |
| Recommended Swing | | | | | |
| Differential | 0.2 | | 1.4 | V p-p | Differential, keep signal at OSCIN and \overline{OSCIN} pins < 2.8 V |
| Single-Ended (<250 MHz) ¹ | 0.2 | | 1.4 | V p-p | Keep signal at OSCIN and \overline{OSCIN} pins < 2.8 V |
| Common-Mode Range | 1.6 | 2.1 | 2.4 | V | If user supplied, on-chip V_{CM} is approximately 2.1 V |
| VCXO Input Slew Rate | 300 | | | mV/ns | Slew rates as low as 100 mV/ns are functional, but can degrade the phase noise plateau by about 3 dB |
| Input Capacitance | | 1.5 | | pF | Per side; 3 pF differential |
| Differential Input Resistance | | 100 to 1000 | | Ω | User selectable |
| Return Loss | | -12 | | dB | When terminated with 100 Ω differential |
| PLL2 EXTERNAL VCO INPUT | | | | | |
| Recommended Input Power, AC-Coupled | | | | | |
| Differential | -6 | | 6 | dBm | |
| Single-Ended ¹ | -6 | | 6 | dBm | |
| Return Loss | | -12 | | dB | When terminated with 100 Ω differential |
| External VCO Frequency ¹ | | | | | |
| | 400 | | | MHz | When all channel dividers are equal to one or channels are in the fundamental mode. If <1 GHz, set the low frequency external VCO path bit (Register 0x0064, Bit 0) |
| | 800 | | | MHz | When channel dividers are larger than 1 and synchronization is needed |
| | | | 3200 | MHz | External VCO Divider is disabled. Register 0x0064[1] = 0 |
| | | | 6000 | MHz | External VCO Divider is enabled. Register 0x0064[1] = 1 |
| Common-Mode Range ¹ | 1.6 | 2.1 | 2.2 | V | |
| PLL2 DIVIDERS | | | | | |
| 12-Bit Reference Divider Range (R2) | 1 | | 4095 | | |
| 16-Bit Feedback Divider Range (N2) | 8 | | 65,535 | | |
| PLL2 FREQUENCY LIMITATIONS | | | | | |
| VCXO Frequency (f_{VCXO}) | 10 | | 500 | MHz | 122.88 MHz or 155 MHz are typical |
| VCXO Duty Cycle | | | | | |
| Using Doubler ¹ | 40 | | 60 | % | Distortion can lead to a spur at $f_{PD}/2$ offset, note that minimum pulse width > 3 ns |
| Reference Doubler Input Frequency | 10 | | 175 | MHz | |
| R2 Input Frequency | 10 | | 500 | MHz | |
| PD2 Frequency (f_{PD2}) | 0.00015 | | 250 | MHz | Recommended at high end of the range for best phase noise; typically 122.88 MHz \times 2 |
| PLL2 CHARGE PUMP | | | | | |
| Current Range (I_{CP2}) | | 160 to 2560 | | μ A | I_{CP2} setting from 0 to 15 with 160 μ A step size, $V_{TUNE} = 1.4$ V |
| I_{CP2} Variation over PVT | | ± 25 | | % | $V_{TUNE} = 1.4$ V |
| Source/Sink Current Mismatch | | 2 | | % | Source/sink mismatch at 1.4 V |
| Current Step Size | | 160 | | μ A | |
| Compliance Range | | 0.3 to 2.45 | | V | I_{CP} variation less than 10% |
| PLL2 NOISE PROFILE | | | | | |

SPECIFICATIONS

Table 5. (Continued)

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|------------------------------------|-----|-----------|---|
| Floor FOM | | -232 | | dBc/Hz | Normalized to 1 Hz |
| Flicker FOM | | -266 | | dBc/Hz | Normalized to 1 Hz |
| FOM Variation vs. PVT | | ±3 | | dB | |
| FOM Degradation | | 3 | | dB | At minimum VCXO slew rate |
| PLL2 Flicker Noise | | Determined by formula ² | | dBc/Hz | At f_{OUT} , f_{OFFSET} |
| PLL2 Noise Floor | | Determined by formula ³ | | dBc/Hz | At f_{OUT} , f_{PD2} |
| PLL2 Total Phase Noise (Unfiltered) | | Determined by formula ⁴ | | dBc/Hz | |
| PLL2 BANDWIDTH AND ACQUISITION TIMES | | | | | |
| Supported Loop Bandwidths (PLL2_BW) | | 10 to 700 | | kHz | Set by external components |
| VCO Automatic Gain Control (AGC) Settling Time ¹ | | 10 | 20 | ms | Time from power-up of VCO before initiating calibration; this applies to the 100 nF/1 μ F configuration of external decoupling capacitors on the VCO supply network |
| VCO Calibration Time ⁵ | | 2694 | | t_{PD2} | N2 from 8 to 31 |
| | | 779 | | t_{PD2} | N2 from 32 to 256 |
| | | 214 | | t_{PD2} | N2 from 256 to 4095 |
| | | 139 | | t_{PD2} | N2 > 4095 |
| Temperature Range Postcalibration ¹ | -40 | | +85 | °C | Maintains lock from any temperature to any temperature |
| PLL2 Linear Acquisition Time | | 5/PLL2_BW | | sec | After VCXO has stopped slewing to steady state |
| PLL2 Lock Detect Timer Period ⁵ | | 512 | | t_{PD2} | Low phase error counts to declare lock |

¹ Guaranteed by design and characterization.

² See the [PLL2 Noise Calculations](#) section for more information on how to calculate the flicker noise for PLL2.

³ See the [PLL2 Noise Calculations](#) section for more information on how to calculate the noise floor for PLL2.

⁴ See the [PLL2 Noise Calculations](#) section for more information on how to calculate the total phase noise (unfiltered) for PLL2.

⁵ t_{PD2} is the period of Phase Detector 2.

VCO CHARACTERISTICS

Table 6.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------|----------|------|--------|--|
| VOLTAGE CONTROLLED OSCILLATOR (VCO) | | | | | |
| Frequency Tuning Range, On-Board VCOs ¹ | 2400 | | 2880 | MHz | Low VCO typical coverage |
| | 2650 | | 3200 | MHz | High VCO typical coverage |
| | 2400 | | 3200 | MHz | Guaranteed frequency coverage ² |
| Tuning Sensitivity | | 38 to 44 | | MHz/V | Low frequency VCO at 2457.6 MHz |
| | | 35 to 40 | | MHz/V | High frequency VCO at 2949.12 MHz |
| OPEN-LOOP VCO PHASE NOISE | | | | | |
| $f_{OUT} = 2457.6$ MHz | | | | | |
| $f_{OFFSET} = 100$ kHz | | -109 | | dBc/Hz | High performance mode, does not include floor contribution due to output network |
| $f_{OFFSET} = 800$ kHz | | -134 | | dBc/Hz | |
| $f_{OFFSET} = 1$ MHz | | -136 | | dBc/Hz | |
| $f_{OFFSET} = 10$ MHz | | -156 | | dBc/Hz | |
| Normalized Phase Noise Variation vs. Frequency | | ±2 | | dB | Sweep across both VCOs, all bands; normalize to 2457.6 MHz |
| Phase Noise Variation vs. Temperature | | ±2 | | dB | |
| Phase Noise Degradation in Low Performance Mode | | 2 | | dB | |

SPECIFICATIONS

¹ Guaranteed by design and characterization.

² Although the device covers this range without any gaps, for frequencies between ~2700 Hz and 2900 Hz, using a different VCO core to synthesize the frequency can be required as process parameters shift. Features are built into the HMC7044 to determine which core is selected for a given frequency that can fall in this range, but it can require software to configure these circuits appropriately.

CLOCK OUTPUT DISTRIBUTION CHARACTERISTICS

Table 7.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|---------------|------|--------------------------|---|
| CLOCK OUTPUT SKEW | | | | | Please refer to Phase Behavior of Synchronized Divided Clocks section for pulse generation skew behavior. |
| CLKOUTx/CLKOUTx to SCLKOUTx/SCLKOUTx Skew within One Clock Output Pair | | 15 | | ps | Same pair, same type termination, and configuration |
| Any CLKOUTx/CLKOUTx to Any SCLKOUTx/ SCLKOUTx | | 30 | | ps | Any pair, same type termination, and configuration |
| CLOCK OUTPUT DIVIDER | | | | | |
| 12-Bit Divider Range | 1 | | 4094 | | 1, 3, 5, and all even numbers up to 4094 |
| SYSREF CLOCK OUTPUT DIVIDER | | | | | |
| 12-Bit Divider Range | 1 | | 4094 | | 1, 3, 5 and all even numbers up to 4094; pulse generator behavior is only supported for divide ratios ≥ 32 |
| CLOCK OUTPUT ANALOG FINE DELAY | | | | | |
| Analog Fine Delay | | | | | |
| Adjustment Range ¹ | 135 | | 670 | ps | 24 delay steps, $f_{\text{CLKOUT}} = 983.04 \text{ MHz}$ |
| Resolution | | 25 | | ps | $f_{\text{CLKOUT}} = 983.04 \text{ MHz}$ (2949.12 MHz/3) |
| Maximum Analog Fine Delay Frequency ¹ | | 3200 | | MHz | |
| CLOCK OUTPUT COARSE DELAY (FLIP FLOP BASED) | | | | | |
| Coarse Delay Adjustment Range | 0 | | 17 | $\frac{1}{2}$ VCO period | 17 delay steps in $\frac{1}{2}$ VCO period |
| Coarse Delay Resolution | | 169.54 | | ps | $f_{\text{VCO}} = 2949.12 \text{ MHz}$ |
| Maximum Frequency Coarse Delay ¹ | | 3200 | | MHz | |
| CLOCK OUTPUT COARSE DELAY (SLIP BASED) | | | | | |
| Coarse Delay | | | | | |
| Adjustment Range | | 1 to ∞ | | VCO period | $f_{\text{VCO}} = 2949.12 \text{ MHz}$ |
| Resolution | | 339.08 | | ps | |
| Maximum Frequency Coarse Delay | | 1600 | | MHz | |

¹ Guaranteed by design and characterization.

SPUR CHARACTERISTICS

Table 8.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---------------------------------|-----|-----|-----|------|--------------------------|
| REFERENCE SPUR PERFORMANCE | | | | | |
| At 122.88 MHz and Its Harmonics | | -70 | | dBc | |

NOISE AND JITTER CHARACTERISTICS

Table 9.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|-----|-----|-----|------|---------------------------|
| CLOSED-LOOP PHASE NOISE—WIDE LOOP FILTER | | | | | For best integrated noise |
| Single Sideband Phase Noise | | | | | |
| At 2457.6 MHz ¹ | | | | | |

SPECIFICATIONS

Table 9. (Continued)

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|--------|-----|--------|--------------------------------------|
| At 614.4 MHz ¹ | | -98.0 | | dBc/Hz | Offset = 100 Hz |
| | | -111.1 | | dBc/Hz | Offset = 1 kHz |
| | | -119.8 | | dBc/Hz | Offset = 10 kHz |
| | | -125.2 | | dBc/Hz | Offset = 100 kHz |
| | | -126.9 | | dBc/Hz | Offset = 300 kHz |
| | | -131.3 | | dBc/Hz | Offset = 1 MHz |
| | | -150.0 | | dBc/Hz | Offset = 5 MHz |
| | | -154.0 | | dBc/Hz | Offset = 10 MHz |
| | | -156.3 | | dBc/Hz | Offset = 100 MHz |
| | | 44.0 | | fs | Integrated jitter = 12 kHz to 20 MHz |
| | | -110.4 | | dBc/Hz | Offset = 100 Hz |
| | | -122.8 | | dBc/Hz | Offset = 1 kHz |
| | | -131.3 | | dBc/Hz | Offset = 10 kHz |
| | | -136.6 | | dBc/Hz | Offset = 100 kHz |
| | | -138.3 | | dBc/Hz | Offset = 300 kHz |
| | | -142.7 | | dBc/Hz | Offset = 1 MHz |
| | | -157.6 | | dBc/Hz | Offset = 5 MHz |
| | | -158.8 | | dBc/Hz | Offset = 10 MHz |
| | | -159.2 | | dBc/Hz | Offset = 100 MHz |
| | | 50.0 | | fs | Integrated jitter = 12 kHz to 20 MHz |
| CLOSED-LOOP PHASE NOISE—NARROW LOOP FILTER | | | | | For best 800 kHz offset |
| Single Sideband Phase Noise | | | | | |
| At 2949.12 MHz ² | | | | | |
| At 983.04 MHz ² | | -100.9 | | dBc/Hz | Offset = 100 Hz |
| | | -103.8 | | dBc/Hz | Offset = 1 kHz |
| | | -106.9 | | dBc/Hz | Offset = 10 kHz |
| | | -109.9 | | dBc/Hz | Offset = 100 kHz |
| | | -132.3 | | dBc/Hz | Offset = 800 kHz |
| | | -134.5 | | dBc/Hz | Offset = 1 MHz |
| | | -152 | | dBc/Hz | Offset = 10 MHz |
| | | -155.3 | | dBc/Hz | Offset = 100 MHz |
| | | 108 | | fs | Integrated jitter = 12 kHz to 20 MHz |
| | | -110.4 | | dBc/Hz | Offset = 100 Hz |
| | | -113.3 | | dBc/Hz | Offset = 1 kHz |
| | | -116.4 | | dBc/Hz | Offset = 10 kHz |
| | | -119.4 | | dBc/Hz | Offset = 100 kHz |
| | | -141.7 | | dBc/Hz | Offset = 800 kHz |
| | | -143.7 | | dBc/Hz | Offset = 1 MHz |
| | | -157.1 | | dBc/Hz | Offset = 10 MHz |
| | | -157.1 | | dBc/Hz | Offset = 100 MHz |
| | | 102 | | fs | Integrated jitter 12 kHz to 20 MHz |
| OUTPUT NETWORK FLOOR FOM | | | | | |
| CML with 100 Ω Internal Termination (CML100) | | | | | |
| Fundamental Mode | | -250 | | dBc/Hz | High performance |
| Divide by 1 to Divide by N | | -248 | | dBc/Hz | High performance |
| Divide by 1 to Divide by N | | -247 | | dBc/Hz | Low power (4 dB less power) |

SPECIFICATIONS

Table 9. (Continued)

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|------------------------------------|-----|-------------------------|---------------------------------------|
| LVPECL | | | | | |
| Fundamental Mode | | -250 | | dBc/Hz | |
| Divide by 1 to Divide by N | | -247 | | dBc/Hz | |
| LVDS | | | | | |
| Divide by 1 to Divide by N | | -244 | | dBc/Hz | High performance |
| Divide by 1 to Divide by N | | -243 | | dBc/Hz | Low power (4 dB less power) |
| PHASE NOISE DEGRADATION DUE TO HARMONICS ³ | | | | | |
| Fundamental Only | | 0.00 | | dB | |
| Third Harmonic | | 0.25 | | dB | |
| Third and Fifth Harmonics | | 0.40 | | dB | |
| Third, Fifth, and Seventh Harmonics | | 0.50 | | dB | |
| Third, Fifth, Seventh, and Ninth Harmonics | | 0.53 | | dB | |
| Third Through 61 st Harmonics | | 0.64 | | dB | |
| PHASE NOISE FLOOR AND JITTER | | | | | |
| Phase Noise Floor at f_{OUT} | | Determined by formula ⁴ | | dBc/Hz | |
| Jitter Density of Floor at f_{OUT} | | Determined by formula ⁵ | | sec/ $\sqrt{\text{Hz}}$ | |
| RMS Additive Jitter Due to Floor | | Determined by formula ⁶ | | sec | From f_{OUT} and output channel FOM |

¹ PLL2 locked at 122.88 MHz $\times 2 \times 10$, wide (600 kHz) loop filter for best 12 kHz to 20 MHz jitter, CML100 high performance output buffer.

² PLL2 locked at 122.88 MHz $\times 2 \times 12$, narrow loop for best 800 Hz offset, CML100 high performance output buffer.

³ When the harmonics of the signal are captured in the measurement bandwidth of the receiving instrument/circuit, the noise power of those harmonics can fold and influence the overall noise. Their presence causes a decibel for decibel influence. For example, if the third harmonic is at -10 dBc, there is an additional noise contributor of 10 dB lower than the fundamental at all offsets that folds in-band and causes a 0.2 dB hit overall. The influence of the harmonics factoring into the degradation is primarily a function of the frequency of the buffer bandwidth relative to the third, fifth, and seventh harmonics. As the output frequency reduces, more harmonics fall into the observation bandwidth, and the degradation worsens, but only slightly. This effect produces a penalty of 0.65 dB maximum if harmonics up to the 61st harmonic is included.

⁴ See the [Phase Noise Floor and Jitter](#) section for more information on how to calculate the phase noise floor.

⁵ See the [Phase Noise Floor and Jitter](#) section for more information on how to calculate the jitter density of floor.

⁶ See the [Phase Noise Floor and Jitter](#) section for more information on how to calculate the rms additive jitter due to floor.

CLOCK OUTPUT DRIVER CHARACTERISTICS

Table 10.

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---------------------------------------|------|-----------------|------|-------------|--|
| CML MODE (LOW POWER) | | | | | $R_L = 100 \Omega$, 9.6 mA |
| -3 dB Bandwidth | | 1950 | | MHz | Differential output voltage = 980 mV p-p diff |
| Output Rise Time | | 175 | | ps | $f_{CLKOUT} = 245.76 \text{ MHz}$, 20% to 80% |
| | | 145 | | ps | $f_{CLKOUT} = 983.04 \text{ MHz}$, 20% to 80% |
| Output Fall Time | | 185 | | ps | $f_{CLKOUT} = 245.76 \text{ MHz}$, 20% to 80% |
| | | 145 | | ps | $f_{CLKOUT} = 983.04 \text{ MHz}$, 20% to 80% |
| Output Duty Cycle ¹ | 47.5 | 50 | 52.5 | % | $f_{CLKOUT} = 1075 \text{ MHz}$ (2150 MHz/2) |
| Differential Output Voltage Magnitude | | 1390 | | mV p-p diff | $f_{CLKOUT} = 245.76 \text{ MHz}$ (2949.12 MHz/12) |
| | | 1360 | | mV p-p diff | $f_{CLKOUT} = 983.04 \text{ MHz}$ (2949.12 MHz/3) |
| Common-Mode Output Voltage | | $V_{CC} - 1.05$ | | V | $f_{CLKOUT} = 245.76 \text{ MHz}$ (2949.12 MHz/12) |
| CML MODE (HIGH POWER) | | | | | $R_L = 100 \Omega$, 14.5 mA |
| 3 dB Bandwidth | | 1400 | | MHz | Differential output voltage = 1410 mV p-p diff |
| Output Rise Time | | 250 | | ps | $f_{CLKOUT} = 245.76 \text{ MHz}$, 20% to 80% |
| | | 165 | | ps | $f_{CLKOUT} = 983.04 \text{ MHz}$, 20% to 80% |
| Output Fall Time | | 255 | | ps | $f_{CLKOUT} = 245.76 \text{ MHz}$, 20% to 80% |
| | | 170 | | ps | $f_{CLKOUT} = 983.04 \text{ MHz}$, 20% to 80% |

SPECIFICATIONS

Table 10. (Continued)

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---------------------------------------|------|-----------------|------|-------------|--|
| Output Duty Cycle ¹ | 47.5 | 50 | 52.5 | % | $f_{CLKOUT} = 1075 \text{ MHz (2150 MHz/2)}$ |
| Differential Output Voltage Magnitude | | 2000 | | mV p-p diff | $f_{CLKOUT} = 245.76 \text{ MHz (2949.12 MHz/12)}$ |
| | | 1800 | | mV p-p diff | $f_{CLKOUT} = 983.04 \text{ MHz (2949.12 MHz/3)}$ |
| Common-Mode Output Voltage | | $V_{CC} - 1.6$ | | V | $f_{CLKOUT} = 245.76 \text{ MHz (2949.12 MHz/12)}$ |
| LVPECL MODE | | | | | $R_L = 150 \Omega$, 4.8 mA |
| 3 dB Bandwidth | | 2400 | | MHz | Differential output voltage = 1240 mV p-p diff |
| Output Rise Time | | 135 | | ps | $f_{CLKOUT} = 245.76 \text{ MHz, 20% to 80%}$ |
| | | 130 | | ps | $f_{CLKOUT} = 983.04 \text{ MHz, 20% to 80%}$ |
| Output Fall Time | | 135 | | ps | $f_{CLKOUT} = 245.76 \text{ MHz, 20% to 80%}$ |
| | | 130 | | ps | $f_{CLKOUT} = 983.04 \text{ MHz, 20% to 80%}$ |
| Output Duty Cycle ¹ | 47.5 | 50 | 52.5 | % | $f_{CLKOUT} = 1075 \text{ MHz (2150 MHz/2)}$ |
| Differential Output Voltage Magnitude | | 1760 | | mV p-p diff | $f_{CLKOUT} = 245.76 \text{ MHz (2949.12 MHz/12)}$ |
| | | 1850 | | mV p-p diff | $f_{CLKOUT} = 983.04 \text{ MHz (2949.12 MHz/3)}$ |
| Common-Mode Output Voltage | | $V_{CC} - 1.3$ | | V | $f_{CLKOUT} = 245.76 \text{ MHz (2949.12 MHz/12)}$ |
| LVDS MODE (LOW POWER) ² | | | | | 1.75 mA |
| Maximum Operating Frequency | | 600 | | MHz | Differential output voltage = 400 mV p-p diff |
| Output Rise Time | | 135 | | ps | $f_{CLKOUT} = 245.76 \text{ MHz, 20% to 80%}$ |
| | | 100 | | ps | $f_{CLKOUT} = 983.04 \text{ MHz, 20% to 80%}$ |
| Output Fall Time | | 135 | | ps | $f_{CLKOUT} = 245.76 \text{ MHz, 20% to 80%}$ |
| | | 95 | | ps | $f_{CLKOUT} = 983.04 \text{ MHz, 20% to 80%}$ |
| Output Duty Cycle ¹ | 47.5 | 50 | 52.5 | % | $f_{CLKOUT} = 1075 \text{ MHz (2150 MHz/2)}$ |
| Differential Output Voltage Magnitude | | 390 | | mV p-p diff | $f_{CLKOUT} = 245.76 \text{ MHz (2949.12 MHz/12)}$ |
| Common-Mode Output Voltage | | 1.1 | | V | $f_{CLKOUT} = 245.76 \text{ MHz (2949.12 MHz/12)}$ |
| LVDS MODE (HIGH POWER) ² | | | | | 3.5 mA |
| Maximum Operating Frequency | | 1700 | | MHz | Differential output voltage = 650 mV p-p diff |
| Output Rise Time | | 145 | | ps | $f_{CLKOUT} = 245.76 \text{ MHz, 20% to 80%}$ |
| | | 105 | | ps | $f_{CLKOUT} = 983.04 \text{ MHz, 20% to 80%}$ |
| Output Fall Time | | 145 | | ps | $f_{CLKOUT} = 245.76 \text{ MHz, 20% to 80%}$ |
| | | 100 | | ps | $f_{CLKOUT} = 983.04 \text{ MHz, 20% to 80%}$ |
| Output Duty Cycle ¹ | 47.5 | 50 | 52.5 | % | $f_{CLKOUT} = 1075 \text{ MHz (2150 MHz/2)}$ |
| Differential Output Voltage Magnitude | | 750 | | mV p-p diff | $f_{CLKOUT} = 245.76 \text{ MHz (2949.12 MHz/12)}$ |
| | | 730 | | mV p-p diff | $f_{CLKOUT} = 983.04 \text{ MHz (2949.12 MHz/3)}$ |
| Common-Mode Output Voltage | | 1.1 | | V | $f_{CLKOUT} = 245.76 \text{ MHz (2949.12 MHz/12)}$ |
| CMOS MODE | | | | | |
| Maximum Operating Frequency | | 600 | | MHz | Single-ended output voltage = 940 mV p-p diff |
| Output Rise Time | | 425 | | ps | $f_{CLKOUT} = 245.76 \text{ MHz, 20% to 80%}$ |
| Output Fall Time | | 420 | | ps | $f_{CLKOUT} = 245.76 \text{ MHz, 20% to 80%}$ |
| Output Duty Cycle ¹ | 47.5 | 50 | 52.5 | % | $f_{CLKOUT} = 1075 \text{ MHz (2150 MHz/2)}$ |
| Output Voltage | | | | | |
| High | | $V_{CC} - 0.07$ | | V | Load current = 1 mA |
| | | $V_{CC} - 0.5$ | | V | Load current = 10 mA |
| Output | | 0.07 | | V | Load current = 1 mA |
| | | 0.5 | | V | Load current = 10 mA |

¹ Guaranteed by design and characterization.² Refer to the [Clock Output Network](#) section for N-Pulse SYSREF generation operation.

ABSOLUTE MAXIMUM RATINGS

Table 11.

| Parameter | Rating |
|--|------------------|
| VCC1_VCO, VCC2_OUT, VCC3_SYSREF, VCC4_OUT, VCC5_PLL1, VCC6_OSCOUT, VCC7_PLL2, VCC8_OUT, VCC9_OUT | -0.3 V to +3.6 V |
| Maximum Junction Temperature (T_{JMAX}) | 125°C |
| Maximum Peak Reflow Temperature | 260°C |
| Storage Temperature Range | -65°C to +150°C |
| Operating Temperature Range | -40°C to +85°C |
| ESD Sensitivity Level | |
| Human Body Model | Class 1C |
| Charged Device Model | Class 2B |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required. θ_{JA} is the natural convection, junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance. θ_{JB} is the junction to bottom ground paddle thermal resistance.

Table 12. Thermal Resistance

| PCB Type | θ_{JA} | θ_{JC} | θ_{JB} | Unit |
|------------------|---------------|---------------|---------------|------|
| JEDEC 2s2p Board | 23.95 | 8.27 | 0.9 | °C/W |

TRANSISTOR COUNT

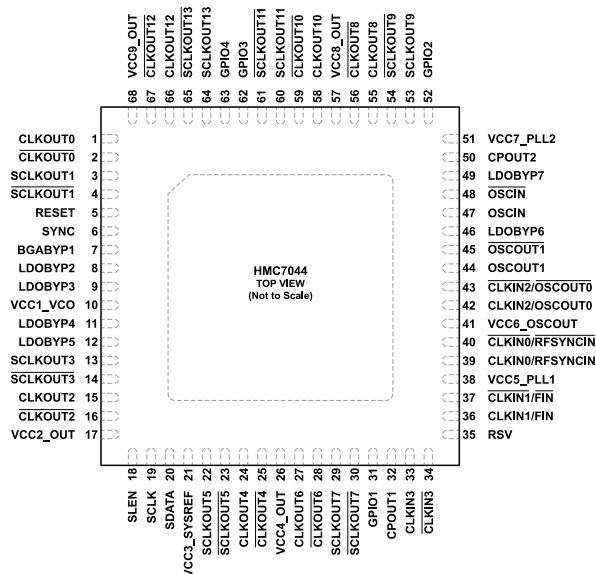
The transistor count for the HMC7044 is 340307 (CMOS) and 9688 (bipolar).

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES

1. EXPOSED PAD, CONNECT THE EXPOSED PAD TO A HIGH QUALITY RF/DC GROUND.

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Figure 2. Pin Configuration

Table 13. Pin Function Descriptions

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|------------------------------|-------------------|---|
| 1 | CLKOUT0 | O | True Clock Output Channel 0. Default DCLK profile. |
| 2 | $\overline{\text{CLKOUT0}}$ | O | Complementary Clock Output Channel 0. Default DCLK profile. |
| 3 | SCLKOUT1 | O | True Clock Output Channel 1. Default SYSREF profile. |
| 4 | $\overline{\text{SCLKOUT1}}$ | O | Complementary Clock Output Channel 1. Default SYSREF profile. |
| 5 | RESET | I | Device Reset Input. Active high. For normal operation, set RESET to 0. |
| 6 | SYNC | I | Synchronization Input. This pin is used for multichip synchronization. If not used, set SYNC to 0. |
| 7 | BGABYP1 | | Band Gap Bypass Capacitor Connection. Connect a 4.7 μF capacitor to ground. This pin affects all internally regulated supplies. |
| 8 | LDOBYP2 | | LDO Bypass 2. Connect a 4.7 μF capacitor to ground. The internal digital supply is 1.8 V. This pin is the LDO bypass for the PLL1, PLL2, and SYSREF sections. |
| 9 | LDOBYP3 | | LDO Bypass 3. Connect a 4.7 μF capacitor to ground. This pin is the 2.8 V supply to PLL1, Phase Frequency Detector 1 (PFD1), Charge Pump 1 (CP1), RF synchronization (RFSYNC), and Pin 36 buffers. |
| 10 | VCC1_VCO | P | 3.3 V Supply for VCO and VCO Distribution. |
| 11 | LDOBYP4 | | LDO Bypass 4. Connect a 1 μF capacitor to ground. This pin is the first stage regulator for the VCO supply. |
| 12 | LDOBYP5 | | LDO Bypass 5. Connect a 100 nF capacitor to LDOBYP4. This pin is the VCO core supply voltage. |
| 13 | SCLKOUT3 | O | True Clock Output Channel 3. Default SYSREF profile. |
| 14 | $\overline{\text{SCLKOUT3}}$ | O | Complementary Clock Output Channel 3. Default SYSREF profile. |
| 15 | CLKOUT2 | O | True Clock Output Channel 2. Default DCLK profile. |
| 16 | $\overline{\text{CLKOUT2}}$ | O | Complementary Clock Output Channel 2. Default DCLK profile. |
| 17 | VCC2_OUT | P | Power Supply for Clock Group 1 (Southwest)—Channel 2 and Channel 3. See the Clock Grouping, Skew, and Crosstalk section. |
| 18 | SLEN | I | SPI Latch Enable. |
| 19 | SCLK | I | SPI Clock. |
| 20 | SDATA | I/O | SPI Data. |
| 21 | VCC3_SYSREF | P | Power Supply for Common SYSREF Divider. |
| 22 | SCLKOUT5 | O | True Clock Output Channel 5. Default SYSREF profile. |
| 23 | $\overline{\text{SCLKOUT5}}$ | O | Complementary Clock Output Channel 5. Default SYSREF profile. |
| 24 | CLKOUT4 | O | True Clock Output Channel 4. Default DCLK profile. |

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 13. Pin Function Descriptions (Continued)

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|-----------------|-------------------|---|
| 25 | CLKOUT4 | O | Complementary Clock Output Channel 4. Default DCLK profile. |
| 26 | VCC4_OUT | P | Power Supply for Clock Group 2 (South)—Channel 4, Channel 5, Channel 6, and Channel 7. See the Clock Grouping, Skew, and Crosstalk section. |
| 27 | CLKOUT6 | O | True Clock Output Channel 6. Default DCLK profile. |
| 28 | CLKOUT6 | O | Complementary Clock Output Channel 6. Default DCLK profile. |
| 29 | SCLKOUT7 | O | True Clock Output Channel 7. Default SYSREF profile. |
| 30 | SCLKOUT7 | O | Complementary Clock Output Channel 7. Default SYSREF profile. |
| 31 | GPIO1 | I/O | Programmable General-Purpose Input/Output 1. |
| 32 | CPOUT1 | O | PLL1 Charge Pump Output. |
| 33 | CLKIN3 | I | True Reference Clock Input 3 of PLL1. |
| 34 | CLKIN3 | I | Complementary Reference Clock Input 3 of PLL1. |
| 35 | RSV | R | Reserved Pin. This pin must be tied to ground. |
| 36 | CLKIN1/FIN | I | True Reference Clock Input 1 of PLL1/External VCO Input for External VCO Mode. |
| 37 | CLKIN1/FIN | I | Complementary Reference Clock Input 1 of PLL1/Complementary External VCO Input for External VCO Mode. |
| 38 | VCC5_PLL1 | P | Power Supply for LDO, Used for PLL1. |
| 39 | CLKIN0/RFSYNCIN | I | True Reference Clock Input 0 of PLL1/RF Synchronization Input with Deterministic Delay. |
| 40 | CLKIN0/RFSYNCIN | I | Complementary Reference Clock Input 0 of PLL1/Complementary RF Synchronization Input with Deterministic Delay. |
| 41 | VCC6_OSCOUT | P | Power Supply for Oscillator Output Path. |
| 42 | CLKIN2/OSCOU0 | I/O | True Reference Clock Input 2 (Bidirectional Pin) of PLL1/Buffered Output 0 of Oscillator Input. |
| 43 | CLKIN2/OSCOU0 | I/O | Complementary Reference Clock Input 2 (Bidirectional Pin) of PLL1/Complementary Buffered Output 0 of Oscillator Input. |
| 44 | OSCOU1 | O | True Buffered Output 1 of Oscillator Input. |
| 45 | OSCOU1 | O | Complementary Buffered Output 1 of Oscillator Input. |
| 46 | LDOBYP6 | | LDO Bypass, Connect a 4.7 μ F capacitor to ground. This pin is the LDO bypass for R2, N2, Phase Frequency Detector 2 (PFD2), Charge Pump 2 (CP2), and the PLL2 loop filter. |
| 47 | OSCIN | I | True Feedback Input to PLL1. This pin is a reference input to PLL2. |
| 48 | OSCIN | I | Complementary Feedback Input to PLL1. This pin is a reference input to PLL2. |
| 49 | LDOBYP7 | | LDO Bypass. Connect a 4.7 μ F capacitor to ground. This pin is the LDO bypass for the VCXO buffer and frequency doubler oscillator output divider. |
| 50 | CPOUT2 | I/O | PLL2 Charge Pump Output. |
| 51 | VCC7_PLL2 | P | Power Supply for LDO for PLL2. |
| 52 | GPIO2 | I/O | Programmable General-Purpose Input/Output 2. |
| 53 | SCLKOUT9 | O | True Clock Output Channel 9. Default SYSREF profile. |
| 54 | SCLKOUT9 | O | Complementary Clock Output Channel 9. Default SYSREF profile. |
| 55 | CLKOUT8 | O | True Clock Output Channel 8. Default DCLK profile. |
| 56 | CLKOUT8 | O | Complementary Clock Output Channel 8. Default DCLK profile. |
| 57 | VCC8_OUT | P | Power Supply for Clock Group 3 (North)—Channel 8, Channel 9, Channel 10, and Channel 11. See the Clock Grouping, Skew, and Crosstalk section. |
| 58 | CLKOUT10 | O | True Clock Output Channel 10. Default DCLK profile. |
| 59 | CLKOUT10 | O | Complementary Clock Output Channel 10. Default DCLK profile. |
| 60 | SCLKOUT11 | O | True Clock Output Channel 11. Default SYSREF profile. |
| 61 | SCLKOUT11 | O | Complementary Clock Output Channel 11. Default SYSREF profile. |
| 62 | GPIO3 | I/O | Programmable General-Purpose Input/Output 3. Sleep input by default. |
| 63 | GPIO4 | I/O | Programmable General-Purpose Input/Output 4. Pulse generator request by default. |
| 64 | SCLKOUT13 | O | True Clock Output Channel 13. Default SYSREF profile. |
| 65 | SCLKOUT13 | O | Complementary Clock Output Channel 13. Default SYSREF profile. |
| 66 | CLKOUT12 | O | True Clock Output Channel 12. Default DCLK profile. |
| 67 | CLKOUT12 | O | Complementary Clock Output Channel 12. Default DCLK profile. |
| 68 | VCC9_OUT | P | Power Supply for Clock Group 0 (Northwest)—Channel 0, Channel 1, Channel 12, and Channel 13. See the Clock Grouping, Skew, and Crosstalk section. |

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS**Table 13. Pin Function Descriptions (Continued)**

| Pin No. | Mnemonic | Type ¹ | Description |
|---------|----------|-------------------|--|
| | EP | | Exposed Pad. Connect the exposed pad to a high quality RF/dc ground. |

¹ O is output, I is input, P is power, and I/O is input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, PFD PLL1 = 7.68 MHz, PFD PLL2 = 122.88 MHz $\times 2$; I_{CP1} = 1.92 mA, I_{CP2} = 2.56 mA (wide loop), I_{CP2} = 1.12 mA (narrow loop), PLL1 loop Bandwidth ~ 70 Hz, PLL2 wide loop Bandwidth ≈ 650 kHz, PLL2 narrow loop Bandwidth ≈ 215 kHz, PLL2 narrow loop filter = 1.1 nF | 160 Ω \times 33 nF; PLL2 wide loop filter = 150 pF | 430 Ω \times 4.7 nF; PLL1 loop filter = 4.7 nF | 10 μ F \times 1.2 k Ω .

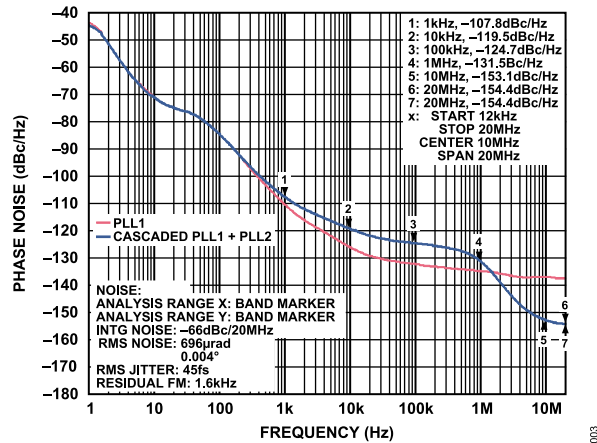


Figure 3. Cascaded Phase Noise at 2457.6 MHz, PLL2 Wide Loop Bandwidth

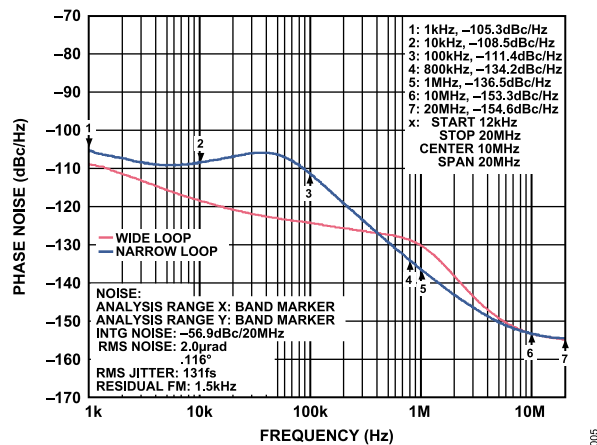


Figure 4. Phase Noise at 2457.6 MHz, Narrow vs. PLL2 Wide Loop Bandwidth

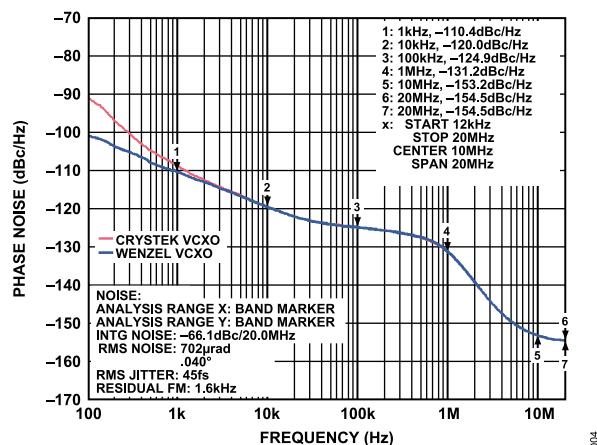
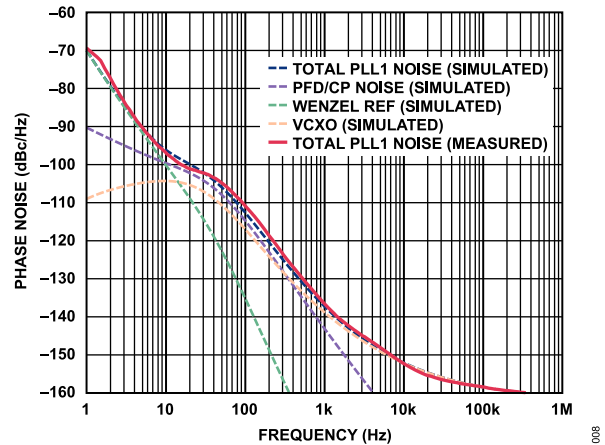
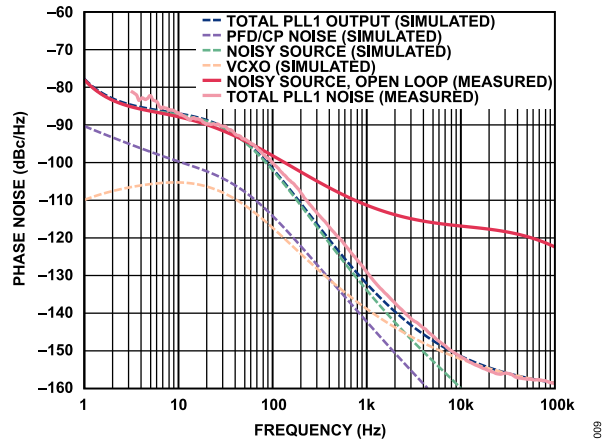


Figure 5. PLL2 Phase Noise vs. Frequency, VCXO Quality at 2457.6 MHz, Wide Loop Bandwidth

Figure 6. Closed-Loop Phase Noise at 122.88 MHz, PLL1 Measurement vs. Simulated, Clean Reference Source, ~ 70 Hz Loop Bandwidth 80° Phase MarginFigure 7. Closed-Loop Phase Noise at 122.88 MHz, PLL1 Measurement vs. Simulated, Noisy Reference Source, ~ 70 Hz Loop Bandwidth, 80° Phase Margin

TYPICAL PERFORMANCE CHARACTERISTICS

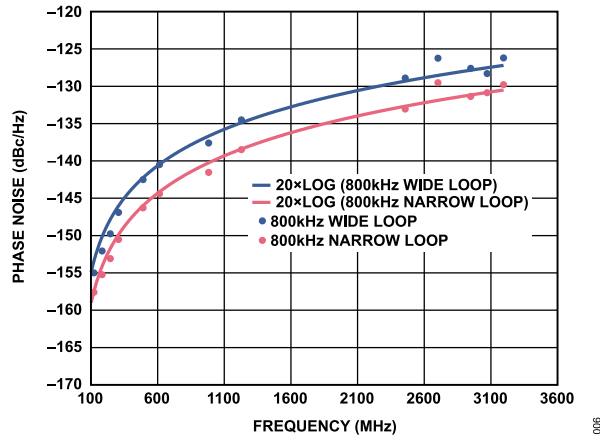


Figure 8. Phase Noise vs. Frequency at Common Output Frequencies

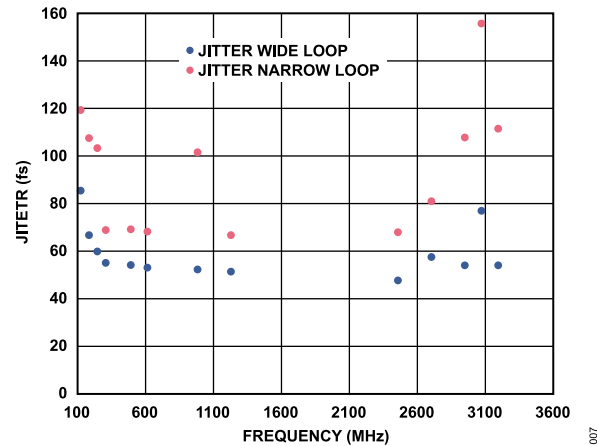


Figure 9. 12 kHz to 20 MHz Jitter vs. Frequency, Wide Loop and Narrow Loop at Common Output Frequencies

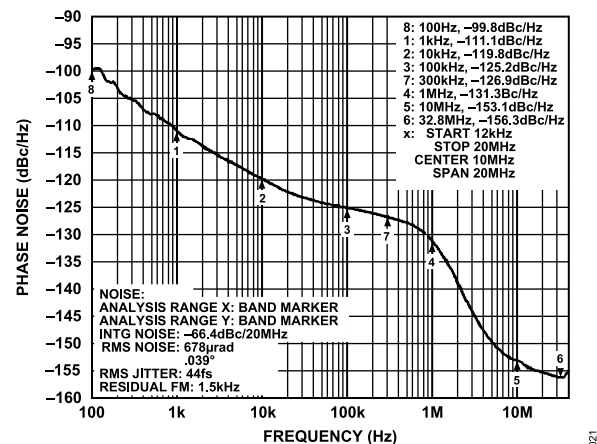


Figure 10. Phase Noise, CLKOUTx/CLKOUTx = 2457.6 MHz, Optimized for Best Integrated Jitter (12 kHz to 20 MHz)

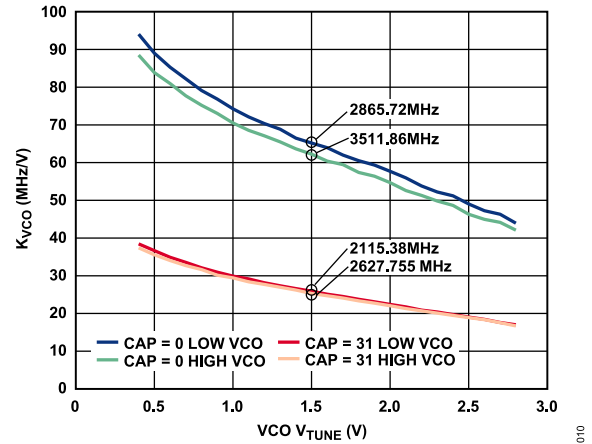
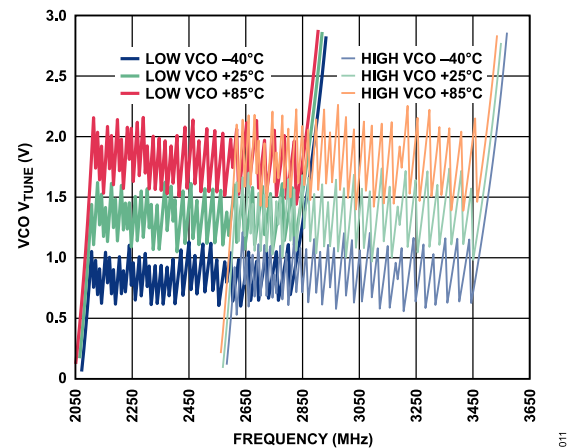
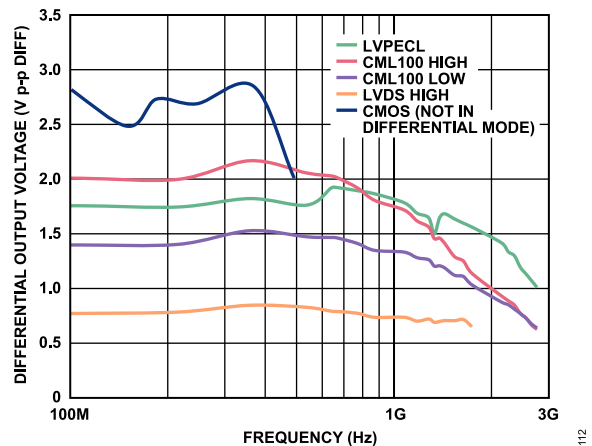
Figure 11. VCO Gain (K_{VCO}) vs. VCO V_{TUNE} Figure 12. VCO V_{TUNE} vs. Frequency

Figure 13. Differential Output Voltage vs. Frequency at Different Modes

TYPICAL PERFORMANCE CHARACTERISTICS

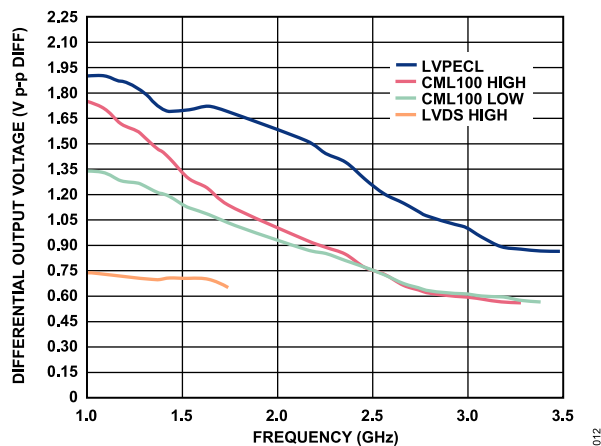


Figure 14. Differential Output Voltage vs. Frequency at Different Modes

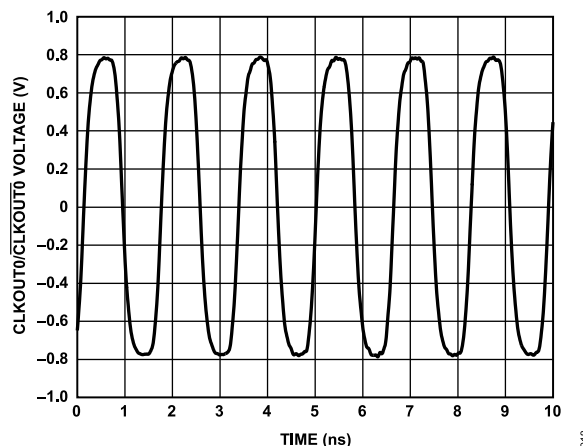


Figure 17. Differential CLKOUT0/CLKOUT0 Voltage at 614.4 MHz, LVPECL

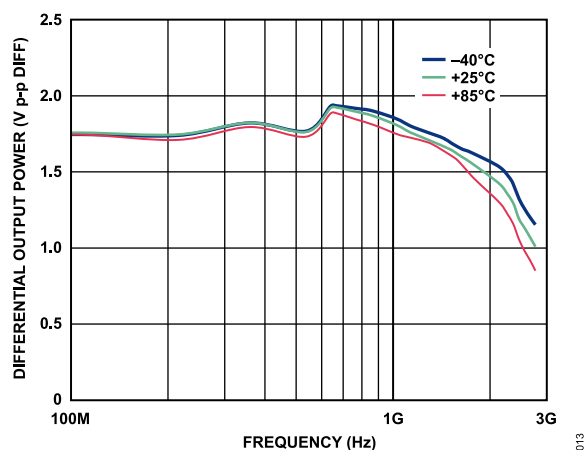


Figure 15. LVPECL Differential Output Voltage vs. Frequency at Different Temperatures

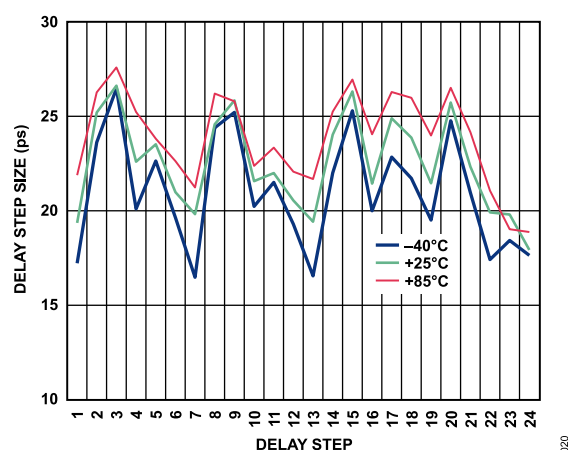


Figure 18. Analog Delay Step Size vs. Delay Step over Temperature, LVPECL at 1474.56 MHz

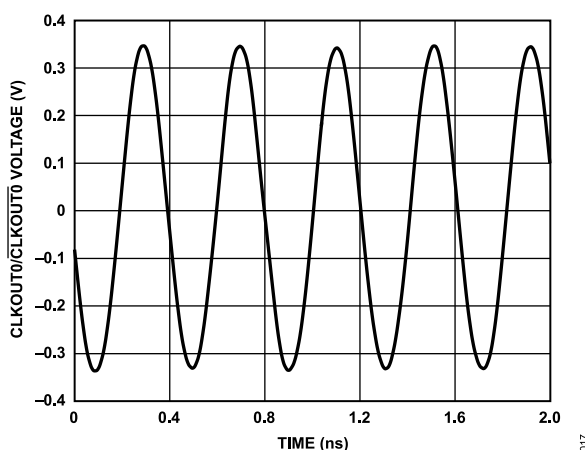


Figure 16. Single Ended CLKOUT0/CLKOUT0 at 2457 MHz, LVPECL

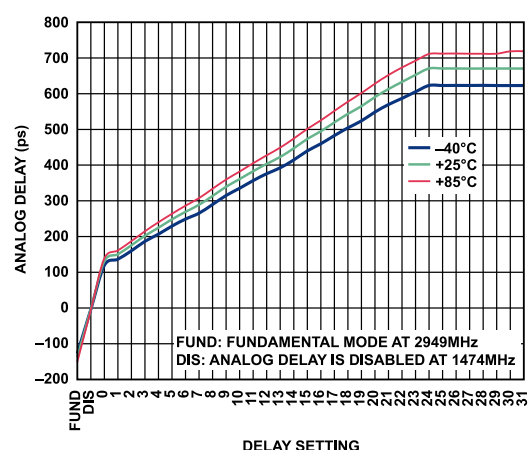


Figure 19. Analog Delay vs. Delay Setting over Temperature, LVPECL at 1474.56 MHz

TYPICAL PERFORMANCE CHARACTERISTICS

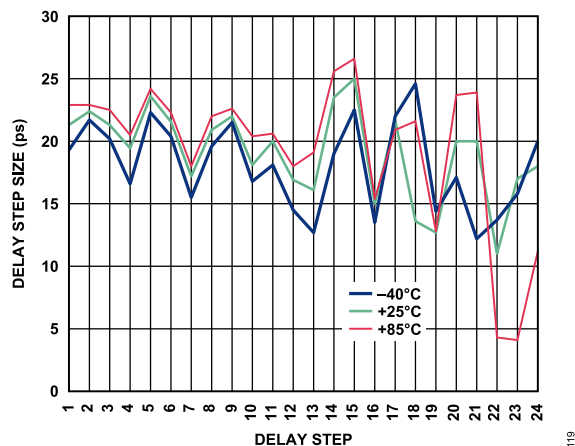


Figure 20. Analog Delay Step Size Vs Delay Step over Temperature, LVPECL at 3072 MHz with Digital Delay = 0

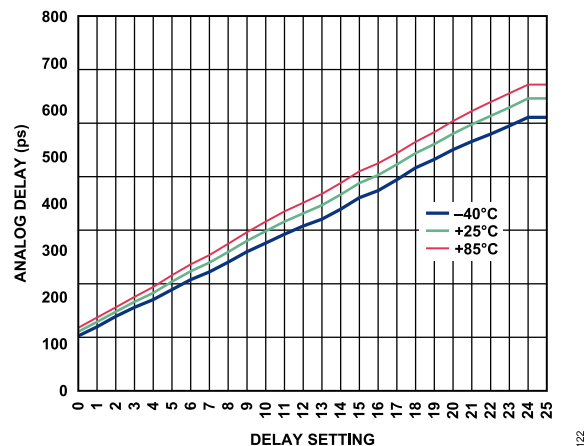


Figure 23. Analog Delay vs. Delay Setting over Temperature, LVPECL at 3072 MHz with Digital Delay = 1

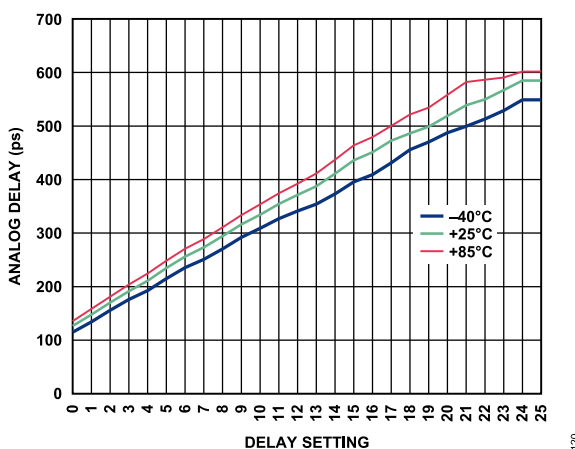


Figure 21. Analog Delay vs. Delay Setting over Temperature, LVPECL at 3072 MHz with Digital Delay = 0

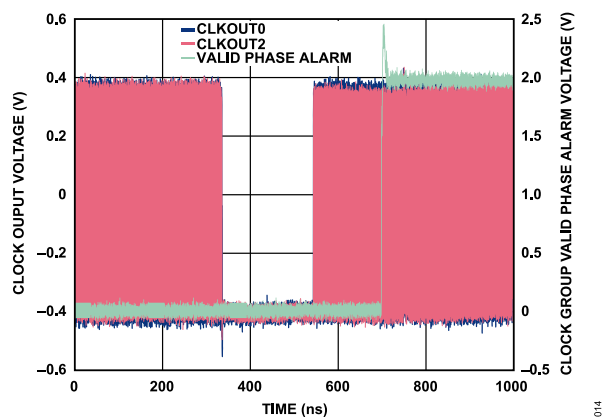


Figure 24. Output Channel Synchronization Before and After Rephase

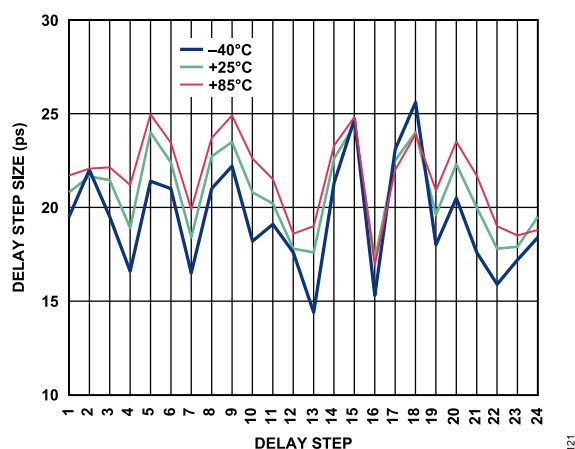


Figure 22. Analog Delay Step Size Vs Delay Step over Temperature, LVPECL at 3072 MHz with Digital Delay = 1

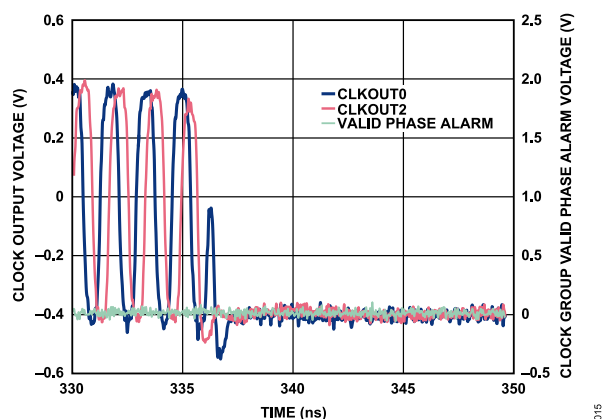


Figure 25. Output Channel Synchronization Before Rephase

TYPICAL PERFORMANCE CHARACTERISTICS

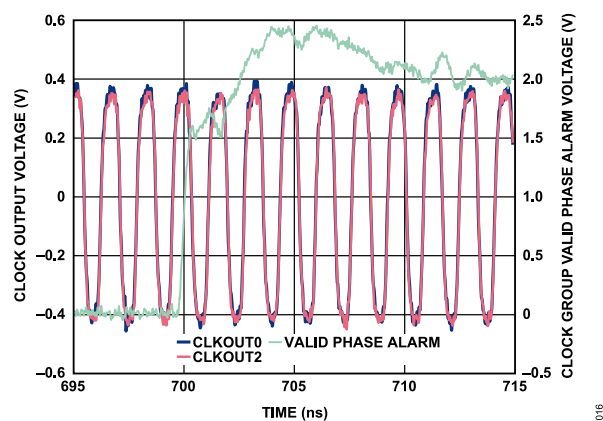


Figure 26. Output Channel Synchronization After Rephase

TYPICAL APPLICATION CIRCUITS

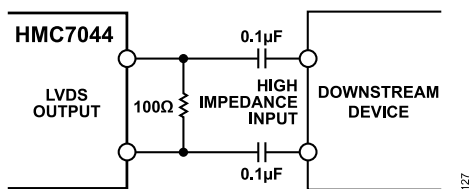


Figure 27. AC-Coupled LVDS Output Driver

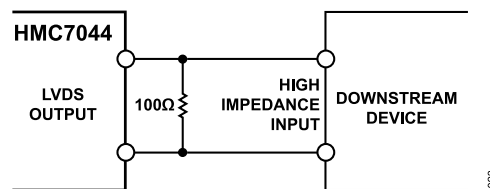


Figure 32. DC-Coupled LVDS Output Driver

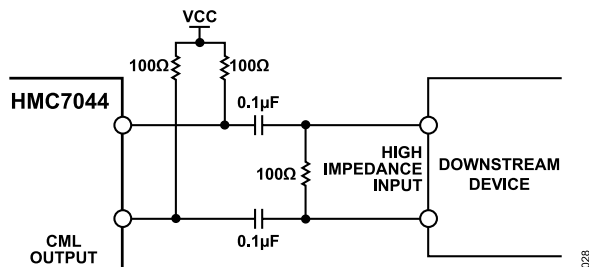


Figure 28. AC-Coupled CML (Configured High-Z) Output Driver

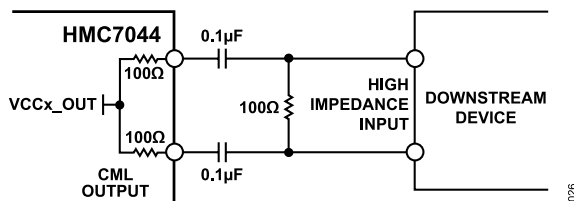


Figure 29. AC-Coupled CML (Internal) Output Driver

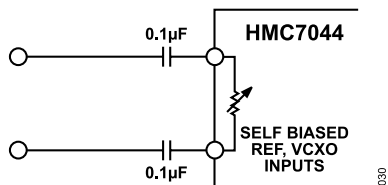


Figure 30. CLKIN0/CLKIN0, CLKIN1/CLKIN1, CLKIN2/CLKIN2, CLKIN3/CLKIN3, and OSCIN/OSCIN Input, Differential Mode

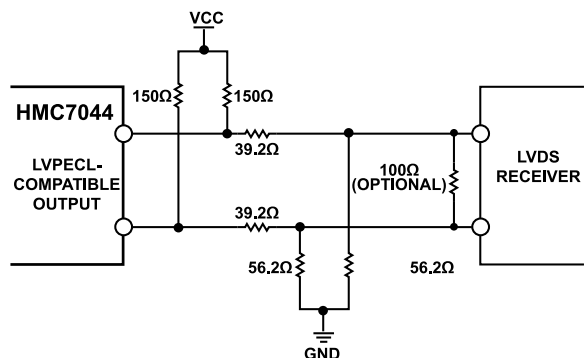


Figure 31. Level Translation for LVDS N-Pulse Operation. Place 100Ω Termination Resistor If Receiver Does Not Have It

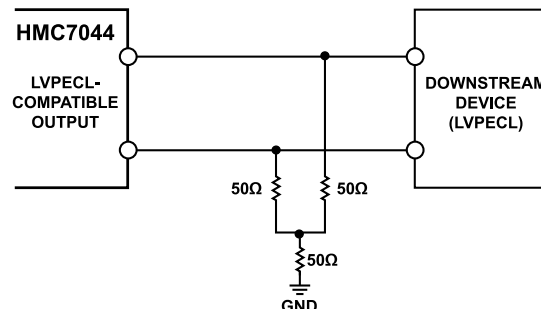


Figure 33. DC-Coupled LVPECL Output Driver

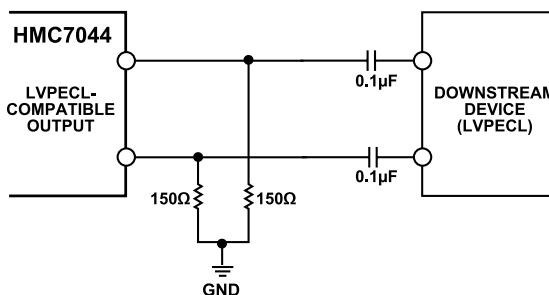


Figure 34. AC-Coupled LVPECL Output Driver

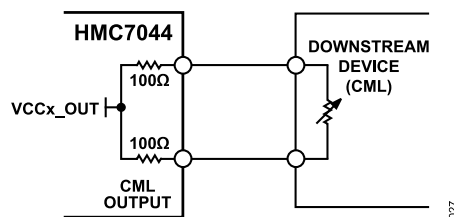


Figure 35. DC-Coupled CML (Internal) Output Driver

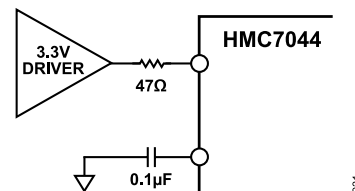


Figure 36. CLKIN0, CLKIN1, CLKIN2, CLKIN3, and OSCIN Input, Single-Ended Mode

TERMINOLOGY

Phase Jitter

An ideal sine wave can be thought of as having a continuous and even progression of phase with time from 0° to 360° for each cycle. Actual signals, however, display a certain amount of variation from ideal phase progression over time. This phenomenon is phase jitter. Although many causes can contribute to phase jitter, one major cause is random noise, which is characterized statistically as being Gaussian (normal) in distribution.

This phase jitter leads to the energy of the sine wave in the frequency domain spreading out, producing a continuous power spectrum. This power spectrum is usually reported as a series of values whose units are dBc/Hz at a given offset in frequency from the sine wave (carrier). The value is a ratio (expressed in decibels) of the power contained within a 1 Hz bandwidth with respect to the power at the carrier frequency. For each measurement, the offset from the carrier frequency is also given.

Phase Noise

It is meaningful to integrate the total power contained within some interval of offset frequencies (for example, 10 kHz to 10 MHz). This is the integrated phase noise over that frequency offset interval and can be readily related to the time jitter due to the phase noise within that offset frequency interval.

Phase noise has a detrimental effect on the performance of ADCs, DACs, and RF mixers. It lowers the achievable dynamic range of the converters and mixers, although they are affected in somewhat different ways.

Time Jitter

Phase noise is a frequency domain phenomenon. In the time domain, the same effect is exhibited as time jitter. When observing a sine wave, the time of successive zero crossings varies. In

a square wave, the time jitter is a displacement of the edges from their ideal (regular) times of occurrence. In both cases, the variations in timing from the ideal are the time jitter. Because these variations are random in nature, the time jitter is specified in seconds root mean square (rms) or 1 sigma of the Gaussian distribution.

Time jitter that occurs on a sampling clock for a DAC or an ADC decreases the signal-to-noise ratio (SNR) and dynamic range of the converter. A sampling clock with the lowest possible jitter provides the highest performance from a given converter.

Additive Phase Noise

Additive phase noise is the amount of phase noise that is attributable to the device or subsystem being measured. The phase noise of any external oscillators or clock sources is subtracted, which makes it possible to predict the degree to which the device impacts the total system phase noise when used with the various oscillators and clock sources, each of which contributes its own phase noise to the total. In many cases, the phase noise of one element dominates the system phase noise. When there are multiple contributors to phase noise, the total is the square root of the sum of squares of the individual contributors.

Additive Time Jitter

Additive time jitter is the amount of time jitter that is attributable to the device or subsystem being measured. The time jitter of any external oscillators or clock sources is subtracted, which makes it possible to predict the degree to which the device impacts the total system time jitter when used with the various oscillators and clock sources, each of which contributes its own time jitter to the total. In many cases, the time jitter of the external oscillators and clock sources dominates the system time jitter.

THEORY OF OPERATION

The HMC7044 is a high performance, dual-loop, integer N jitter attenuator capable of performing frequency translation, reference selection, and generation of ultralow phase noise references for high speed data converters with either parallel or serial (JESD204B and JESD204C type) interfaces. The device is designed to meet the requirements of demanding base station designs, and offers a wide range of clock management and distribution features to simplify baseband and radio card clock tree designs.

The HMC7044 uses a dual-loop architecture, where two integer mode PLLs are connected in series to form a jitter attenuating clock multiplier unit. The high performance dual-loop topology of the HMC7044 enables the wireless/RF system designer to attenuate the incoming jitter of a primary system reference clock (for example, Common Public Radio Interface™ (CPRI) source) and generate low phase noise, high frequency clocks to drive data converter sample clock inputs. The HMC7044 provides 14 low noise and configurable outputs to offer flexibility in interfacing with many different components in an RF transceiver system, such as data converters, local oscillators, transmit/receive modules, FPGAs, and digital front-end (DFE) ASICs.

The first PLL in the HMC7044 is designed for low bandwidth configuration using appropriately selected external loop filter components, and internal charge pump bias settings to achieve less than a few hundred Hz bandwidth, typically. The exact bandwidth roll-off points depend on the frequency spectrum of noise that must be attenuated in the system. The first PLL locks an external VCXO and provides the clock holdover functions and the reference frequency to the high performance second PLL loop. The combination of the loops provides an excellent clock generation unit with the capability to attenuate incoming reference clock jitter. The second PLL loop features two overlapping on-chip VCOs that are SPI selectable with center frequencies at 2.5 GHz and 3 GHz, respectively. Both VCOs are designed to have wide tuning ranges for broad output frequency coverage. The desired output frequency is set by the chosen VCXO frequency, VCO core (higher or lower frequency core), and the programmed second PLL feedback divider and output channel divider values.

The HMC7044 generates up to seven DCLK and SYSREF clock pairs per the JESD204B and JESD204C interface requirements. The system designer can generate a lower number of DCLK and SYSREF pairs, and configure the remaining output signal paths as desired, either as DCLKs or additional SYSREFs or other reference clocks with independent phase and frequency adjustment. Frequency adjustment can be accomplished by selecting the appropriate output divider values. One of the unique features of the HMC7044 is the independent flexible phase management of each of the 14 channels. Using a combination of divider slip-based, digital/coarse, and analog/fine delay adjustments, each channel can be programmed to have a different phase offset. The phase adjustment capability allows the designer to offset board flight time delay variations, data converter sample window matching, and meet JESD204B and JESD204C synchronization challenges. The output signal path design of the HMC7044 is implemented

to ensure both linear phase adjustment steps and minimal noise perturbation when phase adjustment circuits are turned on.

One of the key challenges in JESD204B and JES204C system design is ensuring the synchronization of data converter frame alignment across the system, from the FPGA or DFE to ADCs and DACs through a large clock tree that can comprise multiple clock generation and distribution ICs. The HMC7044 is specifically designed to offer features to address this challenge. Using the SYSREF valid interrupt feature, the wait time latency can be reduced in the FPGAs. The HMC7044 raises this flag through its GPO port when all counters are set and outputs are at the desired phases. Additionally, an external reference-based synchronization feature (SYNC via PLL2 or RF SYNC only in fanout mode) synchronizes multiple devices, that is, it ensures that all clock outputs start with same rising edge. This operation is achieved by rephasing the SYSREF control unit deterministically, and then restarting the output dividers with this new desired phase.

Offering excellent crosstalk, frequency isolation, and spurious performance, the device generates independent frequencies in both single-ended and differential formats. The four input reference options allow up to three backup frequency sources, with hitless switching and holdover capabilities, supporting system redundancy and uninterrupted operation on reference data and clock failures. The device also features dedicated oscillator fanout mode for best clock isolation, which generates multiple copies of the VCXO clock to be distributed across the board with excellent frequency isolation.

Both the DCLK and SYSREF clock outputs can be configured to support different signaling standards, including CML, LVDS, LVPECL, and LVCMOS, and different bias conditions to offset varying board insertion losses. The outputs can also be programmed for ac or dc coupling and 50 Ω or 100 Ω internal and external termination options.

The HMC7044 is programmed via a 3-wire serial port interface (SPI) and powers up with a default configuration that generates valid output frequencies within the VCO tuning ranges regardless of whether a reference clock exists.

The HMC7044 is offered in a 68-lead, 10 mm \times 10 mm, LFCSP package with the exposed pad to ground.

Note that, throughout this data sheet, multifunction pins, such as CLKIN0/RFSYNCIN, are referred to either by the entire pin name or by a single function of the pin, for example, CLKIN0, when only that function is relevant.

THEORY OF OPERATION

DETAILED BLOCK DIAGRAM

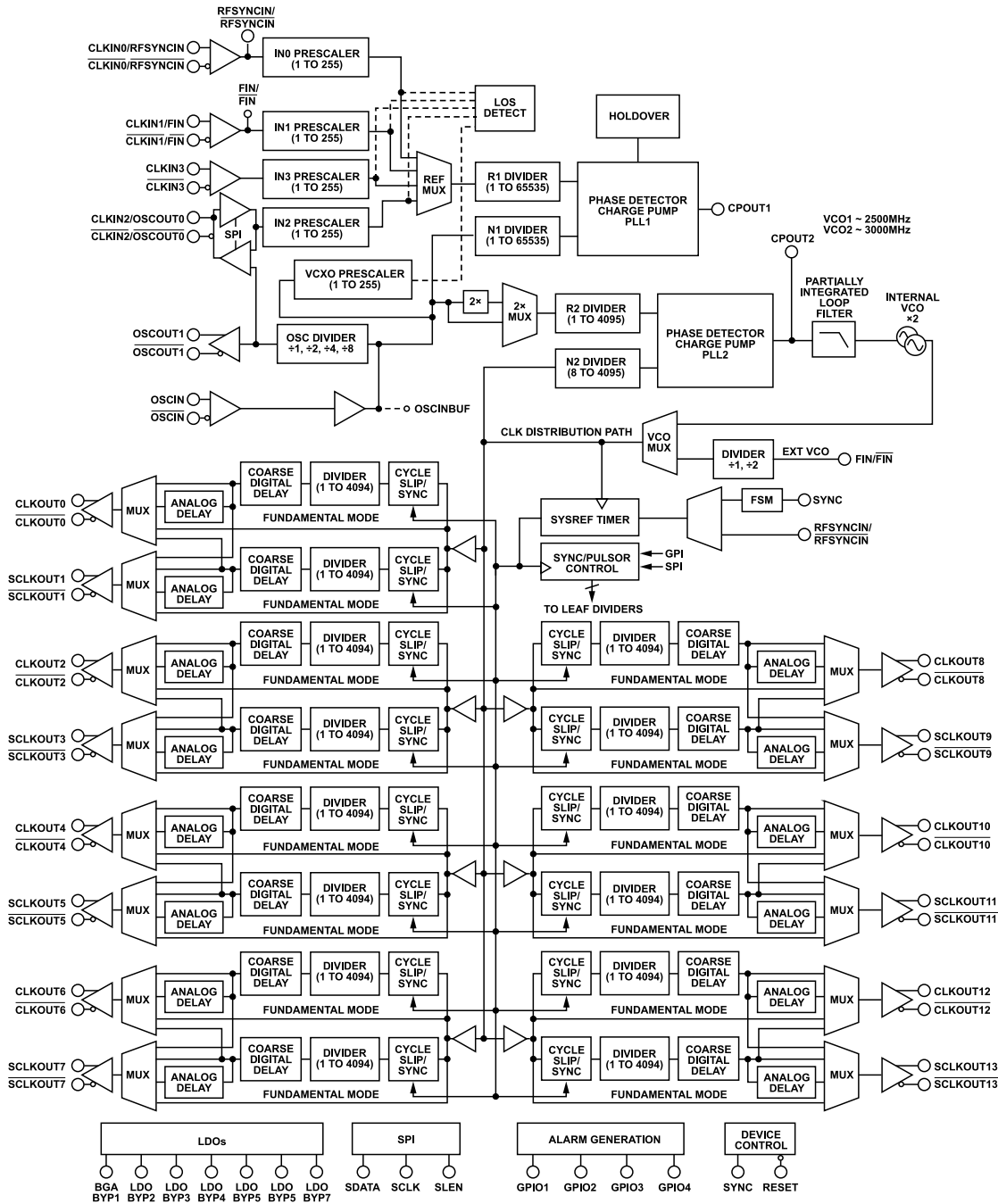


Figure 37. Top Level Diagram

DUAL PLL OVERVIEW

The HMC7044 uses a cascade of two PLLs, referred to as a dual loop topology. The term dual loop sometimes refers to other architectures as well; therefore, always refer to the block diagram shown in Figure 37 to remove any ambiguity. In this architecture, the first PLL (PLL1) normally operates as a jitter attenuator. PLL1 locks a clean local VCXO to a relatively noisy reference using a

very narrow loop bandwidth. The loop bandwidth preserves the average frequency of the reference signal (which is normally correct), while rejecting the majority of its noise. The second PLL takes this low-noise VCXO and multiplies it up to the VCO frequency (in the 2 GHz to 3 GHz range) with very little additive noise. The architecture provides the benefits of an output frequency locked to an input reference signal, while being insensitive to its noise profile.

THEORY OF OPERATION

In ICs such as the HMC7044, the VCO is then connected to an array of output channels, each with an optional RF divider and phase control. The key feature that distinguishes an IC with JESD204B and JES204C support is the ability to ensure that all of the outputs with their associated dividers have a user-defined phase relationship each and every time, regardless of process, voltage, or temperature. This ability is necessary to support the JESD204B and JESD204C SERDES standard for data converters, but it is also an immensely useful feature in other applications as well, in all forms of arrayed systems, and many test and measurement scenarios.

COMPONENT BLOCKS—INPUT PLL (PLL1)

PLL1 General Description (Jitter Attenuator)

A variety of local clocks, particularly in synchronous networks, derive their timing from a remote node in the network. These reference signals can arrive via a GPS or clock data recovery (CDR) receiver, or from a variety of other sources. Often, these derived references are relatively poor quality, in terms of spurious content, noise, and reliability.

The function of PLL1 is to lock a clean VCXO to the average frequency of one of these references and feed it to PLL2 to generate a high quality clock for local use.

In addition, PLL1 monitors its active reference for failure and smoothly takes appropriate action, switching to a redundant reference or going into holdover as appropriate. Figure 38 shows the architecture of PLL1 with a typical frequency configuration.

Jitter Attenuation

For the purpose of jitter attenuation, PLL1 consists of all the usual components in a PLL: a phase/frequency detector (PFD1), charge

pump (CP1), reference divider (R1), and feedback divider (N1). The loop filter is external to provide maximum flexibility, and the loop bandwidth (BW) is normally configured very narrow (20 Hz to 500 Hz) to filter any jitter and spurious tones coming in from relatively poor references.

The noise profile of PLL1 is typically dependent on the loop bandwidth, input reference noise, and the VCXO characteristic. The inherent noise sources of PLL1 (the PFD, dividers, and charge pump) are not normally observable in an application, and are significantly more relaxed compared with PLL2.

Note that the loop filter components on the board are typically configured to produce a certain loop bandwidth, given a fixed PFD rate, charge pump current, and VCXO characteristic. Adjusting any of these parameters from their nominal positions affects the loop dynamics, which can be to the advantage of the user (for example, to scale loop BW with charge pump current), but it must not be performed without an analysis of the stability of the loop. Analog Devices, Inc., provides ADISimCLK software tools to design the loop filter and model the effects of any change in parameters. Visit analog.com/ADISimCLK for the latest information.

The lock time of PLL1 typically takes the longest duration in the clock network, and, aside from any nonlinear slewing, takes approximately $5/\text{PLL1_BW}$ (for example, 5 ms for a 1 kHz loop BW). Fortunately, there are no requirements that PLL1 must be locked before proceeding with PLL2, output calibration, and phasing, which normally allows system configuration to continue in parallel while PLL1 is settling.

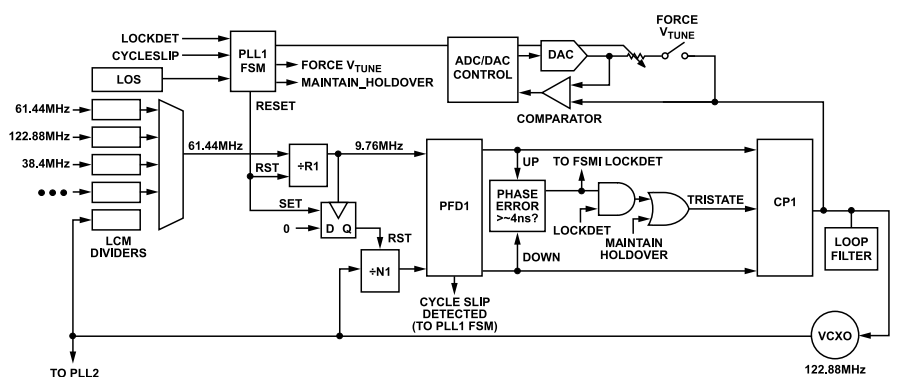


Figure 38. PLL1 Architecture with a Typical Frequency Configuration

THEORY OF OPERATION

Lock Detect

The locks detect circuit in both PLL1 and PLL2 function the same way. They count the number of consecutive clock cycles in which the phase error at the PFD is below a threshold. Any phase error above this threshold resets the counter, and the count is restarted. When the count reaches its programmed limit, the lock detect signal is issued and the clock of the counter is gated off to reduce power/coupling until a large phase error restarts the process.

Although the PLL2 loop bandwidth is relatively well defined, the PLL1 loop bandwidth can vary widely in any given application. The SPI word, PLL1 Lock Detect Timer[4:0] in Register 0x0028, configures the PLL1 lock detect timer and looks for $2^{\text{PLL1 Lock Detect Timer[4:0]}}$ consecutive LCM clock cycles with a phase-error $< \sim 4$ ns to issue the lock detect. Because the loop bandwidth of PLL1 can vary drastically depending on the application, the user must set up the threshold such that $2^{\text{PLL1 Lock Detect Timer[4:0]}}$ LCM periods is on the order of $2\times$ to $4\times$ the loop time constant. For example, for $f_{\text{LCM}} = 61.44$ MHz, and a loop bandwidth of 200 Hz, set PLL1 Lock Detect Timer[4:0] = 19 or 20. If the value is set much higher, the lock detect circuit takes an unnecessary length of time to indicate lock after the phases stabilize. If the value is set much lower (for example, much less than a loop time constant), it can improperly indicate lock during acquisition, which can cause the PLL1 finite state machine (FSM) to improperly fall in and out of holdover mode.

Holdover/Reference Switching Overview

When switching between redundant references, or when all references are gone and the PLL1 is left open loop, there are often requirements to prevent frequency deviations that can cause downstream circuits and traffic links to overrun FIFOs and/or lose lock themselves.

PLL1 can operate in manual or automode (via the automode reference switching bit). In manual mode, the user selects the active reference using Manual Mode Reference Switching[1:0] in Register 0x0029 and determines whether to go into holdover (via the force holdover bit). In automode, the PLL1 FSM uses the loss of signal (LOS) information, phase error data, lock detect, and configuration data from the SPI to determine how to handle reference interruptions. In either mode, all status indicators are available, but PLL1 only takes evasive action in automode. Figure 39 shows a simplified state diagram of the PLL1 FSM.

During reset, PLL1 is held in the initialization (INIT) state. When reset is deasserted, during the preload state, the enabled reference paths, the reference priority table, and LOS indicators are examined to select the best reference, and, on the next cycle, it attempts to lock. After the requisite number of counts has elapsed with low phase error, lock detect is asserted and PLL1 transitions to the locked state. When PLL1 is locked, a loss of lock, LOS on the active reference, or a reference switch event initiated by a priority clash transitions the FSM to enter holdover, where it tristates the CP and potentially forces V_{TUNE} with the holdover DAC. When a

stable clock is available and other optional conditions are met, the FSM exits holdover. Exiting holdover is handled in one of a few different ways, designed to minimize phase/frequency hits during the transition. Figure 39 shows a simplification of the PLL1 FSM. In the actual implementation, the holdover state is broken into a number of subsections corresponding to holdover entry, stable holdover conditions, and holdover exit. The state of the PLL1 FSM is always available for a read via the SPI (PLL1 FSM State[2:0] bits in Register 0x0082).

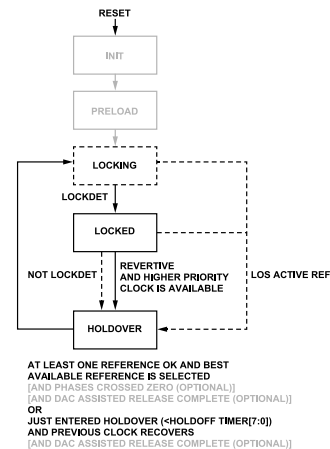


Figure 39. PLL1 FSM Simplified State Diagram—
Autorevertive Reference Switching = 1

PLL1 Reference Inputs

PLL1 accepts up to four candidate references on CLKIN3/CLKIN3̄ to CLKIN0/CLKIN0̄. If all references appear valid, according to the LOS, PLL1 uses a reference priority table to select the best candidate. Using the PLL1 reference priority control bits, program the highest priority clock (CLKIN0/CLKIN0̄, CLKIN1/CLKIN1̄, CLKIN2/CLKIN2̄, or CLKIN3/CLKIN3̄), and then second priority clock, and so on. It is not necessary to include unused reference inputs in the reference priority table. Instead, specify the same useful clock in multiple positions. In automode, reference switching occurs in the preload state (see Figure 39) as PLL1 exits reset, or while PLL1 is in the holdover state.

The reference clock input pins (Pin 36, Pin 37, Pin 39, Pin 40, Pin 42, and Pin 43) have dual functions; therefore, SPI configuration is important for proper functionality. See the [PLL1 Programming Considerations](#) section for more information about the relevant control bits, and the [Reference Buffer Details](#) section for interface recommendations.

When a reference fails, the sourcing circuit recognizes a fault and disables either the clock or the buffer driving the signal to the HMC7044. For this reason, hysteresis in the input buffers prevents internal toggling for signal swings $< \sim 75$ mV p-p differential, which allows further elements in the PLL1 architecture to cleanly recognize the interruption and prevent unwanted transients in the frequency.

THEORY OF OPERATION

PLL1 LOS Detection

The HMC7044 checks the validity of a reference by comparing its approximate frequency vs. the VCXO. The HMC7044 supports references at different frequencies. The first step is to divide the available references and the VCXO to the lowest common multiple frequency (f_{LCM}). These divider settings are available via the SPI control bits (CLKINx/CLKINx Input Prescaler[7:0] and OSCIN/OSCIN Input Prescaler[7:0]). In the example shown in [Figure 38](#), $f_{LCM} = 61.44$ MHz. The VCXO derived clock at f_{LCM} is the main clock to the PLL1 FSM controlling the FSM, lock detect timer, and ADC/DAC filtering and holdover circuits. Although not required, using the VCXO clock allows the LOS detection and PLL1 FSM to operate at a higher rate than the PFD, allowing it to recognize a reference failure early and enter holdover, sometimes before a failing reference that has started to drift in either phase or frequency (or both) can influence the PFD or CP.

The dividers in the LOS block, and to some extent, R1, pose a few challenges. The input frequencies are up to 800 MHz, with a wide divider range. Furthermore, they are designed to tolerate glitchy clocks without catastrophic results, because a reset phase is not always available after an issue is detected.

When all the references are divided to the same frequency, they are compared relative to the VCXO derived path, and thus each other. This comparison is performed by a circuit that looks for three edges of a clock within one period of the other. If it appears that a reference signal is too slow, its LOS flag is asserted and, in automode, PLL1 uses this information to disqualify and/or abandon a reference. Conversely, if it appears that the VCXO is too slow according to any of the active references, a warning is generated (available as one of the configurable options for the GPO, or readable on the SPI) but no automated action occurs.

The HMC7044 monitors reference signals for three edges of a clock within one period of the other, instead of the more intuitive two edges, to avoid false LOS flags as clocks that are slightly out of frequency cross each other in phase in the presence of interference, noise, and circuit offsets. The result is that the LOS triggers when the failing reference clock frequency is approximately an octave from the intended frequency.

After a reference signal returns and its frequency is within an octave of the VCXO, two to three cycles of the LOS validation timer must expire before the LOS flag is deasserted and the reference is considered for potential use. The LOS validation timer is programmable between 0 LCM cycles (no hysteresis), and 64 LCM cycles via LOS Validation Timer[2:0] in Register 0x0015, Bits[2:0].

PLL1 Holdover Entry Shortcut

When a reference fails, the LOS circuit takes a number of LCM clock cycles to recognize the problem and to request the PLL1 FSM enter holdover and tristate the CP. By that time, if one of the missing edges is needed to trigger the R divider output, the PFD and CP have already saturated, pulling current out of the loop

filter for these cycles, and disturbing the holdover frequency. The probability of this happening decreases as the PFD rate decreases relative to f_{LCM} , but it is not eliminated. The HMC7044 includes a unique feature to prevent this type of frequency runaway.

A sensor watches the up/down pulses from the PFD (see [Figure 37](#)). When locked, the pulse width is small, based on any small signal error, PFD/CP offset, and the reset delay of the PFD. If the device is in the locked state and has a phase error that is larger than expected (~4 ns), it is a sign that the reference has failed, and the device immediately tristates the pump, reducing the amount of time charge can be extracted from the loop from about five LCM cycles (162 ns at 30.72 MHz) to <4 ns. This error indication also invalidates the lock detect. When the FSM acknowledges the issue, it holds the CP in tristate. When using the optional DAC-based holdover, the FSM instructs the ADC/DAC that is tracking the V_{TUNE} voltage to switch from sense mode to force mode, holding it steady to within 1 LSB (about 20 mV or 0.4 ppm) until the HMC7044 senses a stable reference and transitions out of holdover.

PLL1 Holdover Steady State

When in the holdover state, the user has the following two options:

- Tristate the CP
- Tristate the CP and engage the holdover DAC

When in tristate mode, the HMC7044 has a very high impedance charge pump output (~10 GΩ). This output is normally an insignificant contributor to PLL1 V_{TUNE} leakage, which is determined primarily by the on-board loop filter components and the VCXO tuning port. This mode allows the tuning voltage to maintain itself for significant periods while in holdover.

To accommodate indefinite periods in holdover, or to ensure V_{TUNE} is driven and not susceptible to drift, the second option (set via the holdover uses DAC bit in Register 0x0029, Bit 2) forces the V_{TUNE} voltage to its time averaged value, obtained by low-pass filtering the ADC value while the PLL is reporting lock. The holdover sensing ADC and the driving DAC are seven bits each, and have an LSB of approximately 19 mV.

PLL1 Holdover Exit

The transition out of holdover can happen in three ways and is controlled by the Holdover Exit Criteria[1:0] bits and the Holdover Exit Action[1:0] bits in Register 0x0016 (see the [Control Register Map Bit Descriptions](#) section for details), which describes the steps that the FSM takes as the HMC7044 exits holdover and acquires lock.

The recommended methods are as follows:

- Wait for zero phase error (no divider reset): wait for LOS = 0 and low phase error at PFD (Holdover Exit Criteria[1:0] = 1, Holdover Exit Action[1:0] = 1)

THEORY OF OPERATION

- ▶ Resetting the dividers: wait for LOS = 0 and reset the R1/N2 dividers (Holdover Exit Criteria[1:0] = 0, Holdover Exit Action[1:0] = 0)
- ▶ DAC assisted release: wait for LOS = 0, reset R1/N2, and configure for DAC assisted release (Holdover Exit Criteria[1:0] = 0, Holdover Exit Action[1:0] = 3)

Wait for Zero Phase Error

While the CP is still in tristate, the FSM monitors the PDF for a cycle slip indication as the candidate reference and VCXO signal cross each other. The crossing of the reference and VCXO phases eventually occurs but can take a long time, as determined by the inherent frequency error due to an imperfect holdover. Just after a cycle slip event, the phase error at the PFD is at its minimum value, and there is minimal glitch as the PLL reacquires. Figure 40 shows an example where the reference is removed and PLL1 goes into tristate-based holdover. After approximately 7 sec, the reference is restored and, about a second later, the phases cross and the PLL reacquires, all with less than 0.15 ppm of deviation from the original frequency value.

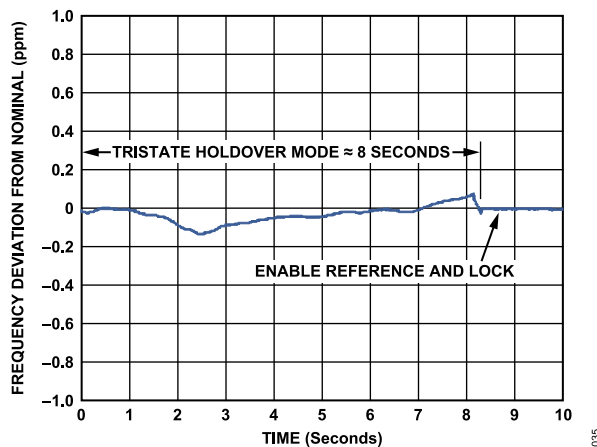


Figure 40. Frequency Deviation from Nominal vs. Time of Tristate Holdover Entry and Exit When the Phases Cross Zero

This first method of uncontrolled release suffers from an indeterminate amount of time for the phases to cross and exit holdover. However, if it takes 1 sec for the phases to cross, the frequencies are off by only 1 Hz. If it takes 10 sec to cross, the error is 0.1 Hz. If the error is so low that it takes a long time to exit holdover, the device is effectively frequency locked. In some applications, being open-loop for this long of a duration can be acceptable, considering the very small frequency errors. Although this method of holdover exit is very smooth, it can take a very long time to occur.

Resetting the Dividers

If using tristate-based holdover, the second holdover exit method is recommended. When a reference appears available (LOS = 0), the FSM resets the R and N dividers and allows them to restart immediately. This approach limits the maximum phase error coming

out of holdover to two VCXO cycles (about 8 ns for typical VCXO frequencies). There is no need to wait an undetermined amount of time (as in the first method of uncontrolled release) to initiate the switch.

DAC Assisted Release

If using DAC-based holdover, the DAC and CP can set V_{TUNE} concurrently as the device exits holdover. With the DAC output impedance at a relatively low setting (for example, 5 Ω), the device resets the dividers as in the second method, and then the CP attempts to influence V_{TUNE} . The CP fails, with the DAC sinking the current it is trying to inject into the V_{TUNE} node. Gradually, the device increases the output impedance of the DAC, and the CP gains more influence to manipulate V_{TUNE} , pulling the phases into alignment. Using this DAC assisted CP release method limits the holdover exit transients to within ~1 ppm.

Figure 41 to Figure 43 compare the holdover release methods: resetting the dividers vs. DAC assisted release, and uncontrolled release (which starts with a phase error of up to one PFD period) as the device exits holdover and reacquires to a reference signal.

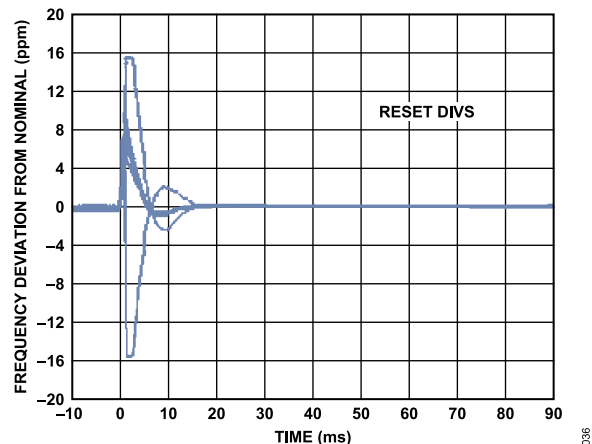


Figure 41. Resetting the Dividers

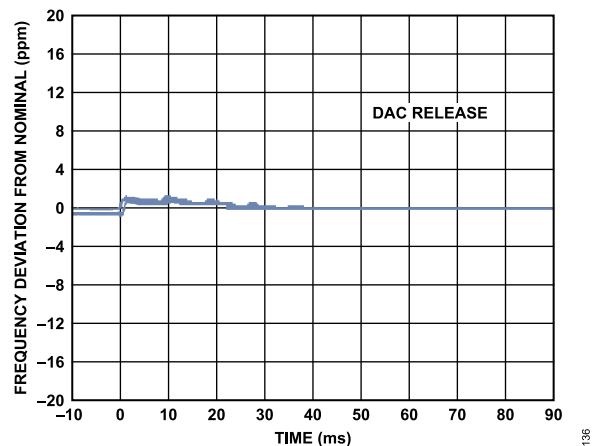


Figure 42. DAC Assisted Release

THEORY OF OPERATION

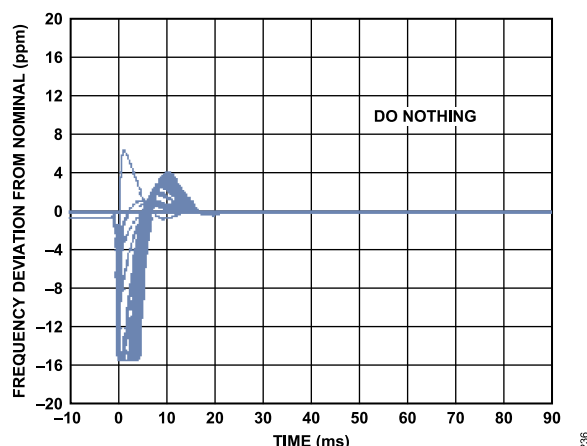


Figure 43. Wait for Zero Phase Error (No Divider Reset)

PLL1 Programming Considerations

Configuring Reference Inputs for PLL1 vs. Other Uses

To use the four reference clocks for PLL1, the input buffer must be enabled and selected as a relevant path for PLL1.

Table 14. Input Buffer and Reference Path Settings

| Bit Name | Description |
|---------------------------------|--|
| Buffer Enable | Enable the input buffer (where x = 0, 1, 2, 3, or V for VCXO) via Register 0x000A to Register 0x000E |
| PLL1 Reference Path Enable[3:0] | Select one of four available reference paths for PLL1 |

Because the CLKIN0/RFSYNCIN, $\overline{\text{CLKIN0}}/\overline{\text{RFSYNCIN}}$, CLKIN1/FIN, and $\overline{\text{CLKIN1}}/\overline{\text{FIN}}$ pins can be configured for output network purposes, and the CLKIN2/OSCOUT0 and $\overline{\text{CLKIN2}}/\overline{\text{OSCOUT0}}$ pins can function as oscillator outputs, the SPI bits in Table 15 must be configured accordingly.

Table 15. Reference Clock Input Bit Settings

| Bit Name | Description |
|---|--|
| CLKIN0/ $\overline{\text{CLKIN0}}$ In RF SYNC Input Mode | 0 = CLKIN0/ $\overline{\text{CLKIN0}}$ does not function as an RF sync input |
| CLKIN1/ $\overline{\text{CLKIN1}}$ in External VCO Input Mode | 0 = CLKIN1/ $\overline{\text{CLKIN1}}$ does not function as external VCO (FIN/ $\overline{\text{FIN}}$) |
| OSCOUT0/ $\overline{\text{OSCOUT0}}$ Driver Enable | 1 = OSCOUT0/ $\overline{\text{OSCOUT0}}$ buffer does not drive CLKIN2/ $\overline{\text{CLKIN2}}$ pins |

Choosing f_{PD1}

Although PLL1 supports a wide range of PFD frequencies, there are trade-offs with setting the frequency too high or too low. A few MHz is high enough to allow the comparison frequency to stay at an offset outside of the PLL2 loop bandwidth and thus suppress any coupling that manages to bypass the PLL1 loop filter.

Choosing f_{LCM}

At a minimum, f_{LCM} must be a common submultiple of all available references. Typical frequencies include 122.88 MHz, 61.44 MHz, 38.4 MHz, 30.72 MHz, 3.84 MHz, and 1.92 MHz. This f_{LCM} clock is the main clock for the PLL1 digital logic. This clock rate also scales the PLL1 lock detect timer speeds/thresholds, holdover ADC averaging times, and LOS assertion and revalidation delays. Higher frequencies slightly improve the response times to reference interruptions, whereas lower frequencies can slightly reduce current consumption of the device by up to ~10 mA. Values in the 30 MHz to 70 MHz range are recommended.

Program the PLL1 lock detect timer threshold based on the PLL1 loop bandwidth and f_{LCM} of the user.

There are reserved registers, as described in the [Control Register Map Bit Descriptions](#) section, that must be reprogrammed from their default values. For example, Register 0x00A5 must be set from 0x00 to 0x06.

COMPONENT BLOCKS—OUTPUT PLL (PLL2)

PLL2 Overview

PLL2 is a very low noise integer PLL designed to multiply the frequency from the VCXO to the VCO. It typically operates with a loop BW of 10 kHz to 700 kHz. Use bandwidths on the lower end of the range to preserve the inherent VCO phase noise at 800 kHz offset (useful in GSM-based systems), where bandwidths on the upper end can provide the best integrated phase noise/jitter values.

Internally, PLL2 has a number of features that allow it to efficiently achieve a Banerjee floor FOM of -232 dBc and a flicker FOM of -266 dBc. The combination of the on-board VCO, an internal VCXO doubler, a low N2 minimum divide ratio, and the ability to clock the PFD at up to 250 MHz results in an integrated jitter (at 12 kHz to 20 MHz) of 44.0 fs typical.

PLL2 has the following features:

- ▶ Lock detect
- ▶ Frequency doubler
- ▶ Partially integrated loop filter
- ▶ VCO selection, external VCO use
- ▶ VCO calibration
- ▶ Multichip synchronization via PLL2

Lock Detect

The lock detect function of PLL2 behaves the same way as in PLL1. It counts the number of consecutive PFD clock cycles that occur with a low phase error. When it reaches a count of 512, it declares lock. The threshold of 512 is adjustable, but because the PLL2 loop bandwidth does not vary as much as PLL1, it is expected that the user never needs to change this threshold.

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Frequency Doubler

The user can engage a frequency doubler after the VCXO buffer and before the reference divider (see Figure 37). The frequency doubler assumes an approximate 50% input duty cycle, where any duty cycle distortion can result in a spur, at $f_{PD2}/2$, suppressed by the PLL2 loop filter. Use of the frequency doubler is highly recommended to achieve the best spectral performance, provided the PFD is kept under its 250 MHz frequency limit.

Partially Integrated Loop Filter

Although the large components for the PLL2 loop filter are off chip, there is a small on-chip resistor/capacitor (RC) section formed with $R = 80\ \Omega$ and $C = 4.7\ \text{pF}$ in series. This RC section forms a higher order pole at $\sim 420\ \text{MHz}$. For practical conditions, this filter segment does not affect the stability of the loop.

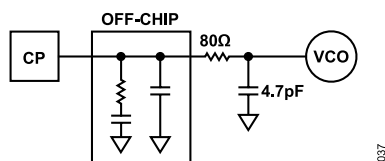


Figure 44. On-Chip RC Circuit

Figure 45 shows the VCO input network. Depending on the frequency band of interest (2.5 GHz or 3.0 GHz), the user must specify which VCO to enable via the VCO Selection[1:0] SPI word. To use the CLKIN1/FIN pin as an external VCO signal, program this word to 0, and set the CLKIN1/CLKIN1 in external VCO input mode bit. When it is intended to use external VCO, set VCO selection first, then set CLKIN1/CLKIN1 to ensure bias of the internal VCOs is disconnected.

VCO Selection, External VCO Use

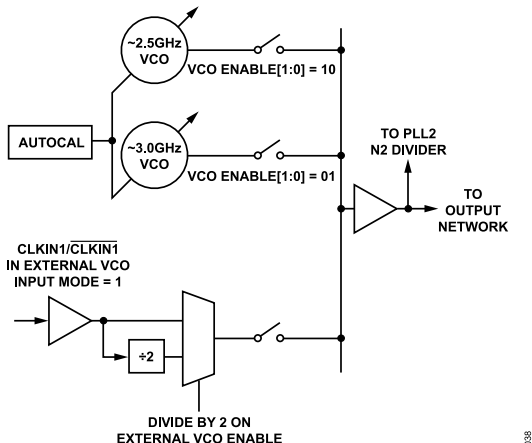


Figure 45. VCO Input Network

VCO Calibration

The on-board VCOs contain an AGC loop that regulates the core voltage of the oscillator to achieve the desired swing and thus the trade-off between phase-noise and power consumption. This AGC loop uses large external bypass capacitors to eliminate the noise impact of the AGC loop, and therefore takes time to settle after power-up, sleep, or after changing the VCO Selection[1:0] setting. With the 100 nF/1 μF configuration, settling time takes approximately 10 ms (typical).

Each of the VCOs in the HMC7044 has 32 frequency bands. Normally, three or more subbands can synthesize any particular frequency, and an on-board autotune algorithm selects the solution that provides tuning margin for temperature fluctuations. Temperature compensation is applied inside to ensure that the device can be calibrated at any frequency and maintain lock as the frequency is carried to any other frequency in the operating range.

The autotune is triggered by toggling the restart dividers/FSMs bit in Register 0x0001, Bit 1, after R2 and N2 are programmed, the VCXO is applied, and the VCO peak detector loop has settled.

When the VCXO is applied to the system and the R2 and N2 divide ratios are programmed, the autotune algorithm has the information needed to find the appropriate band of the VCO.

Manual VCO Calibration

As it is stated in the VCO Calibration section, the HMC7044 has 32 overlapping subbands (capacitor banks) for each core to cover a wide range of frequencies. Autocalibration selects the appropriate subband for the related VCO frequency.

Output phase of the VCO can vary between the capacitor banks. In some applications, it is required to have a constant phase difference between multiple parallel working HMC7044 devices. This constant phase difference can be calibrated out at the design stage for a given capacitor selection. However, autocalibration can pick different capacitor bank in another autocalibration. This results with a different phase relation between multiple parts.

To ensure constant phase relation between multiple parts in each power-up, autocalibration can be bypassed and capacitor bank can be set manually.

The procedure consists of two stages, reading back the capacitor bank selected by autocalibration and setting the capacitor bank manually for following usage.

Steps to determine the capacitor bank for a specific output frequency are as follows:

- Provide reference signal for PLL2 through OSCIN.
- Set R2 and N2 values for desired VCO frequency.
- Select the VCO core with Register 0x0003, Bit[4:3] (High VCO Core: 01, Low VCO Core: 10).

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- ▶ Send restart command by setting Register 0x001, Bit 1 = 1 and Register 0x001, Bit 1 = 0, consecutively.
- ▶ Read Register 0x008C, which is the corresponding capacitor bank value selected by autocalibration.
- ▶ Create a lookup table with frequency, VCO core, and capacitor bank value, R2 and N2 divider values for each desired frequency.

Steps to set the capacitor bank manually are as follows:

- ▶ Set the corresponding VCO core from lookup table selected before Register 0x0003. Bit[4:3] (High VCO Core: 01, Low VCO Core: 10).
- ▶ Set Register 0x00B2, Bit 0 = 1 to enable capacitor bank selection from SPI.
- ▶ Set Register 0x00B2, Bit[6:2] to value from the lookup table.
- ▶ Set R2 and N2 values for desired VCO frequency.

Multichip Synchronization via PLL2

To synchronize multiple HMC7044 devices together, it is recommended to use the SYNC input pin. If the SYNC pin transitions from 0 to 1 with sufficient setup/hold margin with respect to the VCXO, this synchronization event is deterministically carried through PLL2, up the timing chain through the N2 divider, and then to the main SYSREF timer (see the [Clock Output Network](#) section for more information). This mechanism of deterministic phase adjustment allows synchronization of the SYSREF timer and output phases of multiple HMC7044 devices.

Apply the SYNC input rising edge only once. After sensing the rising edge on the VCXO domain, the SYNC input is ignored for the next $16 \times 6 t_{PD2}$ periods as the FSM processes the event. After this period expires, the FSM becomes sensitive again to the SYNC pin. If the SYNC is applied periodically, the first edge initializes the synchronization process, and then the subsequent edges may or may not be recognized depending on their width/repetition rate with respect to $16 \times 6 t_{PD2}$.

Note that the SYNC rising edge must be provided cleanly with respect to the HMC7044 VCXO input pin (OSCIN/OSCIN). The user normally has access to the CLKINx/CLKINx pins of PLL1, and not to the VCXO signal directly. When PLL1 is locked, however, the VCXO rising edge is roughly aligned to the PLL1 active reference, and, therefore, the user has indirect knowledge of the phase of the VCXO. The VCXO is also available as an output of the HMC7044, if the user wants to retune the SYNC signal more directly.

The phase offset of the PLL1 active reference with respect to the VCXO is a function of the internal delay of each path. This base delay offset is a function of deterministic conditions (LCM, R1, N1 divider setpoints, termination setups, and slew rates), but is also subject to PVT variations that compress or exaggerate this offset.

For most practical purposes, the multichip synchronization feature is limited to PLL1 reference rates <200 MHz.

CLOCK OUTPUT NETWORK

In the HMC7044, PLL1 is responsible for frequency cleanup, redundancy, and hitless switching. PLL2 and the VCOs handle integrated jitter and performance at an 800 kHz offset. Although the PLL1/PLL2 and VCXO components are important, much of the uniqueness of a JESD204B and JESD204C clock generation chip relates to its array of output channels.

In a device such as the HMC7044, some of the output network requirements include the following:

- ▶ Very good phase noise floor of the DCLK channels that can be connected to critical data converter sample clock inputs
- ▶ A large number of DCLK and SYSREF channels
- ▶ Deterministic phase alignment between all output channels relative to one another
- ▶ Fine phase control of synchronization channels with respect to the DCLK channel
- ▶ Frequency coverage to satisfy typical clock rates in expectant systems
- ▶ Skew between SYSREF and DCLK channels that is much less than a DCLK period
- ▶ Spur and crosstalk performance that does not impact system budgets

The HMC7044 output network also supports the following recommended features, which are sometimes critical in user applications:

- ▶ Deterministic synchronization of the output channels with respect to an external signal, which allows multichip synchronization and clean expansion to larger systems
- ▶ Pulse generator behavior to temporarily generate a synchronization pulse stream at user request
- ▶ Flexibility to define unused JESD204B and JESD204C SYSREF and DCLK channels for other purposes
- ▶ Glitchless phase control of signals relative to each other
- ▶ 50% duty cycle clocks with odd division ratios
- ▶ Multimode output buffers with a variety of swings and termination options
- ▶ Skew between all channels that is much less than a DCLK period
- ▶ Adjustable performance vs. power consumption for less sensitive clock channels
- ▶ Flexibility to use an external VCO for very high performance application requirements

Each of the 14 output channels is logically identical. The only distinction between the SYSREF and DCLK channels is in the SPI configuration and in how they are used. Each channel contains independent dividers, phase adjustment, and analog delay circuits. This combination provides the ultimate flexibility, cleanly accommodating nonJESD204B devices in the system.

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In addition to the 14 output channel dividers, there is an internal SYSREF timer that continually operates, and the synchronization of the output channel dividers occurs deterministically with respect to this timer, which can be rephased externally by the user.

The pulse generator functionality of the JESD204B and JESD204C standard involves temporarily generating SYSREF output pulses, with appropriate phasing, to downstream devices. The centralized SYSREF timer and its associated SYNC/pulse generator control manage the process of enabling the intended SYSREF channels,

phasing them, and then disabling them for signal integrity and power saving advantages.

HMC7044 can provide continuous SYSREF clocks in LVPECL, CML, LVDS, and CMOS modes and N-pulse SYSREF clocks in LVPECL, CML, and CMOS modes. If N-pulse LVDS SYSREF clock is needed, output driver type must be set as LVPECL and level translation circuitry given in [Figure 31](#) must be placed between clock channel and LVDS downstream device.

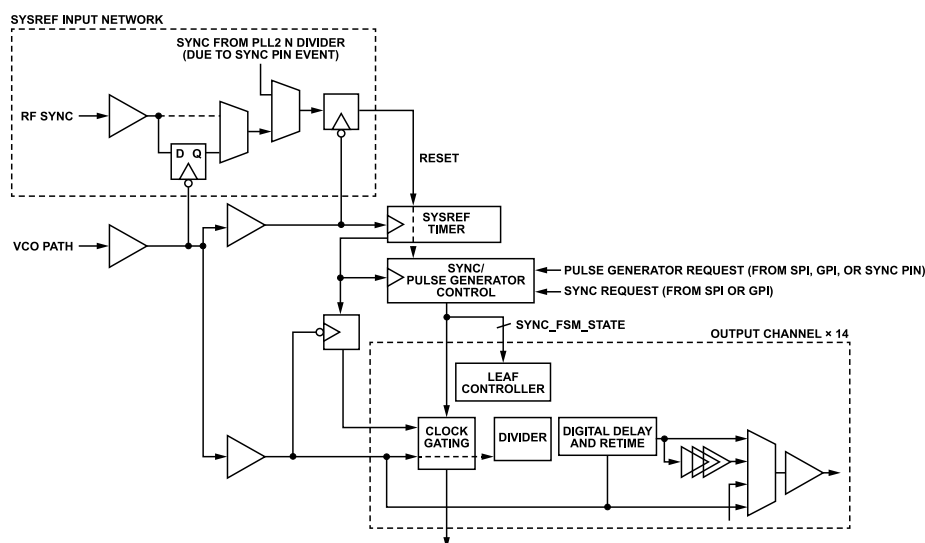


Figure 46. Clock Output Network Simplified Diagram

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Basic Output Divider Channel

Each of the 14 output channels is logically identical, and support divide ratios from 1 to 4094. The supported odd divide ratios (1, 3, 5) have 50.0% duty cycle. The only distinction between a SYSREF channel and a DCLK channel is in the SPI configuration and the typical usage of a given channel.

For basic functionality and phase control, each output path consists of the following:

- ▶ Divider—generates the logic signal of the appropriate frequency and phase
- ▶ Digital phase adjust—adjusts the phase of each channel in increments of $\frac{1}{2}$ VCO cycles
- ▶ Retimer—a low noise flip flop to retime the channel, removing any accumulated jitter
- ▶ Analog fine delay—provides a number of ~25 ps delay steps
- ▶ Selection mux—selects the fundamental, divider, or analog delay, or an alternate path
- ▶ Multimode output buffer—low noise LVDS, CML, CMOS, or LVPECL

The digital phase adjuster and retimer launch on either clock phase of the VCO, depending on the digital phase adjust setpoint (Coarse Digital Delay[4:0]).

To support divider synchronization, arbitrary phase slips, and pulse generator modes, the following blocks are included:

- ▶ A clock gating stage pauses the clock for synchronization or slip operations
- ▶ An output channel leaf ($\times 14$) controller manages slip, synchronization, and pulse generators with information from the SYSREF FSM

Each channel has an array of control signals. Some of the controls are described in [Table 16](#).

System wide broadcast signals can be triggered from the SPI or general-purpose input (GPI) port to issue a SYNC command

(to align dividers to the system internal SYSREF timer), issue a pulse generator stream (temporarily exporting SYSREF signals to receivers), or to cause the dividers to slip a number of VCO cycles to adjust their phases.

Individual dividers can be made sensitive to these events by adjusting their slip enable, SYNC enable, and Start-Up Mode[1:0] configuration, as described in [Table 17](#).

When output buffers are configured in CMOS mode and phase alignment is required among the outputs, additional multislip delays must be issued for Channel 0, Channel 3, Channel 5, Channel 6, Channel 9, Channel 10, and Channel 13. The value of the delay must be as large as half of the selected divider ratio. Note that this requirement of having additional multislip delays is not needed when channels are used in LVPECL, CML, or LVDS mode.

When output buffers are configured in CMOS mode, output driver impedance control bitfield (see [Table 77](#)) is used to control enabled output pin (none, positive, negative or both).

If a channel is configured to behave as a pulse generator, to temporarily power up and power down according to GPI, SPI, or SYNC pin pulse generator commands, it has additional controls to define its behavior outside of the pulse generator chain (see [Table 18](#)).

Each divider has an additional phase offset register that adjusts its start phase, or to influence the behavior of slip events sent via the SPI (see [Table 19](#)).

[Table 20](#) outlines the typical configuration combinations for a DCLK channel relative to a SYSREF synchronization channel. Note that other combinations are possible. Synchronization of downstream devices can be managed manually, or by using the pulse generator functionality of the HMC7044. See the [Typical Programming Sequence](#) section for more information about the differences between the two methods.

Table 16. Basic Divider Controls

| Bit Name | Description |
|------------------------------|--|
| Channel Enable | Channel enable. If 0, the channel is disabled. If 1, the channel can be enabled depending on the settings of Start-Up Mode[1:0], Seven Pairs of 14-Channel Outputs Enable[6:0], and sleep mode. |
| 12-Bit Channel Divider[11:0] | Divide ratio. 12-bit divide ratio, split across two words (MSB and LSB). Set to 0 if not using the channel divider (Output Mux Selection[1:0] = 2 or 3). |
| High Performance Mode | High performance mode. Adjusts divider and buffer bias to slightly improve swing/phase noise at the expense of power. The performance advantage is about 1 dB, and the current penalty depends on whether the divider is enabled. |
| Coarse Digital Delay[4:0] | Digital delay. Adjusts the phase of the divider signal by up to $17 \frac{1}{2}$ cycles of the VCO. This circuit is practically noiseless; however, note that a low amount of additional current is consumed. |
| Fine Analog Delay[4:0] | Analog delay. Adjusts the delay of the divider signal in increments of ~25 ps. Set Output Mux Selection[1:0] = 1 to expose this channel. Causes phase noise degradation of up to 12 dB; therefore, do not use on noise sensitive DCLK channels. |
| Output Mux Selection[1:0] | Output mux selection. 00 = divider channel, 01 = analog delay, 10 = other channel of pair, 11 = input VCO clock. Fundamental mode can be generated with the divider (12-Bit Channel Divider[11:0] = 1), or via Output Mux Selection[1:0] = 10 and 12-Bit Channel Divider[11:0] = 0. Because the divider path consumes power and degrades phase noise slightly, the fundamental mux path is |

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Table 16. Basic Divider Controls (Continued)

| Bit Name | Description |
|----------|--|
| | recommended, but at a cost of a deterministic skew vs. a path that is divider based. Such skew can be compensated for with delay (digital and analog) on the divider-based path. |

Table 17. Channel Features

| Bit Name | Description |
|--------------------|--|
| Slip Enable | Slip enable. A channel process slip requests broadcast from the SPI or GPI (or, if multislip enable = 1, initiated following a recognized SYNC or pulse generator startup). |
| SYNC Enable | SYNC enable. A channel processes synchronization events broadcast from the SPI or GPI or due to SYNC/RF SYNC (via the SYSREF FSM) to reset its phase. This signal can be safely toggled on and off to adjust SYNC sensitivity without risking the state of the divider. |
| Start-Up Mode[1:0] | 00 = asynchronous (normal mode). The divider starts with uncontrolled phase. It is rephased by SYNC events if SYNC enable = 1. 11 = dynamic (pulse generator mode). The divider monitors pulse generator events broadcast from the SYSREF controller. It is powered up just before a pulse generator chain, rephased at the start, and powered down after the pulse generator chain. This is only supported for divide ratios > 31. |

Table 18. Pulse Generator Mode Behavior Options

| Bit Name | Description |
|-----------------------|---|
| Dynamic Driver Enable | Dynamic output buffer enable (pulse generator mode only). 0 = the output buffer is simply enabled/disabled with the main channel enable. 1 = the output buffer enable is controlled together with the channel divider, which allows it to dynamically power down outside pulse generator events. |
| Force Mute[1:0] | Force mute for dynamic mode. If 10, and the channel enable is true (channel enable = 1), the signal just before the output buffer is asynchronously forced to Logic 0 when not generating pulses. Otherwise, if 00, outputs are forced to float naturally to V_{CM} . To see the effect of this, the output buffer must be enabled, which is dependent on the dynamic driver enable and Start-Up Mode[1:0] controls. Logic 0 is supported for CML, LVPECL, and CMOS driver modes. Additional circuitry for LVDS Logic 0 operation is given in Figure 31 . |

Table 19. Multislip Configuration

| Bit Name | Description |
|--------------------------------------|--|
| Multislip Enable | Allow multislip. This bit determines whether the 12-Bit Multislip Digital Delay[11:0] parameter is used for multislip operations. Note that a multislip operation is automatically started following a SYNC or pulse generator initiation if multislip enable = 1. |
| 12-Bit Multislip Digital Delay[11:0] | Multislip amount. If multislip enable = 1, any slip events (caused by GPI, SPI, SYNC, or pulse generator events) repeat the number of times set by 12-Bit Multislip Digital Delay[11:0] to adjust the phase by the multislip amount \times VCO cycles. A value of 0 is not supported if multislip enable = 1. Note that phase slips are free from a noise and current perspective, that is, no additional power is needed and with no noise degradation, but they take some time to occur. Each slip operation takes a number of nanoseconds to complete, and thus the phases do not necessarily stabilize immediately. An alarm is available for the user to indicate when all phase operations are complete. |

Table 20. Typical Configuration Combinations

| Bit Name | DCLK | Pulse Generator SYSREF | Manual SYSREF | Non-JESD204B or JESD204C |
|------------------------------|-------------|------------------------|---------------|--------------------------|
| 12-Bit Channel Divider[11:0] | Small | Big | Big | Any |
| Start-Up Mode Bit | Normal | Pulse generator | Normal | Normal |
| Fine Analog Delay[4:0] | Off | Optional | Optional | Off |
| Coarse Digital Delay[4:0] | Optional | Optional | Optional | Optional |
| Slip Enable | Optional | Optional | Optional | Optional |
| Multislip Enable | Optional | Off | Optional | Optional |
| High Performance Mode | Optional | Off | Off | Optional |
| Sync Enable | On | On | On | Optional |
| Dynamic Driver Enable | Do not care | On | Do not care | Do not care |
| Force Mute[1:0] | Do not care | On | Do not care | Do not care |

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Synchronization FSM/Pulse Generator Timing

The block diagram showing the interface of the SYNC/pulse generator control to the divider channels and the internal SYSREF timer is shown in [Figure 46](#).

The SYSREF timer counts in periods defined by SYSREF Timer[11:0], a 12-bit setting from the SPI. It sequences the enable, reset, and startup, and disables the downstream dividers in the event of SYNC or pulse generator requests. Program the SYSREF timer count to a submultiple of the lowest output frequency in the clock network, and not faster than 4 MHz. To synchronize divider channels, it is recommended, though not required, that the SYSREF Timer[11:0] bits be set to a related frequency that is either a factor or multiple of other frequencies on the IC.

The pulse generator is defined with respect to the periods of this SYSREF timer, not with respect to the output period. This leads to timing constraint that must be considered to prevent any runt pulses from affecting the pulse generator stream.

[Figure 48](#) shows the start-up behavior of an example divider that is configured as a pulse generator, with a period matching the internal SYSREF period.

The startup of the pulse stream occurs a fixed number of VCO cycles after the FSM transitions to the start phase. Disabling the pulse generator stream where the logic path is forced to zero comes from a combinational path, directly from the FSM.

Because the divider has the option for nearly arbitrary phase adjustment, it provides the opportunity for the stop condition to arrive when the pulse stream is a Logic 1, and creates a runt pulse.

For phase offsets of zero to 50% – 8 VCO cycles, and VCO frequencies <3 GHz, this condition is met naturally within the design. For fanout only mode >3 GHz, it is recommended to use digital delay or slip offsets to increase the natural phase offset and avoid the stress condition.

The situation is avoided by never applying phase offset more than 50% – 8 VCO cycles to an output channel configured as a pulse generator.

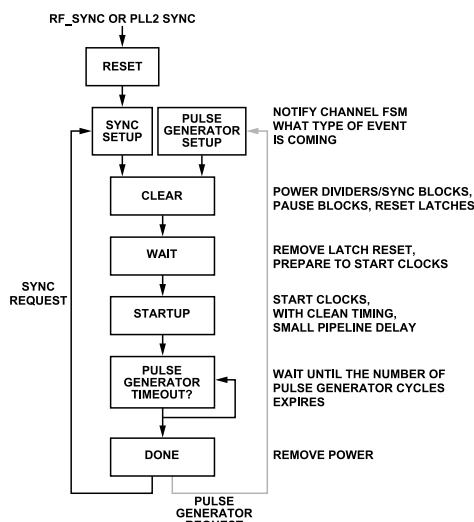


Figure 47. Synchronization FSM Flowchart

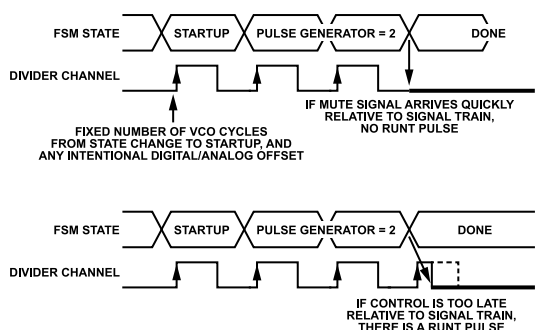


Figure 48. Start-Up Behavior of an Example Divider Configured as a Pulse Generator

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Clock Grouping, Skew, and Crosstalk

Although the output channels are logically independent, for physical reasons, they are first grouped into pairs called clock groups. Each clock group shares a reference, an input buffer, and a sync retime flip flop originating from the VCO distribution network.

The second level of grouping is according to the supply pin. Clock Group 1 (Channel 2 and Channel 3) is on an independent supply, and the other supply pins are each responsible for two clock groups.

As the output channels are more tightly coupled (by sharing a clock group, or by sharing a supply pin), the skew is minimized. However, the isolation between those channels suffers. [Table 21](#) shows the clock grouping, and [Table 22](#) show the typical skew and isolation that can be expected and how it scales with distance between output channels.

Isolation improves as either the aggressor or affected frequencies decrease. Nevertheless, for particularly important clock channels where spurious tones must be minimized, carefully consider their frequency and channel configurations to isolate continuously running frequencies onto different supply domains. Channels configured as pulse generators are normally not an issue, because they are disabled during normal operation.

Table 21. Supply Pin Clock Grouping by Location

| Supply Pin | Location | Clock Group | Channel |
|------------|-----------|-------------|----------|
| VCC2_OUT | Southwest | 1 | 2 3 |
| VCC4_OUT | South | 2 | 4 5 |
| | | 3 | 6 7 |
| VCC8_OUT | North | 4 | 8 9 |
| | | 5 | 10 11 |
| VCC9_OUT | Northwest | 6 | 12 13 |
| | | 0 | 0 1 |

Table 22. Typical Skew and Isolation vs. Distance

| Distance | Typical Skew (ps) | 1 GHz Isolation Differential (dB) |
|--|-------------------|-----------------------------------|
| Distant Supply Group | ±20 | 90 to 100 |
| Closest Neighbor on Different Supply Group | ±15 | 70 |
| Shared Supply | ±10 | 60 |
| Same Clock Group | ±10 | 45 |

Output Buffer Details

Figure 49 shows the clock groups by supply pin location on the package. With appropriate supply pin bypassing, spurious noise of the outputs is improved. Table 21 describes how the supply pins of each of the 14 clock channels are connected within the seven clock groups. Clock channels that are closest to each other have the best channel to channel skew performance, but they also have the lowest isolation from each other. Select critical signals that require high isolation from each other from groups with distant supply pin locations. An example of the expected isolation and channel to channel skew performance of the HMC7044 at 1 GHz is provided in Table 22.

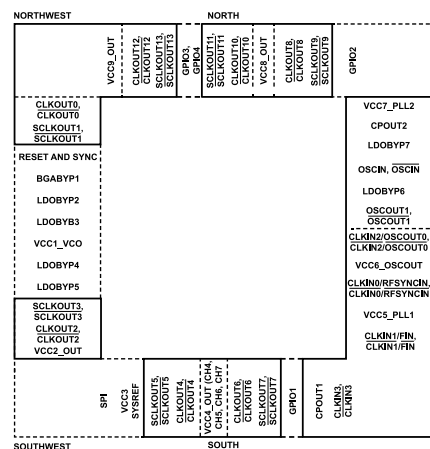


Figure 49. Clock Grouping

SYSREF Valid Interrupt

One of the challenges in a JESD204B and JESD204C system is to control and minimize the latency from the primary system controller IC, typically an ASIC, or FPGA, to the data converters. To estimate the correct amount of latency in the system, the designer must know how long it takes for a main clock generator like the HMC7044 to provide the correct output phases at each output channel after receiving the synchronization request. Typically, a period of time is required on the device to implement the change requests on the outputs due to internal state machine cycles, data transfers, and any propagation delays. The SYSREF valid interrupt is a function to notify the user that the correct output settings and phase relationships are established, allowing the user to identify quickly that the desired SYSREF and device clock states are presented at the outputs of the HMC7044.

The user has the flexibility to assign the SYSREF valid interrupt to a GPO pin or to use a software flag, set via Register 0x007D, Bit 2, which the user can poll as necessary. The flag notifies the user when the system is configured and operating in the desired state, or conversely when it is not ready.

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Phase Behavior of Synchronized Divided Clocks

When the output dividers of the HMC7044 are synchronized, division ratios larger than 1 may lead to instances of synchronization failure under cold temperatures or low supply voltages. This may result in the first falling edge shifting by ± 4 VCO (ΔT) cycles, causing all following pulses or clock cycles to shift by the same number of VCO cycles. Figure 50 shows the timing diagram of this behavior. This issue was resolved on the HMC7044B, which is a form, fit, and functionally compatible device to the HMC7044. For new designs, the HMC7044B is recommended for use instead of the HMC7044. Contact the factory for more information if desired.

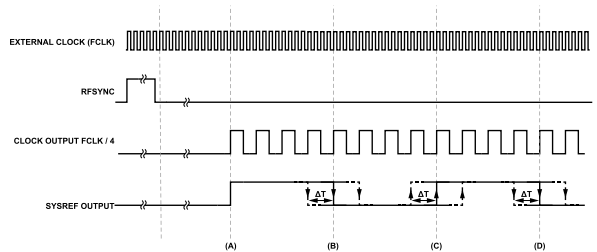


Figure 50. Timing Diagram of Intermittent Edge Shift Behavior

REFERENCE BUFFER DETAILS

Input Termination Network—Common for All Input Buffers

The four reference input buffers to PLL1, as well as the VCXO input buffer, share similar architecture, and control features. The input termination network is configurable to 100 Ω , 200 Ω , and 2 k Ω differentially. It is typically ac-coupled on the board, and uses the on-chip resistive divider to set the internal common-mode voltage, V_{CM} , to 2.1 V.

By closing the 50 Ω termination switch (see Figure 51), the network also serves as the termination system for an LVPECL driver. Although the input termination network for the four PLL1 reference buffers and the VCXO input buffer is identical, the buffer behind the network is different.

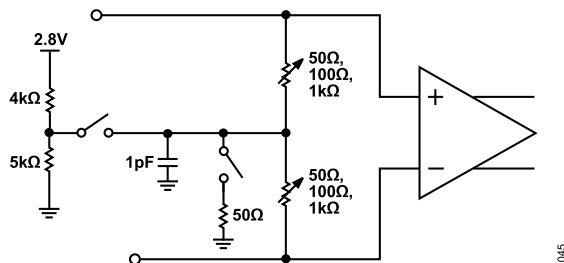


Figure 51. On-Chip Termination Network for VCXO and Reference Buffers

PLL1 Reference Buffer Stages

The PLL1 reference buffers use a CMOS input stage, are capable of a wide common-mode input range (0.4 V to 2.4 V), and have hysteresis to support reliable LOS detection. These buffers are designed to be driven reliably with an input swing of >375 mV p-p diff (the half swing point of the LVDS standard), and support up to 800 MHz operation. For signal swings that are below 375 mV p-p diff, the hysteresis of the buffer can engage and shut down the signal to the internal reference paths. The exact input hysteresis threshold varies as a function of common-mode level and input frequency, but generally ranges from about 75 mV p-p diff to 300 mV p-p diff.

VCXO Buffer Stage

The VCXO input buffer is implemented with a bipolar input stage to meet the stringent noise requirements of PLL2. Its common-mode input range is tighter and, if set externally, must be kept between 1.6 V and 2.4 V. This buffer does not have hysteresis and is functional down to very low signal levels. Although the buffer remains functional down to these low signal levels, for optimal performance, keep the input power greater than -4 dBm when driven single-ended, or -7 dBm per side when driven differentially.

Recommendations for Normal Use

For both styles of buffer, unless there are extenuating circumstances in the application, use the 100 Ω differential termination to control reflections, use the on-chip dc bias network to set the common-mode level, and externally ac couple the input signals. Do not use receiver side dc termination of the LVPECL signal.

Single-Ended Operation

The buffers support single-ended signals with a slightly reduced input sensitivity and bandwidth. If driving these buffers single-ended, ac couple the unused section of the buffer to ground at the input of the die.

Maximum Signal Swing Considerations

The internal supplies to these buffers are regulated from 3.3 V to 2.8 V using on-chip regulation. With very high power references, the signal swing can be enough to drive the signal above the 2.8 V rail. The ESD network and parasitic diodes are generally able to shunt the excess power, and protect the internal circuits even above 13 dBm. Nevertheless, to protect from latch-up concerns, the signals on reference inputs must not exceed the 2.8 V internal supply. For a 2.1 V common-mode, 50 Ω single-ended source, this 2.8 V limit allows ~700 mV of amplitude, or 6 dBm of maximum reference power.

TYPICAL PROGRAMMING SEQUENCE

To initialize the HMC7044 to an operational state, use the following programming procedure:

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1. Connect the HMC7044 to the rated power supplies. No specific power supply sequencing is necessary.
2. Release the hardware reset by switching from Logic 1 to Logic 0) when all supplies are stable.
3. Load the configuration updates (provided by Analog Devices) to specific registers (Register 0x009F, Register 0x00A0, Register 0x00A5, Register 0x00A8, and Register 0x00B0 must be updated with new values, see [Table 75](#)).
4. Program PLL2. Select the VCO range (high or low). Then program the dividers (R2, N2, and reference doubler).
5. Program PLL1. Set the lock detect timer threshold based on the PLL1 bandwidth of the user system. Set the LCM, R1, and N1 divider setpoints. Enable the reference and VCXO input buffer terminations.
6. Program the SYSREF timer. Set the divide ratio (a submultiple of the lower output channel frequency). Set the pulse generator mode configuration, for example, selecting level sensitive option and the number of pulses desired.
7. Program the output channels. Set the output buffer modes (for example, LVPECL, CML, and LVDS). Set the divide ratio, channel start-up mode, coarse/analog delays, and performance modes.
8. Wait until the VCO peak detector loop has stabilized (~10 ms after Step 4).
9. Ensure that the references are provided to PLL1 and the VCXO is powered.
10. Issue a software restart to reset the system and initiate calibration. Toggle the restart dividers/FSMs bit to 1 and then back to 0.
11. PLL1 starts to lock in parallel with PLL2 going through its calibration and lock procedure. Wait for PLL2 to be locked (takes ~50 μ s in typical configurations).
12. Confirm that PLL2 is locked by checking the PLL2 lock detect bit.
13. Send a sync request via the SPI (set the reseed request bit) to align the divider phases and send any initial pulse generator stream.
14. Wait 6 SYSREF periods ($6 \times \text{SYSREF Timer}[11:0]$) to allow the outputs to phase appropriately (takes ~3 μ s in typical configurations).
15. Confirm that the outputs have all reached their phases by checking that the clock outputs phases status bit = 1.
16. At this time, initialize any other devices in the system. PLL1 may not be locked yet, but the small frequency offset that can result on the output of the HMC7044 is not normally severe enough to cause synchronization or initialization failures. Configure node JESD204B/JESD204C devices in the system to operate with the SYSREF signal outputs from the HMC7044. SYSREF channels from the HMC7044 can either be on asynchronously, or dynamically, and can temporarily turn on for a pulse generator stream.

17. Wait for PLL1 to lock. This takes ~50 ms for a 100 Hz bandwidth (from Step 11).
18. When all JESD204B/JESD204C nodes are powered and ready, send a pulse generator request to send out a pulse generator chain on any SYSREF channels programmed for pulse generator mode.

The system is now initialized.

For power savings and the reduction of the cross-coupling of frequencies on the HMC7044, shut down the SYSREF channels.

1. Program each JESD204B/JESD204C node to ignore the SYSREF input channel.
2. On the HMC7044, disable the individual channel enable bits of each SYSREF channel.

To resynchronize one or more of the JESD204B/JESD204C nodes, use the following procedure:

1. Set the channel enable (and SYNC enable bit) of the SYSREF channel of interest.
2. To prevent an output channel from responding to a sync request, disable the SYNC enable mask of each channel so that it continues to run normally without a phase adjustment.
3. Issue a reseed request to phase the SYSREF channel properly with respect to the DCLK.
4. Enable the JESD204B/JESD204C node sensitivity to the SYSREF channel.
5. If the SYSREF channel is in pulse generator mode, wait at least 20 SYSREF periods from Step 3, and issue a pulse generator request.

POWER SUPPLY CONSIDERATIONS

The HMC7044 contains on-board regulators to shield some of the more sensitive supplies from external noise and interference as much as possible. Nevertheless, the user must still take special care to the supply noise profile of the VCC1_VCO supply to achieve the intended performance of the device.

In general, a flat input noise of 200 nV/Hz is an equivalent contributor to the VCO noise and causes a 3 dB increase in the noise profile from about 100 kHz to 10 MHz when the VCO is the dominant contributor. This increase equates to a roughly one-to-one conversion from dBV to dBc/Hz at a 1 MHz offset, and $f_{\text{OUT}} = 2.457$ GHz, that is, 200 nV/Hz = -134 dBV, and the performance of the VCO at 1 MHz offset at 2.4576 GHz is ~-134 dBc/Hz. The PSRR of the VCO follows its closed-loop noise profile; therefore, as the offset moves in and the VCO profile becomes higher, the 200 nV/Hz noise stays approximately equal to the VCO. To stay suitably below the VCO, a supply input with <50 nV/Hz is recommended on the VCC1_VCO pin across the 100 kHz to 10 MHz frequency range.

The output buffers are also susceptible to supply noise, but to a lesser extent. A noise tone of -60 dBV at a 40 MHz offset results in a -90 dBc tone at the output of the buffers in CML mode and

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–85 dBc in LVPECL mode. This result is a relatively flat frequency response, and these numbers are measured differentially. Phase noise/spurs caused by supply noise on the output buffers do not scale with output frequency, whereas those on the VCO do.

Table 23 lists the supply network of the HMC7044 by pin, showing the relevant functional blocks. Six different usage profiles are defined for the network, not including the output channel supplies, which are accounted for separately.

The values listed under Profile 0 to Profile 5 in Table 23 and Table 24 are the typical currents of that block or feature. If a number is not listed in a profile column, a typical profile does not exist for that block or feature, but the user can mix and match features outside of the profile list, and can determine what the power consumption is going to be given the current listings per feature.

Table 23. Supply Network of the HMC7044 by Pin for PLL1, PLL2, VCO, and SYSREF

| Circuit Block | Comment | Typical Current (mA) | Profile ¹ | | | | | |
|---|---|-------------------------|----------------------|-----|----|-----|----|----|
| | | | 0 | 1 | 2 | 3 | 4 | 5 |
| VCC5_PLL1 | | | | | | | | |
| CLKIN1/CLKIN1 | Used as a PLL1 reference | 2 | | 2 | 2 | | 2 | 2 |
| CLKIN1/CLKIN1 Buffer | Extra if used as buffer for external VCO | 5 | | | | | 5 | 5 |
| CLKIN0/CLKIN0 | Used as a PLL1 reference | 2 | | 2 | | | | |
| CLKIN0/CLKIN0 Buffer | Extra current if used as RF synchronization buffer ² | 5 | | | | | | |
| External VCO Path (f _{OUT}) | | 18 | | | | | 18 | |
| External VCO Path | Extra current for divide by 2 | 10 | | | | | | |
| External RF Synchronization Path ³ | | 3 | | | | | | |
| Regulator to 1.8 V, Bypassed on LDOBYP2 | N2, digital functions | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| PLL1 Functions | LOS, R1, N1, FSMs | 10 | | 10 | 10 | | | |
| PLL2 Functions | R2, N2, lock detect | 17 | | 17 | | 17 | 17 | |
| SYSREF Timer | | 1 | | 1 | | | | |
| GPO Drivers in High Speed Mode ⁴ | | | | | | | | |
| Regulator to 2.8 V, Bypassed on LDOBYP3 | | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| PLL1 PFD/CP | | 7 | | 7 | 7 | | | |
| PLL1 DAC Holdover Circuits | | 2 | | 2 | | | | |
| CLKIN2/CLKIN2 Buffer | | 2 | | 2 | | | | |
| CLKIN3/CLKIN3 Buffer | | 2 | | 2 | | | | |
| Subtotal for VCC5_PLL1 | | 90 | 4 | 49 | 23 | 21 | 46 | 11 |
| VCC7_PLL2 | | | | | | | | |
| Regulator to 2.8 V, Bypassed on LDOBYP7 | | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| PLL2 PFD, Doubler, and R2 and N2 Outputs | | 21 | 4 | 21 | | 21 | 21 | |
| PLL2 Charge Pump | | 8 | | 8 | | 8 | 8 | |
| Regulator to 2.8 V, Bypassed on LDOBYP6 | | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| VCXO Buffer | | 16 | | 16 | 16 | 16 | 16 | |
| OSCOUTx/OSCOUTx Divider/Mux ⁵ | | 8 | | | | | | |
| Subtotal for VCC7_PLL2 | | 57 | 8 | 49 | 20 | 49 | 49 | 4 |
| VCC1_VCO | | | | | | | | |
| VCO Distribution Network | Minimum possible value | 71 | 8 | 71 | 0 | 71 | 71 | 71 |
| Sync Retiming Network | Minimum possible value ⁶ | 8 | | | | | | |
| VCO Regulator, Bypass to LDOBYP4 and LDOBYP5 | | 84 | | 84 | | 84 | | |
| VCO Core | | | | | | | | |
| Subtotal for VCC1_VCO | | 163 | 8 | 155 | 0 | 155 | 71 | 71 |
| VCC3_SYSREF | | | | | | | | |
| SYSREF Input Network ³ | | 11 | | | | | | |
| SYSREF Counter Base | | 12 | | 12 | | | | 12 |
| SYSREF Counter, SYNC network | | 4 | | | | | | |

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Table 23. Supply Network of the HMC7044 by Pin for PLL1, PLL2, VCO, and SYSREF (Continued)

| Circuit Block | Comment | Typical Current (mA) | Profile ¹ | | | | | |
|---------------------------------|---------|----------------------|----------------------|-----|----|-----|-----|----|
| | | | 0 | 1 | 2 | 3 | 4 | 5 |
| Subtotal for VCC3_SYSREF | | 27 | 0 | 12 | 0 | 0 | 0 | 12 |
| Subtotal (Without Output Paths) | | | 20 | 265 | 43 | 225 | 166 | 98 |

¹ Profile 0 = sleep mode; Profile 1 = power-up defaults, PLL1 with four references and PLL2 locked with internal VCO, SYSREF timer running; Profile 2 = PLL1 only, one reference; Profile 3 = PLL2 + VCO, PLL1 disabled, Profile 4 = PLL2 with external VCO, PLL1 disabled, Profile 5 = fanout mode only, SYSREF running.

² This is the incremental amount of current for the circuit when put in this mode. For example, the CLKIN0/CLKIN0 buffer used for PLL1 reference path is 2 mA. If it is used as the external synchronization buffer instead, it is 2 + 5 mA.

³ The transient current in PLL2 synchronization mode can be temporarily enabled when using external synchronization.

⁴ The current is highly dependent on rate of input/output and load of input/output traces. For heavily loaded traces, it is recommended to use a series resistance of ~100 Ω to minimize the IR drop on the internal regulator during transitions.

⁵ The function varies from 8 mA to 14 mA depending on divide ratio.

⁶ A temporary current only.

Table 24. Supply Network of the HMC7044 by Pin for the Clock Output Network

| Per Output Channel | Comment | Typical Current (mA) | Profile ¹ | | | | |
|-------------------------------------|---------------------------|-----------------------|----------------------|-----|-----|-----|-----|
| | | | 0 | 1 | 2 | 3 | 4 |
| Digital Regulator and Other Sources | | 2.5 | 0.5 | 2.5 | 2.5 | 2.5 | 2.5 |
| Buffer | | | | | | | |
| LVPECL | | | | | | | |
| | Including term currents | 43 | | 43 | 43 | | 43 |
| CML100 | | | | | | | |
| High Power | Including term currents | 31 | | | | | |
| Low Power | | 24 | | | | | |
| LVDS | | | | | | | |
| High Power | At 307 MHz | 10 | | | | 10 | |
| Low Power | | | | | | | |
| CMOS | At 100 MHz, both sections | 25 | | | | | |
| Channel Mux | | Included ² | | | | | |
| Digital Delay | | | | | | | |
| Off | | Included ² | | | | | |
| Setpoint > 1 | | 3 | | | 3 | | 3 |
| Analog Delay | | | | | | | |
| Off | | Included ² | | 0 | | | |
| Minimum Setting | Glitchless mode enabled | 9 | | | 9 | | |
| Maximum Setting | | 9 | | | | | 9 |
| Divider Logic | | | | | | | |
| 0 | Not using divider path | Included ² | | 0 | | 0 | |
| ÷1 | | 27 | | | | | |
| ÷2 | | 27 | | | | | |
| ÷3 | | 31 | | | | | |
| ÷4 | | 29 | | | | | |
| ÷5 | | 32 | | | | | |
| ÷6 | | 29 | | | | | |
| ÷8 | | 30 | | | | | |
| ÷16 | | 31 | | | 31 | | |
| ÷32 | | 32 | | | | | |
| ÷2044 | | 32 | | | | | 32 |

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Table 24. Supply Network of the HMC7044 by Pin for the Clock Output Network (Continued)

| Per Output Channel | Comment | Typical Current (mA) | Profile ¹ | | | | |
|-------------------------|---------|----------------------|----------------------|----|----|----|----|
| | | | 0 | 1 | 2 | 3 | 4 |
| SYNC Logic ³ | | 4 | | | | | |
| Slip Logic ³ | | 4 | | | | | |
| Subtotal | | | 2.5 | 48 | 89 | 13 | 92 |

¹ Profile 0 = sleep mode; Profile 1 = fundamental mode; Profile 2 = SYSREF channel matched to fundamental mode; Profile 3 = LVDS—high power signal source from other channel; Profile 4 = worst case configuration for power consumption of a channel.

² The base current consumption of the circuit (for example, mux) is included in the buffer typical current.

³ Currents occur only temporarily during a synchronization event.

SERIAL CONTROL PORT

SERIAL PORT INTERFACE (SPI) CONTROL

The HMC7044 can be controlled via the SPI using 24-bit registers and three pins: serial port enable (SLEN) serial data input/output (SDATA), and serial clock (SCLK).

The 24-bit register, shown in Table 25, consists of the following:

- ▶ 1-bit read/write command
- ▶ 2-bit multibyte field (W1, W0)
- ▶ 13-bit address field (A12 to A0)
- ▶ 8-bit data field (D7 to D0)

Table 25. SPI Bit Map

| MSB | | | | LSB |
|--------|--------|--------|------------|-----------|
| Bit 23 | Bit 22 | Bit 21 | Bits[20:8] | Bits[7:0] |
| R/W | W1 | W0 | A12 to A0 | D7 to D0 |

Typical Read Cycle

A typical read cycle is shown in Figure 51 and occurs as follows:

1. The main (host) asserts both SLEN and SDATA to indicate a read, followed by a rising edge SCLK. The node (HMC7044) reads SDIO on the first rising edge of SCLK after SLEN. Setting SDATA high initiates a read.
2. The host places the 2-bit multibyte field to be written to low (0) on the next two falling edges of SCLK. The HMC7044 registers the 2-bit multibyte field on the next two rising edges of SCLK.
3. The host places the 13-bit address field (A12 to A0) MSB first on SDATA on the next 13 falling edges of SCLK. The HMC7044

registers the 13-bit address field (MSB first) on SDATA over the next 13 rising edges of SCLK.

4. The host registers the 8-bit data on the next eight rising edges of SCLK. The HMC7044 places 8-bit data (D7 to D0) MSB first on the next eight falling edges of SCLK.
5. Deassertion of SLEN completes the register read cycle.

Typical Write Cycle

A typical write cycle is shown in Figure 52, and occurs as follows:

1. The main (host) asserts both SLEN and SDATA to indicate a read, followed by a rising edge SCLK. The node (HMC7044) reads SDIO on the first rising edge of SCLK after SLEN. Setting SDATA low initiates a write.
2. The host places the 2-bit multibyte field to be written to low (0) on the next two falling edges of SCLK. The HMC7044 registers the 2-bit multibyte field on the next two rising edges of SCLK.
3. The host places the 13-bit address field (A12 to A0), MSB first on SDATA on the next 13 falling edges of SCLK. The HMC7044 registers the 13-bit address field (MSB first) on SDIO over the next 13 rising edges of SCLK.
4. The host places the 8-bit data (D7 to D0) MSB first on the next eight falling edges of SCLK. The HMC7044 register the 8-bit data (D7 to D0) MSB first on the next eight rising edges of SCLK.
5. The final rising edge of SCLK performs the internal data transfer into the register file, updating the configuration of the device.
6. Deassertion of SLEN completes the register write cycle.

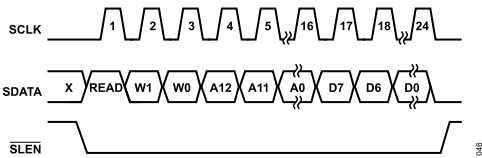


Figure 52. SPI Timing Diagram, Read Operation

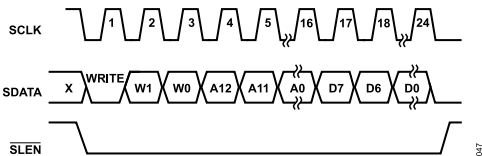


Figure 53. SPI Timing Diagram, Write Operation

APPLICATIONS INFORMATION

PLL1 NOISE CALCULATIONS

Use the following equations to calculate the flicker noise, noise floor, and total unfiltered phase noise specifications for PLL1 (see Table 4).

Calculate the flicker noise using the following equation:

$$PN(f_{OUT}, f_{OFFSET}) = Flicker_FOM + 20 \times \log(f_{OUT}) - 10 \times \log(f_{OFFSET}) \quad (1)$$

where:

$PN()$ is the phase noise.

f_{OUT} is the output frequency.

f_{OFFSET} is the offset of noise frequency from the output carrier frequency.

$Flicker_FOM$ is the figure of merit at the flicker frequency.

Calculate the noise floor as follows:

$$PN(f_{OUT}, f_{PD1}) = Floor_FOM + 20 \times \log\left(\frac{f_{OUT}}{f_{PD1}}\right) + 10 \times \log(f_{PD1}) \quad (2)$$

where:

f_{PD1} is the phase detector frequency of PLL1.

$Floor_FOM$ is the figure of merit at the floor frequency.

Calculate the total phase noise (unfiltered) as follows:

$$PN(f_{OUT}, f_{PD1}, f_{OFFSET}) = 10 \times \log\left(\sqrt{10\left(\frac{PN_Flicker}{10}\right)^2 + 10\left(\frac{PN_Floor}{10}\right)^2}\right) \quad (3)$$

where:

$PN_Flicker$ is the phase noise at the flicker frequency.

PN_Floor is the phase noise at the floor frequency.

PLL2 NOISE CALCULATIONS

Use the following equations to calculate the flicker noise, noise floor, and total unfiltered phase noise specifications for PLL2 (see Table 5).

Calculate the flicker noise using the following equation:

$$PN(f_{OUT}, f_{OFFSET}) = Flicker_FOM + 20 \times \log(f_{OUT}) - 10 \times \log(f_{OFFSET}) \quad (4)$$

where:

f_{OUT} is the output frequency.

f_{OFFSET} is the offset of noise frequency from the output carrier frequency.

$Flicker_FOM$ is the figure of merit at the flicker frequency.

Calculate the noise floor as follows:

$$PN(f_{OUT}, f_{PD2}) = Floor_FOM + 20 \times \log\left(\frac{f_{OUT}}{f_{PD2}}\right) + 10 \times \log(f_{PD2}) \quad (5)$$

where:

$Floor_FOM$ is the figure of merit at the floor frequency.

f_{PD2} is the phase detector frequency of PLL2.

Calculate the total phase noise (unfiltered) as follows:

$$PN(f_{OUT}, f_{PD2}, f_{OFFSET}) = 10 \times \log\left(\sqrt{10\left(\frac{PN_Flicker}{10}\right)^2 + 10\left(\frac{PN_Floor}{10}\right)^2}\right) \quad (6)$$

where:

$PN_Flicker$ is the phase noise at the flicker frequency.

PN_Floor is the phase noise at the floor frequency.

PHASE NOISE FLOOR AND JITTER

Use the following equations to calculate the phase noise floor, jitter density, and rms additive jitter due to floor specifications (see Table 9).

Calculate the phase noise floor using the following equation:

$$PN_{FLOOR} = FOM_{OCHAN} + 10 \times \log(f_{OUT}) + Harmonic\ Degradation + Power\ Degradation \quad (7)$$

where:

PN_{FLOOR} is the phase noise floor at f_{OUT} .

FOM_{OCHAN} is the figure of merit of the output channel.

Harmonic Degradation is the harmonics of the signal captured in the measurement bandwidth of the receiving instrument/circuit. The noise power of those harmonics can fold and influence the overall noise.

Power Degradation results when the noise floor (–174 dBm/Hz) of the measurement system approaches the noise power in the phase noise floor of the signal. For example, a phase noise value of –155 dBc/Hz at 0 dBm carrier level is –155 dBm/Hz and is easily measurable. If, however, the carrier level is –20 dBm, the phase noise of –155 dBc/Hz is –175 dBm/Hz, and is not measurable below the other noise sources in the system.

Calculate the jitter density at f_{OUT} as follows:

$$JITTER_DENSITY_FLOOR = 2 \times 10^{\left(\frac{PN_{Floor}/10}{f_{OUT} \times 2\pi}\right)} \quad (8)$$

where $JITTER_DENSITY_FLOOR$ is the jitter density of floor at f_{OUT} .

Calculate the rms additive jitter due to floor using the following equation:

APPLICATIONS INFORMATION

$$\begin{aligned} &JITTER_RMS_FLOOR \\ &= \frac{JITTER_DENSITY_FLOOR}{\times \sqrt{Observation \ Bandwidth}} \end{aligned} \quad (9)$$

where *Observation Bandwidth* is the desired integration bandwidth of the noise with a lower and upper bound offset from the output carrier frequency.

CONTROL REGISTERS

CONTROL REGISTER MAP

Register addresses that are not listed in [Table 26](#) are not used, and writing to those registers has no effect. Do not change the values of registers that are marked as reserved. When writing to registers with bits that are marked reserved, take care to always write the default value for the reserved bits, unless listed otherwise in the other controls subsection of [Table 26](#).

Table 26. Control Register Map

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) |
|----------------|------------------------------------|--|---|--|-------------------------------------|--|-------------------------|---|----------------------|---------------------------|
| Global Control | | | | | | | | | | |
| 0x0000 | Global soft reset control | Reserved | | | | | | | Soft reset | 0x00 |
| 0x0001 | Global request and mode control | Reseed request | High performance distribution path | Reserved | Force holdover | Mute output drivers | Pulse generator request | Restart dividers/FSMs | Sleep mode | 0x00 |
| 0x0002 | | Reserved | | | | | PLL2 autotune trigger | Slip request | Reserved | 0x00 |
| 0x0003 | Global enable control | Reserved | | RF reseed enable | VCO Selection[1:0] | | SYSREF timer enable | PLL2 enable | PLL1 enable | 0x37 |
| 0x0004 | | Reserved | Seven Pairs of 14-Channel Outputs Enable[6:0] | | | | | | | 0x7F |
| 0x0005 | Global mode and enable control | SYNC Pin Mode Selection[1:0] | | CLKIN1/CLKIN1 in external VCO input mode | CLKIN0/CLKIN0 in RF SYNC input mode | PLL1 Reference Path Enable[3:0] | | | | 0x4F |
| 0x0006 | Global clear alarms | Reserved | | | | | | | Clear alarms | 0x00 |
| 0x0007 | Global miscellaneous control | Reserved | | | | | | | | 0x00 |
| 0x0008 | | Reserved (Scratchpad) | | | | | | | | 0x00 |
| 0x0009 | | Reserved | | | | | | | Disable SYNC at lock | 0x01 |
| PLL1 | | | | | | | | | | |
| 0x000A | CLKIN0/CLKIN0 input buffer control | Reserved | | | Input Buffer Mode[3:0] | | | Buffer enable | 0x07 | |
| 0x000B | CLKIN1/CLKIN1 input buffer control | Reserved | | | Input Buffer Mode[3:0] | | | Buffer enable | 0x07 | |
| 0x000C | CLKIN2/CLKIN2 input buffer control | Reserved | | | Input Buffer Mode[3:0] | | | Buffer enable | 0x07 | |
| 0x000D | CLKIN3/CLKIN3 input buffer control | Reserved | | | Input Buffer Mode[3:0] | | | Buffer enable | 0x07 | |
| 0x000E | OSCIN/OSCIN input buffer control | Reserved | | | Input Buffer Mode[3:0] | | | Buffer enable | 0x07 | |
| 0x0014 | PLL1 reference priority control | Fourth Priority CLKINx/CLKINx Input[1:0] | | Third Priority CLKINx/CLKINx Input[1:0] | | Second Priority CLKINx/CLKINx Input[1:0] | | First Priority CLKINx/CLKINx Input[1:0] | | 0xE4 |

CONTROL REGISTERS

Table 26. Control Register Map (Continued)

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) |
|----------------|---------------------------------------|------------------------------------|----------------------------|--------------------------------------|--------------------|---------------------------|-------------------------------------|------------------------------------|--------------------------------|---------------------------|
| 0x0015 | PLL1 loss of signal (LOS) control | Reserved | | | | | LOS Validation Timer[2:0] | | | 0x03 |
| 0x0016 | PLL1 holdover exit control | Reserved | | | | Holdover Exit Action[1:0] | | Holdover Exit Criteria[1:0] | | 0x0C |
| 0x0017 | PLL1 holdover DAC/ADC control | Reserved | Holdover DAC Value[6:0] | | | | | | | 0x00 |
| 0x0018 | | Reserved | | | | ADC tracking disable | Force DAC to holdover in quick mode | Holdover BW Reduction[1:0] | | 0x04 |
| 0x0019 | PLL1 LOS mode control | Reserved | | | | | | LOS bypass input prescaler | LOS uses VCXO prescaler | 0x00 |
| 0x001A | PLL1 charge pump control | Reserved | | | | PLL1 CP Current[3:0] | | | | 0x08 |
| 0x001B | PLL1 PFD control | Reserved | | | PLL1 PFD up enable | PLL1 PFD down enable | PLL1 PFD up force | PLL1 PFD down force | PLL1 PFD polarity | 0x18 |
| 0x001C | CLKIN0/CLKIN0 input prescaler control | CLKIN0/CLKIN0 Input Prescaler[7:0] | | | | | | | | 0x04 |
| 0x001D | CLKIN1/CLKIN1 input prescaler control | CLKIN1/CLKIN1 Input Prescaler[7:0] | | | | | | | | 0x01 |
| 0x001E | CLKIN2/CLKIN2 input prescaler control | CLKIN2/CLKIN2 Input Prescaler[7:0] | | | | | | | | 0x04 |
| 0x001F | CLKIN3/CLKIN3 input prescaler control | CLKIN3/CLKIN3 Input Prescaler[7:0] | | | | | | | | 0x01 |
| 0x0020 | OSCIN/OSCIN Input prescaler control | OSCIN/OSCIN Input Prescaler[7:0] | | | | | | | | 0x04 |
| 0x0021 | PLL1 reference divider control (R1) | 16-Bit R1 Divider[7:0] (LSB) | | | | | | | | 0x04 |
| 0x0022 | | 16-Bit R1 Divider[15:8] (MSB) | | | | | | | | 0x00 |
| 0x0026 | PLL1 feedback divider control (N1) | 16-Bit N1 Divider[7:0] (LSB) | | | | | | | | 0x10 |
| 0x0027 | | 16-Bit N1 Divider[15:8] (MSB) | | | | | | | | 0x00 |
| 0x0028 | PLL1 lock detect control | Reserved | PLL1 lock detect uses slip | PLL1 Lock Detect Timer[4:0] | | | | | | 0x0F |
| 0x0029 | PLL1 reference switching control | Reserved | Bypass debouncer | Manual Mode Reference Switching[1:0] | | | Holdover uses DAC | Auto-revertive reference switching | Auto- mode reference switching | 0x05 |
| 0x002A | PLL1 holdoff time control | Holdoff Timer[7:0] | | | | | | | | 0x00 |

CONTROL REGISTERS

Table 26. Control Register Map (Continued)

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) |
|---------------------|---|-------------------------------|-------------------------------------|-------|-----------------------|-------------------------------|--|------------------------|---|---------------------------|
| PLL2 | | | | | | | | | | |
| 0x0031 | PLL2 miscellaneous control | Reserved | | | | | | | | 0x01 |
| 0x0032 | PLL2 frequency doubler control | Reserved | | | | | | | Bypass frequency doubler | 0x01 |
| 0x0033 | PLL2 reference divider control (R2) | 12-Bit R2 Divider[7:0] (LSB) | | | | | | | | 0x02 |
| 0x0034 | | Reserved | | | | 12-Bit R2 Divider[11:8] (MSB) | | | | 0x00 |
| 0x0035 | PLL2 feedback divider control (N2) | 16-Bit N2 Divider[7:0] (LSB) | | | | | | | | 0x20 |
| 0x0036 | | 16-Bit N2 Divider[15:8] (MSB) | | | | | | | | 0x00 |
| 0x0037 | PLL2 charge pump control | Reserved | | | | PLL2 CP Current[3:0] | | | | 0x0F |
| 0x0038 | PLL2 PFD control | Reserved | | | PLL2 PFD up enable | PLL2 PFD down enable | PLL2 PFD up force | PLL2 PFD down force | PLL2 PFD polarity | 0x18 |
| 0x0039 | OSCOUTx/ OSCOUTx path control | Reserved | | | | | OSCOUTx/OSCOUTx Divider[1:0] | | OSCOUTx/ OSCOUTx path enable | 0x00 |
| 0x003A | OSCOUTx/ OSCOUTx driver control | Reserved | OSCOUT0/OSCOUT0 Driver Mode[1:0] | | | Reserved | OSCOUT0/OSCOUT0 Driver Impedance[1:0] | | OSCOUT0/ OSCOUT0 driver enable | 0x00 |
| 0x003B | | Reserved | OSCOUT1/OSCOUT1 Driver Mode[1:0] | | | Reserved | OSCOUT1/OSCOUT1 Driver Impedance[1:0] | | OSCOUT1/ OSCOUT1 driver enable | 0x00 |
| 0x003C | PLL2 miscellaneous control | Reserved | | | | | | | | 0x00 |
| GPIO/SDATA Control | | | | | | | | | | |
| 0x0046 | GPI1 control | Reserved | | | GPI1 Selection[3:0] | | | | GPI1 enable | 0x00 |
| 0x0047 | GPI2 control | Reserved | | | GPI2 Selection[3:0] | | | | GPI2 enable | 0x00 |
| 0x0048 | GPI3 control | Reserved | | | GPI3 Selection[3:0] | | | | GPI3 enable | 0x09 |
| 0x0049 | GPI4 control | Reserved | | | GPI4 Selection[3:0] | | | | GPI4 enable | 0x11 |
| 0x0050 | GPO1 control | GPO1 Selection[5:0] | | | | | | GPO1 mode | GPO1 enable | 0x37 |
| 0x0051 | GPO2 control | GPO2 Selection[5:0] | | | | | | GPO2 mode | GPO2 enable | 0x33 |
| 0x0052 | GPO3 control | GPO3 Selection[5:0] | | | | | | GPO3 mode | GPO3 enable | 0x00 |
| 0x0053 | GPO4 control | GPO4 Selection[5:0] | | | | | | GPO4 mode | GPO4 enable | 0x00 |
| 0x0054 | SDATA control | Reserved | | | | | | SDATA mode | SDATA enable | 0x03 |
| SYSREF/SYNC Control | | | | | | | | | | |

CONTROL REGISTERS

Table 26. Control Register Map (Continued)

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) |
|---------------------------------|------------------------------|-------------------------------|---------------------------------------|-------------------------------|---------------------------------------|----------------------------------|-------------------------------------|------------------------------------|---------------------------------|---------------------------|
| 0x005A | Pulse generator control | Reserved | | | | | Pulse Generator Mode Selection[2:0] | | | 0x00 |
| 0x005B | SYNC control | Reserved | | | | | SYNC retime | SYNC through PLL2 | SYNC polarity | 0x06 |
| 0x005C | SYSREF timer control | SYSREF Timer[7:0] (LSB) | | | | | | | | 0x00 |
| 0x005D | | Reserved | | | SYSREF Timer[11:8] (MSB) | | | | 0x01 | |
| 0x005E | SYSREF miscellaneous control | Reserved | | | | | | | | 0x00 |
| Clock Distribution Network | | | | | | | | | | |
| 0x0064 | External VCO control | Reserved | | | | | | Divide by 2 on external VCO enable | Low frequency external VCO path | 0x00 |
| 0x0065 | Analog delay common control | Reserved | | | | | | | Analog delay low power mode | 0x00 |
| Alarm Masks Registers | | | | | | | | | | |
| 0x0070 | PLL1 alarm mask control | PLL1 near lock mask | PLL1 lock acquisition mask | PLL1 lock detect mask | PLL1 holdover status mask | PLL1 CLKINx/CLKINx LOS Mask[3:0] | | | | 0x00 |
| 0x0071 | Alarm mask control | Reserved | | | Sync request mask | PLL1 and PLL2 lock detect mask | Clock outputs phase status mask | SYSREF sync status mask | PLL2 lock detect mask | 0x10 |
| Product ID Registers | | | | | | | | | | |
| 0x0078 | Product ID | Product ID Value[7:0] (LSB) | | | | | | | | 0x01 |
| 0x0079 | | Product ID Value[15:8] (Mid) | | | | | | | | 0x52 |
| 0x007A | | Product ID Value[23:16] (MSB) | | | | | | | | 0x04 |
| Alarm Readback Status Registers | | | | | | | | | | |
| 0x007B | Readback register | Reserved | | | | | | | Alarm signal | |
| 0x007C | PLL1 alarm readback | PLL1 near lock | PLL1 lock acquisition | PLL1 lock detect | PLL1 holdover status | CLKINx/CLKINx LOS[3:0] | | | | |
| 0x007D | Alarm readback | Reserved | | | Sync request status | PLL1 and PLL2 lock detect | Clock outputs phases status | SYSREF sync status | PLL2 lock detect | |
| 0x007E | Latched alarm readback | Reserved | PLL2 lock acquisition latched | PLL1 lock acquisition latched | PLL1 holdover latched | CLKINx/CLKINx LOS Latched[3:0] | | | | |
| 0x007F | Alarm readback miscellaneous | Reserved | | | | | | | | |
| PLL1 Status Registers | | | | | | | | | | |
| 0x0082 | PLL1 status registers | Reserved | PLL1 Best Clock[1:0] | | PLL1 Active CLKINx/CLKINx[1:0] | | PLL1 FSM State[2:0] | | | |
| 0x0083 | | Reserved | PLL1 Holdover DAC Averaged Value[6:0] | | | | | | | |

CONTROL REGISTERS

Table 26. Control Register Map (Continued)

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) |
|------------------------|---------------------------|--|--------------------------------------|--|-------------------------------|-------------------------------------|---------------------|--------------------------------|---|---------------------------|
| 0x0084 | | Holdover comparator value | PLL1 Holdover DAC Current Value[6:0] | | | | | | | |
| 0x0085 | | Reserved | | | | PLL1 active CLKINx/ CLKINxLOS | PLL1 VCXO status | PLL1 holdover ADC status | PLL1 holdover ADC input range status | |
| 0x0086 | | Reserved | | | PLL1 Holdover Exit Phase[1:0] | | Reserved | | | |
| 0x0087 | | Reserved | | | | | | | | |
| PLL2 Status Registers | | | | | | | | | | |
| 0x008C | PLL2 status registers | PLL2 autotune value | | | | | | | | |
| 0x008D | | PLL2 Autotune Signed Error[7:0] (LSB) | | | | | | | | |
| 0x008E | | PLL2 autotune status | PLL2 autotune error sign | PLL2 Autotune Signed Error[13:8] (MSB) | | | | | | |
| 0x008F | | PLL2 Autotune FSM State[3:0] | | | | PLL2 SYNC FSM State[3:0] | | | | |
| 0x0090 | | Reserved | | | | | | | | |
| SYSREF Status Register | | | | | | | | | | |
| 0x0091 | SYSREF status register | Reserved | | | Channel outputs FSM busy | SYSREF FSM State[3:0] | | | | |
| Other Controls | | | | | | | | | | |
| 0x0096 | Reserved | Reserved | | | | Reserved | | | | 0x00 |
| 0x0097 | Reserved | Reserved | | | | Reserved | | | | 0x00 |
| 0x0098 | Reserved | Reserved | | | | Reserved | | | | 0x00 |
| 0x0099 | Reserved | Reserved | | | | Reserved | | | | 0x00 |
| 0x009A | Reserved | Reserved | | | | Reserved | | | | 0x00 |
| 0x009B | Reserved | Reserved | | | | Reserved | | | | 0xAA |
| 0x009C | Reserved | Reserved | | | | Reserved | | | | 0xAA |
| 0x009D | Reserved | Reserved | | | | Reserved | | | | 0xAA |
| 0x009E | Reserved | Reserved | | | | Reserved | | | | 0xAA |
| 0x009F | Reserved | Clock output driver low power setting (for optimum performance, set to 0x4D instead of default value) | | | | | | | | 0x55 |
| 0x00A0 | Reserved | Clock output driver high power setting (for optimum performance, set to 0xDF instead of default value) | | | | | | | | 0x56 |
| 0x00A1 | Reserved | Reserved | | | | Reserved | | | | 0x97 |
| 0x00A2 | Reserved | Reserved | | | | Reserved | | | | 0x03 |
| 0x00A3 | Reserved | Reserved | | | | Reserved | | | | 0x00 |
| 0x00A4 | Reserved | Reserved | | | | Reserved | | | | 0x00 |
| 0x00A5 | Reserved | PLL1 more delay (PFD1, lock detect) (for optimum performance, set to 0x06 instead of default value) | | | | | | | | 0x00 |
| 0x00A6 | Reserved | Reserved | | | | Reserved | | | | 0x1C |
| 0x00A7 | Reserved | Reserved | | | | Reserved | | | | 0x00 |
| 0x00A8 | Reserved | PLL1 holdover DAC g _m setting (for optimum performance, set to 0x06 instead of default value) | | | | | | | | 0x22 |
| 0x00A9 | Reserved | Reserved | | | | Reserved | | | | 0x00 |
| 0x00AB | Reserved | Reserved | | | | Reserved | | | | 0x00 |
| 0x00AC | Reserved | Reserved | | | | Reserved | | | | 0x20 |
| 0x00AD | Reserved | Reserved | | | | Reserved | | | | 0x00 |
| 0x00AE | Reserved | Reserved | | | | Reserved | | | | 0x08 |
| 0x00AF | Reserved | Reserved | | | | Reserved | | | | 0x50 |
| 0x00B0 | Reserved | VTUNE preset setting (for optimum performance, set to 0x04 instead of default value) | | | | | | | | 0x09 |

CONTROL REGISTERS

Table 26. Control Register Map (Continued)

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) | |
|--------------------|--------------------------|---|-------------|-------------|-----------------------|--|-------|------------------|---------------------------|---------------------------|------|
| 0x00B1 | Reserved | Reserved | | | | | | | | 0x0D | |
| 0x00B2 | Manual VCO Calibration | See Table 76 | | | | | | | | 0x00 | |
| 0x00B3 | Reserved | Reserved | | | | | | | | 0x00 | |
| 0x00B5 | Reserved | Reserved | | | | | | | | 0x00 | |
| 0x00B6 | Reserved | Reserved | | | | | | | | 0x00 | |
| 0x00B7 | Reserved | Reserved | | | | | | | | 0x00 | |
| 0x00B8 | Reserved | Reserved | | | | | | | | 0x00 | |
| Clock Distribution | | | | | | | | | | | |
| 0x00C8 | Channel Output 0 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xF3 | |
| 0x00C9 | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | | 0x04 |
| 0x00CA | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x00 | |
| 0x00CB | | Reserved | | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x00CC | | Reserved | | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x00CD | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | | 0x00 |
| 0x00CE | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 | |
| 0x00CF | | Reserved | | | | | | | Output Mux Selection[1:0] | | 0x00 |
| 0x00D0 | | Force Mute[1:0] | | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x01 |
| 0x00D1 | | Reserved | | | | | | | | | 0x00 |
| 0x00D2 | Channel Output 1 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xFD | |
| 0x00D3 | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | | 0x00 |
| 0x00D4 | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x01 | |
| 0x00D5 | | Reserved | | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x00D6 | | Reserved | | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x00D7 | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | | 0x00 |
| 0x00D8 | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 | |
| 0x00D9 | | Reserved | | | | | | | Output Mux Selection[1:0] | | 0x00 |
| 0x00DA | | Force Mute[1:0] | | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x30 |
| 0x00DB | | Reserved | | | | | | | | | 0x00 |
| 0x00DC | Channel Output 2 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xF3 | |
| 0x00DD | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | | 0x08 |
| 0x00DE | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x00 | |
| 0x00DF | | Reserved | | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x00E0 | | Reserved | | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x00E1 | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | | 0x00 |
| 0x00E2 | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 | |
| 0x00E3 | | Reserved | | | | | | | Output Mux Selection[1:0] | | 0x00 |
| 0x00E4 | | Force Mute[1:0] | | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x01 |

CONTROL REGISTERS

Table 26. Control Register Map (Continued)

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) | |
|----------------|-----------------------------|---|-------------|-------------|--------------------------|--|-------|---------------------|---------------------------|---------------------------|------|
| 0x00E5 | | Reserved | | | | | | | | 0x00 | |
| 0x00E6 | Channel Output 3 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xFD | |
| 0x00E7 | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | 0x00 | |
| 0x00E8 | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x01 | |
| 0x00E9 | | Reserved | | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x00EA | | Reserved | | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x00EB | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | 0x00 | |
| 0x00EC | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 | |
| 0x00ED | | Reserved | | | | | | | Output Mux Selection[1:0] | 0x00 | |
| 0x00EE | | Force Mute[1:0] | | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x30 |
| 0x00EF | | | Reserved | | | | | | | | 0x00 |
| 0x00F0 | Channel Output 4 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xF3 | |
| 0x00F1 | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | 0x02 | |
| 0x00F2 | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x00 | |
| 0x00F3 | | Reserved | | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x00F4 | | Reserved | | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x00F5 | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | 0x00 | |
| 0x00F6 | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 | |
| 0x00F7 | | Reserved | | | | | | | Output Mux Selection[1:0] | 0x00 | |
| 0x00F8 | | Force Mute[1:0] | | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x01 |
| 0x00F9 | | | Reserved | | | | | | | | 0x00 |
| 0x00FA | Channel Output 5 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xFD | |
| 0x00FB | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | 0x00 | |
| 0x00FC | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x01 | |
| 0x00FD | | Reserved | | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x00FE | | Reserved | | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x00FF | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | 0x00 | |
| 0x0100 | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 | |
| 0x0101 | | Reserved | | | | | | | Output Mux Selection[1:0] | 0x00 | |
| 0x0102 | | Force Mute[1:0] | | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x30 |
| 0x0103 | | | Reserved | | | | | | | | 0x00 |
| 0x0104 | Channel Output 6 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xF3 | |
| 0x0105 | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | 0x02 | |
| 0x0106 | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x00 | |
| 0x0107 | | Reserved | | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x0108 | | Reserved | | | | Coarse Digital Delay[4:0] | | | | 0x00 | |

CONTROL REGISTERS

Table 26. Control Register Map (Continued)

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) |
|----------------|--------------------------|---|-------------|-----------------------|---------------------------|--|----------|---------------------------|----------------|---------------------------|
| 0x0109 | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | 0x00 |
| 0x010A | | Reserved | | | | 12-bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 |
| 0x010B | | Reserved | | | | | | Output Mux Selection[1:0] | | 0x00 |
| 0x010C | | Force Mute[1:0] | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x01 |
| 0x010D | | Reserved | | | | | | | | 0x00 |
| 0x010E | Channel Output 7 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xFD |
| 0x010F | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | 0x00 |
| 0x0110 | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x01 |
| 0x0111 | | Reserved | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x0112 | | Reserved | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x0113 | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | 0x00 |
| 0x0114 | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 |
| 0x0115 | | Reserved | | | | | | Output Mux Selection[1:0] | | 0x00 |
| 0x0116 | | Force Mute[1:0] | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x30 |
| 0x0117 | | Reserved | | | | | | | | 0x00 |
| 0x0118 | Channel Output 8 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xF3 |
| 0x0119 | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | 0x02 |
| 0x011A | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x00 |
| 0x011B | | Reserved | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x011C | | Reserved | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x011D | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | 0x00 |
| 0x011E | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 |
| 0x011F | | Reserved | | | | | | Output Mux Selection[1:0] | | 0x00 |
| 0x0120 | | Force Mute[1:0] | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x01 |
| 0x0121 | | Reserved | | | | | | | | 0x00 |
| 0x0122 | Channel Output 9 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xFD |
| 0x0123 | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | 0x00 |
| 0x0124 | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x01 |
| 0x0125 | | Reserved | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x0126 | | Reserved | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x0127 | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | 0x00 |
| 0x0128 | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 |
| 0x0129 | | Reserved | | | | | | Output Mux Selection[1:0] | | 0x00 |
| 0x012A | | Force Mute[1:0] | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x30 |
| 0x012B | | Reserved | | | | | | | | 0x00 |

CONTROL REGISTERS

Table 26. Control Register Map (Continued)

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) | |
|----------------|---------------------------------|---|-------------|-------------|--------------------------|--|-------|---------------------|---------------------------|---------------------------|------|
| 0x012C | Channel Output 10 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xF3 | |
| 0x012D | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | | 0x02 |
| 0x012E | | Reserved | | | | 12-bit channel divider[11:8] (MSB) | | | | 0x00 | |
| 0x012F | | Reserved | | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x0130 | | Reserved | | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x0131 | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | | 0x00 |
| 0x0132 | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 | |
| 0x0133 | | Reserved | | | | | | | Output mux selection[1:0] | | 0x00 |
| 0x0134 | | Force Mute[1:0] | | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x01 |
| 0x0135 | | Reserved | | | | | | | | | 0x00 |
| 0x0136 | Channel Output 11 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xFD | |
| 0x0137 | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | | 0x00 |
| 0x0138 | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x01 | |
| 0x0139 | | Reserved | | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x013A | | Reserved | | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x013B | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | | 0x00 |
| 0x013C | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 | |
| 0x013D | | Reserved | | | | | | | Output Mux Selection[1:0] | | 0x00 |
| 0x013E | | Force Mute[1:0] | | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x30 |
| 0x013F | | Reserved | | | | | | | | | 0x00 |
| 0x0140 | Channel Output 12 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xF3 | |
| 0x0141 | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | | 0x10 |
| 0x0142 | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x00 | |
| 0x0143 | | Reserved | | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x0144 | | Reserved | | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x0145 | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | | 0x00 |
| 0x0146 | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 | |
| 0x0147 | | Reserved | | | | | | | Output Mux Selection[1:0] | | 0x00 |
| 0x0148 | | Force Mute[1:0] | | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x01 |
| 0x0149 | | Reserved | | | | | | | | | 0x00 |
| 0x014A | Channel Output 13 control | High performance mode | SYNC enable | Slip enable | Reserved | Start-Up Mode[1:0] | | Multislip enable | Channel enable | 0xFD | |
| 0x014B | | 12-Bit Channel Divider[7:0] (LSB) | | | | | | | | | 0x00 |
| 0x014C | | Reserved | | | | 12-Bit Channel Divider[11:8] (MSB) | | | | 0x01 | |
| 0x014D | | Reserved | | | | Fine Analog Delay[4:0] | | | | 0x00 | |
| 0x014E | | Reserved | | | | Coarse Digital Delay[4:0] | | | | 0x00 | |
| 0x014F | | 12-Bit Multislip Digital Delay[7:0] (LSB) | | | | | | | | | 0x00 |

CONTROL REGISTERS

Table 26. Control Register Map (Continued)

| Addr. (Hex) | Register Name | Bit 7 (MSB) | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 (LSB) | Default Value (Hex) |
|----------------|---------------|-----------------|-------|--------------------------|------------------|--|----------|-----------------------|---------------------------|---------------------------|
| 0x0150 | | Reserved | | | | 12-Bit Multislip Digital Delay[11:8] (MSB) | | | | 0x00 |
| 0x0151 | | Reserved | | | | | | | Output Mux Selection[1:0] | 0x00 |
| 0x0152 | | Force Mute[1:0] | | Dynamic driver enable | Driver Mode[1:0] | | Reserved | Driver Impedance[1:0] | | 0x30 |
| 0x0153 | | Reserved | | | | | | | | |

CONTROL REGISTER MAP BIT DESCRIPTIONS

Global Control (Register 0x0000 to Register 0x0009)

Table 27. Global Soft Reset Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|------------|----------|---|--------|
| 0x0000 | [7:1] | Reserved | | Reserved. | RW |
| | 0 | Soft reset | | Resets all registers, dividers, and FSMs to default values. | |

Table 28. Global Request and Mode Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|------------------------------------|----------|---|--------|
| 0x0001 | 7 | Reseed request | | Requests the centralized resync timer and FSM to reseed any of the output dividers that are programmed to pay attention to sync events. This signal is rising edge sensitive, and is only acknowledged if the resync FSM has completed all events (has finished any previous pulse generator and/or sync events, and is in the done state; SYSREF FSM State[3:0] = 0010). | RW |
| | 6 | High performance distribution path | 0 1 | High performance distribution path select. The VCO clock distribution path has two modes. Power priority. Noise priority. Provides the option for better noise floors on the divided output signals. | |
| | 5 | Reserved | | Reserved | |
| | 4 | Force holdover | | Force PLL1 into holdover mode. A holdover request from the GPI or SPI is debounced inside the device when transferred to the PLL1 FSM clock domain (which is nominally at the VCXO or LCM rate). With the debouncer enabled, the delay from force holdover assertion to the HOLDOVER state is six clock cycles. If the debouncer is bypassed, the delay is two clock cycles. To asynchronously tristate the charge pump, the user can disable the up and down signals from the PFD via Bits[4:3] (PLL1 PFD up enable, PLL1 PFD down enable) in the PLL1 PFD control register (Register 0x001B). | |
| | 3 | Mute output drivers | | Mutes the output drivers (dividers still run in the background). | |
| | 2 | Pulse generator request | | Asks for a pulse stream (see the Typical Programming Sequence section). | |
| | 1 | Restart dividers/FSMs | | Resets all dividers and FSMs. Does not affect configuration registers. | |
| | 0 | Sleep mode | | Forces shutdown. PLL1 and PLL2, output network, and I/O buffers are disabled. | |
| 0x0002 | [7:3] | Reserved | | Reserved. | RW |
| | 2 | PLL2 autotune trigger | | Triggers an autotune if there is an error/issue when the device comes out of reset. | |
| | 1 | Slip request | | Requests a slip or multislip event from all divider channels that are sensitive to slip or multislip commands. The dividers are rising edge sensitive and take some time to process the request, after which the phase synchronization alarm is asserted. | |
| | 0 | Reserved | | Reserved. | |

Table 29. Global Enable Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--------------------|----------|-----------------------------|--------|
| 0x0003 | [7:6] | Reserved | | Reserved | RW |
| | 5 | RF reseeder enable | | Enable RF reseed for SYSREF | |

CONTROL REGISTERS

Table 29. Global Enable Control (Continued)

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|---|---|--|--------|
| 0x0004 | [4:3] | VCO Selection[1:0] | 00 01 10 | Internal disabled/external High Low | |
| | 2 | SYSREF timer enable | | Enable internal SYSREF time reference | |
| | 1 | PLL2 enable | | Main analog enable to PLL2 | |
| | 0 | PLL1 enable | | Main analog enable to PLL1 | |
| | 7 | Reserved | | Reserved | RW |
| | [6:0] | Seven Pairs of 14 Channel Outputs Enable[6:0] | Bit 0 Bit 1 Bit 2 Bit 3 Bit 4 Bit 5 Bit 6 | Enable Channel 0 and Channel 1 Enable Channel 2 and Channel 3 Enable Channel 4 and Channel 5 Enable Channel 6 and Channel 7 Enable Channel 8 and Channel 9 Enable Channel 10 and Channel 11 Enable Channel 12 and Channel 13 | |
| | | | | | |
| | | | | | |

Table 30. Global Mode and Enable Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|---|----------------------------------|---|--------|
| 0x0005 | [7:6] | SYNC Pin Mode Selection[1:0] | 00 01 10 11 | SYNC pin configuration with respect to PLL2. Disabled. SYNC. A rising edge is carried through PLL2. Useful for multichip synchronization. Pulse generator. Request a pulse generator stream from any channels configured for dynamic startup. This behaves in the same way as a GPI requested pulse generator. Causes SYNC if alarm exists, otherwise causes pulse generator. | RW |
| | 5 | CLKIN1/CLKIN $\bar{1}$ in external VCO input mode | | CLKIN1/CLKIN $\bar{1}$ input is used for external VCO. | |
| | 4 | CLKIN0/CLKIN $\bar{0}$ in RF SYNC input mode | | CLKIN0/CLKIN $\bar{0}$ input is used for external RF sync. | |
| | [3:0] | PLL1 Reference Path Enable[3:0] | Bit 0 Bit 1 Bit 2 Bit 3 | Selects and enables the reference path for PLL1. Enable CLKIN0/CLKIN $\bar{0}$ input path. Enable CLKIN1/CLKIN $\bar{1}$ input path. Enable CLKIN2/CLKIN $\bar{2}$ input path. Enable CLKIN3/CLKIN $\bar{3}$ input path. | |
| | | | | | |

Table 31. Global Clear Alarms

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--------------|----------|----------------------|--------|
| 0x0006 | [7:1] | Reserved | | Reserved | RW |
| | 0 | Clear alarms | | Clear latched alarms | |

Table 32. Global Miscellaneous Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-----------------------|----------|---|--------|
| 0x0007 | [7:0] | Reserved | | Reserved. | RW |
| 0x0008 | [7:0] | Reserved (Scratchpad) | | Reserved. The user can write/read to this register to confirm I/Os to the HMC7044. This register does not affect device operation. | RW |
| 0x0009 | [7:1] | Reserved | | Reserved. | RW |
| | 0 | Disable SYNC at lock | 0 1 | PLL2 sends a sync event up N2 when lock is achieved. This feature is disabled and SYNC is not internally generated on PLL2 lock. | |

CONTROL REGISTERS

PLL1 (Register 0x000A to Register 0x002A)

Table 33. CLKINx/CLKINx and OSCIN/OSCIN Input Buffer Control

| Address | Bits | Bit Name | Settings | Description | Access |
|--|-------|------------------------|----------|--|--------|
| 0x000A, 0x000B, 0x000C, 0x000D, 0x000E | [7:5] | Reserved | | Reserved | RW |
| | [4:1] | Input Buffer Mode[3:0] | Bit 0 | Enable internal 100 Ω termination | |
| | | | Bit 1 | Enable ac coupling input mode | |
| | | | Bit 2 | Enable LVPECL input mode | |
| | | | Bit 3 | Enable high-Z input mode | |
| | 0 | Buffer enable | | Enable input buffer | |

Table 34. PLL1 Reference Priority Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--|----------|---|--------|
| 0x0014 | [7:6] | Fourth Priority CLKINx/CLKINx Input[1:0] | | If third choice clock is not available, use the fourth choice clock | RW |
| | [5:4] | Third Priority CLKINx/CLKINx Input[1:0] | | If second choice clock is not available, use the third choice clock | |
| | [3:2] | Second Priority CLKINx/CLKINx Input[1:0] | | If the first choice clock is not available, use the second choice clock | |
| | [1:0] | First Priority CLKINx/CLKINx Input[1:0] | | This is the first choice clock | |

Table 35. PLL1 Loss of Signal (LOS) Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|---------------------------|----------|--|--------|
| 0x0015 | [7:3] | Reserved | | Reserved. | RW |
| | [2:0] | LOS Validation Timer[2:0] | | LCM cycles of LOS hysteresis. This is the number of LCM cycles to wait before exiting LOS state when the reference input becomes valid again. ¹ | |
| | | | 000 | None. | |
| | | | 001 | 2 cycles. | |
| | | | 010 | 4 cycles. | |
| | | | 011 | 8 cycles. | |
| | | | 100 | 16 cycles. | |
| | | | 101 | 32 cycles. | |
| | | | 110 | 64 cycles. | |
| | | | 111 | 128 cycles. | |

¹ The LOS revalidation takes between two and three times this number of cycles. The LOS revalidation ambiguity is dependent on whether another channel is in LOS.

Table 36. PLL1 Holdover Exit Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-----------------------------|-----------------|---|--------|
| 0x0016 | [7:4] | Reserved | | Reserved | RW |
| | [3:2] | Holdover Exit Action[1:0] | 00 | Reset dividers. | |
| | | | 01 | Do nothing. | |
| | | | 10 | Do nothing. | |
| | | | 11 | DAC assist. | |
| | [1:0] | Holdover Exit Criteria[1:0] | X0 ¹ | Criteria the PLL1 FSM uses to exit holdover mode. | |
| | | | 01 | Exit holdover when LOS is gone. | |
| | | | 11 | Exit holdover when phase error = 0. | |
| | | | | Exit holder immediately. | |

¹ X means don't care.

CONTROL REGISTERS

Table 37. PLL1 Holdover DAC/ADC Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-------------------------------------|----------|---|--------|
| 0x0017 | 7 | Reserved | | Reserved | RW |
| | [6:0] | Holdover DAC Value[6:0] | | In holdover mode, if ADC tracking disable is set 1, the holdover DAC control value is set to this value (regarded as an unsigned integer value); otherwise, the holdover average DAC value is summed by this value (regarded as twos complement coded signed integer value) | |
| 0x0018 | [7:4] | Reserved | | Reserved | RW |
| | 3 | ADC tracking disable | | Disable ADC tracking; use DAC hold word | |
| | 2 | Force DAC to holdover in quick mode | | Force DAC control value from DAC current value to computed DAC holdover value immediately, not gradually | |
| | [1:0] | Holdover BW Reduction[1:0] | | Reduce tracking BW | |

Table 38. PLL1 LOS Mode Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|----------------------------|----------|--|--------|
| 0x0019 | [7:2] | Reserved | | Reserved | RW |
| | 1 | LOS bypass input prescaler | | Bypass LCM R divider cascade; the R1 input is the selected CLKINx/CLKINx input | |
| | 0 | LOS uses VCXO prescaler | | For very low PFD rates; cascades VCXO LCM divider after N1 | |

Table 39. PLL1 Charge Pump Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|----------------------|----------|--------------------------|--------|
| 0x001A | [7:4] | Reserved | | Reserved | RW |
| | [3:0] | PLL1 CP Current[3:0] | | PLL1 charge pump current | |

Table 40. PLL1 PFD Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|----------------------|----------|--|--------|
| 0x001B | [7:5] | Reserved | | Reserved | RW |
| | 4 | PLL1 PFD up enable | | Enable PLL1 PFD up | |
| | 3 | PLL1 PFD down enable | | Enable PLL1 PFD down | |
| | 2 | PLL1 PFD up force | | Force PLL1 charge pump up; do not assert simultaneously with PLL1 PFD down force | |
| | 1 | PLL1 PFD down force | | Force PLL1 charge pump down; do not assert simultaneously with PLL1 PFD up force | |
| | 0 | PLL1 PFD polarity | 0 1 | Select PFD polarity Positive Negative | |

Table 41. CLKINx/CLKINx and OSCIN/OSCIN Input Prescaler Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|------------------------------------|----------|--|--------|
| 0x001C | [7:0] | CLKIN0/CLKIN0 Input Prescaler[7:0] | | CLKIN0/CLKIN0 Prescaler divider setpoint | RW |
| 0x001D | [7:0] | CLKIN1/CLKIN1 Input Prescaler[7:0] | | CLKIN1/CLKIN1 Prescaler divider setpoint | RW |
| 0x001E | [7:0] | CLKIN2/CLKIN2 Input Prescaler[7:0] | | CLKIN2/CLKIN2 Prescaler divider setpoint | RW |
| 0x001F | [7:0] | CLKIN3/CLKIN3 Input Prescaler[7:0] | | CLKIN3/CLKIN3 Prescaler divider setpoint | RW |
| 0x0020 | [7:0] | OSCIN/OSCIN Input Prescaler[7:0] | | OSCIN/OSCIN Prescaler divider setpoint | RW |

Table 42. PLL1 Reference Divider Control (R1)

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-------------------------------|----------|--------------------------------|--------|
| 0x0021 | [7:0] | 16-Bit R1 Divider[7:0] (LSB) | | 16-bit R1 divider setpoint LSB | RW |
| 0x0022 | [7:0] | 16-Bit R1 Divider[15:8] (MSB) | | 16-bit R1 divider setpoint MSB | RW |

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Table 43. PLL1 Feedback Divider Control (N1)

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-------------------------------|----------|--------------------------------|--------|
| 0x0026 | [7:0] | 16-Bit N1 Divider[7:0] (LSB) | | 16-bit N1 divider setpoint LSB | RW |
| 0x0027 | [7:0] | 16-Bit N1 Divider[15:8] (MSB) | | 16-bit N1 divider setpoint MSB | RW |

Table 44. PLL1 Lock Detect Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-----------------------------|----------|---|--------|
| 0x0028 | [7:6] | Reserved | | Reserved | RW |
| | 5 | PLL1 lock detect uses slip | | Use the slip indicator instead of ~2 ns timer for lock detect | |
| | [4:0] | PLL1 Lock Detect Timer[4:0] | | PLL1 lock detect center depth (LCMs); increments of 2 ^{PLL1 Lock Detect Timer[4:0]} cycles | |
| | | | 00000 | 1 cycle | |
| | | | 00001 | 2 cycles | |
| | | | 00010 | 4 cycles | |
| | | | ... | ... | |
| | | | 11110 | 1,073,741,824 cycles | |
| | | | 11111 | 2,147,483,648 cycles | |

Table 45. PLL1 Reference Switching Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--------------------------------------|----------|--|--------|
| 0x0029 | [7:6] | Reserved | | Reserved | RW |
| | 5 | Bypass debouncer | | Bypass the debouncer in manual mode and GPI clock/holdover selection | |
| | [4:3] | Manual Mode Reference Switching[1:0] | | If automode REF switching = 0, manual selection of CLKINx/CLKINx input | |
| | 2 | Holdover uses DAC | 0 | In holdover, selects whether PLL1 uses the DAC or tristates the charge pump | |
| | | | 1 | Tristate the charge pump | |
| | 1 | Autorevertive reference switching | | Revert to PLL1 best clock option if it becomes available again | |
| | 0 | Automode reference switching | | Clock switching is automatic based on LOS/PLL1 reference priority control register (Register 0x0014) | |

Table 46. PLL1 Holdoff Time Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--------------------|----------|---|--------|
| 0x002A | [7:0] | Holdoff Timer[7:0] | | PLL1 waits in holdover for 2 ^{Holdoff Timer[7:0]} LCM cycles to give the abandoned reference a chance to recover before switching to the next priority clock. If Holdoff Timer[7:0] equals to 0, holdoff functionality is disabled and switches directly to the next priority clock. | RW |

PLL2 (Register 0x0031 to Register 0x003C)

Table 47. PLL2 Miscellaneous Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|----------|----------|-------------|--------|
| 0x0031 | [7:0] | Reserved | | Reserved | RW |
| 0x003C | [7:0] | Reserved | | Reserved | RW |

Table 48. PLL2 Frequency Doubler Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--------------------------|----------|--|--------|
| 0x0032 | [7:1] | Reserved | | Reserved | RW |
| | 0 | Bypass frequency doubler | 0 | Bypass PLL2 frequency doubler | |
| | | | 1 | Enable frequency doubler before R2 divider | |
| | | | | Bypass frequency doubler | |

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Table 49. PLL2 Reference Divider Control (R2)

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-------------------------------|----------|--|--------|
| 0x0033 | [7:0] | 12-Bit R2 Divider[7:0] (LSB) | | 12-bit R2 divider setpoint LSB. Divide by 1 to divide by 4095. 00000000, 00000001 = divide by 1. | RW |
| 0x0034 | [7:4] | Reserved | | Reserved. | RW |
| | [3:0] | 12-Bit R2 Divider[11:8] (MSB) | | 12-Bits R2 divider setpoint MSB. | |

Table 50. PLL2 Feedback Divider Control (N2)

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-------------------------------|----------|---------------------------------|--------|
| 0x0035 | [7:0] | 16-Bit N2 Divider[7:0] (LSB) | | 16-bit N2 divider setpoint LSB. | RW |
| 0x0036 | [7:0] | 16-Bit N2 Divider[15:8] (MSB) | | 16-bit N2 divider setpoint MSB. | RW |

Table 51. PLL2 Charge Pump Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|----------------------|----------|---|--------|
| 0x0037 | [7:4] | Reserved | | Reserved. | RW |
| | [3:0] | PLL2 CP Current[3:0] | | These 4 bits set the magnitude of PLL2 charge pump current. Granularity is ~160 μ A with full magnitude of ~2560 μ A. | |

Table 52. PLL2 PFD Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|----------------------|----------|--|--------|
| 0x0038 | [7:5] | Reserved | | Reserved | RW |
| | 4 | PLL2 PFD up enable | | Enable PLL2 PFD up | |
| | 3 | PLL2 PFD down enable | | Enable PLL2 PFD down | |
| | 2 | PLL2 PFD up force | | Force PLL2 charge pump up; do not assert simultaneously with PLL2 PFD down force | |
| | 1 | PLL2 PFD down force | | Force PLL2 charge pump down; do not assert simultaneously with PLL2 PFD up force | |
| | 0 | PLL2 PFD polarity | 0 1 | Select PFD polarity Positive Negative | |

Table 53. OSCOUTx/OSCOUTx Path Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|------------------------------|----------|---|--------|
| 0x0039 | [7:3] | Reserved | | Reserved | RW |
| | [2:1] | OSCOUTx/OSCOUTx Divider[1:0] | | Oscillator output divider ratio | |
| | | | 00 | Divided by 1 | |
| | | | 01 | Divided by 2 | |
| | | | 10 | Divided by 4 | |
| | | | 11 | Divided by 8 | |
| | 0 | OSCOUTx/OSCOUTx path enable | | Enable the oscillator output path (divider and the internal path except driver) | |

Table 54. OSCOUTx/OSCOUTx Driver Control

| Address | Bits | Bit Name | Settings ¹ | Description | Access |
|----------------|-------|---------------------------------------|-----------------------|---|--------|
| 0x003A, 0x003B | [7:6] | Reserved | | Reserved | RW |
| | [5:4] | OSCOUTx/OSCOUTx Driver Mode[1:0] | | Oscillator output driver mode selection | |
| | | | 00 | CML mode | |
| | | | 01 | LVPECL mode | |
| | | | 10 | LVDS mode | |
| | | | 11 | CMOS mode | |
| | [3] | Reserved | | Reserved | |
| | [2:1] | OSCOUTx/OSCOUTx Driver Impedance[1:0] | | Oscillator output driver impedance selection for CML mode | |

CONTROL REGISTERS

Table 54. OSCOUTx/OSCOUTx Driver Control (Continued)

| Address | Bits | Bit Name | Settings ¹ | Description | Access |
|---------|------|-------------------------------|-----------------------|--|--------|
| | | | 00 | Internal resistor disable | |
| | | | 01 | Internal 100 Ω resistor enable per output pin | |
| | | | 10 | Reserved | |
| | | | 11 | Internal 50 Ω resistor enable per output pin | |
| | 0 | OSCOUTx/OSCOUTx driver enable | | Enable oscillator driver | |

¹ X means don't care.

GPIO/SDATA Control (Register 0x0046 to Register 0x0054)

Table 55. GP1x Control

| Address | Bits | Bit Name | Settings | Description | Access |
|--------------------------------|-------|---------------------|--|--|--------|
| 0x0046, 0x0047, 0x0048, 0x0049 | [7:5] | Reserved | | Reserved. | RW |
| | [4:1] | GP1x Selection[3:0] | 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 | Select the GP1x functionality. Reserved. Force PLL1 to holdover. Select PLL1 reference manually, Bit 1. Select PLL1 reference manually, Bit 0. Put the chip into sleep mode. Issue a mute. Select the internal VCO type manually. Reserved Issue a pulse generator request. Issue a reseed request. Issue a restart request. Force the chip into fanout mode. Reserved. Issue a slip request Reserved. Reserved. | |
| | 0 | GP1x enable | | GP1x function enable. Before changing the function of the pin, disable it first, and then reenable it after the function change. ¹ | |

¹ Note that it is possible to have a GPIOx pin configured as both an output and an input.

Table 56. GPOx Control

| Address | Bits | Bit Name | Settings | Description | Access |
|--------------------------------|-------|---------------------|--|---|--------|
| 0x0050, 0x0051, 0x0052, 0x0053 | [7:2] | GPOx Selection[5:0] | 000000 000001 000010 000011 000100 000101 000110 000111 001000 001001 001010 | Select the GPOx functionality Alarm signal SDATA from SPI communication CLKIN3/CLKIN3 LOS for CLKIN3/CLKIN3 input CLKIN2/CLKIN2 LOS for CLKIN2/CLKIN2 input CLKIN1/CLKIN1 LOS for CLKIN1/CLKIN1 input CLKIN0/CLKIN0 LOS for CLKIN0/CLKIN0 input PLL1 holdover enabled signal from PLL1 Lock detect signal from PLL1 Acquiring lock signal from PLL1 PLL1 near lock acquisition status signal from PLL1 PLL2 lock detect signal from PLL2 | RW |

CONTROL REGISTERS

Table 56. GPOx Control (Continued)

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|------|----------|----------|---|--------|
| | | | 001011 | SYSREF sync status has not synchronized since reset | |
| | | | 001100 | Clock outputs phase status | |
| | | | 001101 | PLL1 and PLL2 lock detect is locked | |
| | | | 001110 | Sync request status signal | |
| | | | 001111 | PLL1 active CLKIN0/ $\overline{\text{CLKIN0}}$ | |
| | | | 010000 | PLL1 active CLKIN1/ $\overline{\text{CLKIN1}}$ | |
| | | | 010001 | PLL1 holdover ADC input range status | |
| | | | 010010 | PLL1 holdover ADC input status | |
| | | | 010011 | PLL1 VCXO status | |
| | | | 010100 | PLL1 active CLKINx/ $\overline{\text{CLKINx}}$ status | |
| | | | 010101 | PLL1 FSM state, Bit 0 | |
| | | | 010110 | PLL1 FSM state, Bit 1 | |
| | | | 010111 | PLL1 FSM state, Bit 2 | |
| | | | 011000 | PLL1 holdover exit phase, Bit 0 | |
| | | | 011001 | PLL1 holdover exit phase, Bit 1 | |
| | | | 011010 | Channel outputs FSM busy | |
| | | | 011011 | SYSREF FSM state, Bit 0 | |
| | | | 011100 | SYSREF FSM state, Bit 1 | |
| | | | 011101 | SYSREF FSM state, Bit 2 | |
| | | | 011110 | SYSREF FSM state, Bit 3 | |
| | | | 011111 | Force Logic 1 to GPO | |
| | | | 100000 | Force Logic 0 to GPO | |
| | | | 100001 | Reserved | |
| | | | 100010 | Reserved | |
| | | | 100011 | Reserved | |
| | | | 100100 | Reserved | |
| | | | 100101 | Reserved | |
| | | | 100110 | Reserved | |
| | | | 100111 | PLL1 holdover DAC averaged value, Bit 0 | |
| | | | 101000 | PLL1 holdover DAC averaged value, Bit 1 | |
| | | | 101001 | PLL1 holdover DAC averaged value, Bit 2 | |
| | | | 101010 | PLL1 holdover DAC averaged value, Bit 3 | |
| | | | 101011 | PLL1 holdover DAC current value, Bit 0 | |
| | | | 101100 | PLL1 holdover DAC current value, Bit 1 | |
| | | | 101101 | PLL1 holdover DAC current value, Bit 2 | |
| | | | 101110 | PLL1 holdover DAC current value, Bit 3 | |
| | | | 101111 | Reserved | |
| | | | 110000 | Reserved | |
| | | | 110001 | Reserved | |
| | | | 110010 | Reserved | |
| | | | 110011 | Reserved | |
| | | | 110100 | Reserved | |
| | | | 110101 | Reserved | |
| | | | 110110 | Reserved | |
| | | | 110111 | Reserved | |
| | | | 111000 | Reserved | |
| | | | 111001 | Reserved | |
| | | | 111010 | Reserved | |
| | | | 111011 | Reserved | |

CONTROL REGISTERS

Table 56. GPOx Control (Continued)

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|------|-------------|----------|---------------------------------------|--------|
| | | | 111100 | Reserved | |
| | | | 111101 | Holdover comparator status | |
| | | | 111110 | Pulse generator request status signal | |
| | | | 111111 | Reserved | |
| | 1 | GPOx mode | 0 | Selects the mode of GPOx driver | |
| | | | 1 | Open-drain mode CMOS mode | |
| | 0 | GPOx enable | | GPOx driver enable | |

Table 57. SDATA Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--------------|----------|----------------------------------|--------|
| 0x0054 | [7:2] | Reserved | | Reserved | RW |
| | 1 | SDATA mode | 0 | Selects the mode of SDATA driver | |
| | | | 1 | Open-drain mode CMOS mode | |
| | 0 | SDATA enable | | SDATA driver enable | |

SYSREF/SYNC Control (Register 0x005A to Register 0x005E)

Table 58. Pulse Generator Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-------------------------------------|----------|--|--------|
| 0x005A | [7:3] | Reserved | | Reserved. | RW |
| | [2:0] | Pulse Generator Mode Selection[2:0] | | SYSREF output enable with pulse generator. | |
| | | | 000 | Level sensitive. When the GPIx is configured to issue a pulse generator request (GPIx Selection[3:0] = 1000), or a pulse generator request is issued through the SPI or as a SYNC pin-based pulse generator, run the pulse generator. Otherwise, stop the pulse generator. | |
| | | | 001 | 1 pulse. ¹ | |
| | | | 010 | 2 pulses. ¹ | |
| | | | 011 | 4 pulses. ¹ | |
| | | | 100 | 8 pulses. ¹ | |
| | | | 101 | 16 pulses. ¹ | |
| | | | 110 | 16 pulses. ¹ | |
| | | | 111 | Continuous mode (50% duty cycle). ² | |

¹ Only LVPECL and CML buffer modes support N-Pulse SYSREF operation. When using N-Pulse SYSREF generation, refer to the [Clock Output Network](#) section.

² For continuous SYSREF generation, using an asynchronous start-up mode results in lower power consumption than compared to adynamic start-up mode with a continuous SYSREF mode.

Table 59. SYNC Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-------------------|----------|---|--------|
| 0x005B | [7:3] | Reserved | | Reserved | RW |
| | 2 | SYNC retime | 0 | Bypass the retime (if using SYNC path with on-chip VCO) | |
| | | | 1 | Retime the external SYNC from Reference 0 | |
| | 1 | SYNC through PLL2 | | Allow a reseed event to be through PLL2 | |
| | 0 | SYNC polarity | | SYNC polarity (must be 0 if not using CLKIN0/CLKIN0 as the input) | |
| | | | 0 | Positive | |
| | | | 1 | Negative | |

CONTROL REGISTERS

Table 60. SYSREF Timer Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--------------------------|----------|--|--------|
| 0x005C | [7:0] | SYSREF Timer[7:0] (LSB) | | 12-bit SYSREF timer setpoint LSB. This sets the internal beat frequency of the timer, which controls synchronization and pulse generator events. Set the 12-bit timer to a submultiple of the lowest output SYSREF frequency, and program it to be no faster than 4 MHz. | RW |
| 0x005D | [7:4] | Reserved | | Reserved. | RW |
| | [3:0] | SYSREF Timer[11:8] (MSB) | | 12-bit SYSREF timer setpoint MSB. | |

Table 61. SYSREF Miscellaneous Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|----------|----------|-------------|--------|
| 0x005E | [7:0] | Reserved | | Reserved | RW |

Clock Distribution Network (Register 0x0064 to Register 0x0065)

Table 62. External VCO Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|------------------------------------|----------|---|--------|
| 0x0064 | [7:2] | Reserved | | Reserved | RW |
| | 1 | Divide by 2 on external VCO enable | | Use divide by 2 on external VCO path | |
| | 0 | Low frequency external VCO path | | Changes bias to Class A for low frequency VCO | |

Table 63. Analog Delay Common Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-----------------------------|----------|--|--------|
| 0x0065 | [7:1] | Reserved | | Reserved. | RW |
| | 0 | Analog delay low power mode | | Analog delay is in low power mode, which can save power for low settings of analog delay, but is not glitchless between setpoints. | |

Alarm Masks Registers (Register 0x0070 to Register 0x0071)

Table 64. PLL1 Alarm Mask Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-------------------------------------|----------|---|--------|
| 0x0070 | 7 | PLL1 near lock mask | | If set, allow the PLL1 near lock signal to generate alarm signal | RW |
| | 6 | PLL1 lock acquisition mask | | If set, allow the PLL1 lock acquisition signal to generate alarm signal | |
| | 5 | PLL1 lock detect mask | | If set, allow the PLL1 lock detect signal to generate alarm signal | |
| | 4 | PLL1 holdover status mask | | If set, allow the PLL1 holdover status signal to generate alarm signal | |
| | [3:0] | PLL1 CLKINx/CLKINx Status Mask[3:0] | Bit 0 | If set, allow CLKIN0/CLKIN0 \bar LOS to generate alarm signal | |
| | | | Bit 1 | If set, allow CLKIN1/CLKIN1 \bar LOS to generate alarm signal | |
| | | | Bit 2 | If set, allow CLKIN2/CLKIN2 \bar LOS to generate alarm signal | |
| | | | Bit 3 | If set, allow CLKIN3/CLKIN3 \bar LOS to generate alarm signal | |

Table 65. Alarm Mask Control

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|----------------------------------|----------|---|--------|
| 0x0071 | [7:5] | Reserved | | Reserved | RW |
| | 4 | Sync request mask | | If set, allow the sync request signals to generate alarm signal | |
| | 3 | PLL1 and PLL2 lock detect mask | | If set, allow the PLL1 and PLL2 lock detect signals to generate alarm signal | |
| | 2 | Clock outputs phases status mask | | If set, allow the clock outputs phases status signal to generate alarm signal | |
| | 1 | SYSREF sync status mask | | If set, allow the SYSREF sync status signal to generate alarm signal | |
| | 0 | PLL2 lock detect mask | | If set, allow the PLL2 lock detect signal to generate alarm signal | |

CONTROL REGISTERS

Product ID Registers (Register 0x0078 to Register 0x007A)

Table 66. Product ID

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-------------------------------|----------|-----------------------------------|--------|
| 0x0078 | [7:0] | Product ID Value[7:0] (LSB) | | 24-bit product ID value low | R |
| 0x0079 | [7:0] | Product ID Value[15:8] (Mid) | | 24-bit product ID value high | R |
| 0x007A | [7:0] | Product ID Value[23:16] (MSB) | | 24-bit product ID value very high | R |

Alarm Readback Status Registers (Register 0x007B to Register 0x007F)

Table 67. Readback Register

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--------------|----------|---------------------------------|--------|
| 0x007B | [7:1] | Reserved | | Reserved. | R |
| | 0 | Alarm signal | | Readback alarm status from SPI. | |

Table 68. PLL1 Alarm Readback

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|------------------------|----------|--|--------|
| 0x007C | 7 | PLL1 near lock | | PLL1 near locked. Declare near locked when the counter reaches 1/16 of the programmable limit. | R |
| | 6 | PLL1 lock acquisition | | PLL1 acquiring lock. | |
| | 5 | PLL1 lock detect | | PLL1 locked. | |
| | 4 | PLL1 holdover status | | PLL1 in holdover. | |
| | [3:0] | CLKINx/CLKINx LOS[3:0] | Bit 0 | CLKIN0/CLKIN0 LOS. | |
| | | | Bit 1 | CLKIN1/CLKIN1 LOS. | |
| | | | Bit 2 | CLKIN2/CLKIN2 LOS. | |
| | | | Bit 3 | CLKIN3/CLKIN3 LOS. | |

Table 69. Alarm Readback

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-----------------------------|----------|---|--------|
| 0x007D | [7:5] | Reserved | | Reserved. | R |
| | 4 | Sync request status | | PLL2 locked (or disabled), but unsynchronized. | |
| | 3 | PLL1 and PLL2 lock detect | | PLL1 and PLL2 lock detect status. | |
| | | | 0 | Either PLL1 or PLL2 is not locked or both PLL1 and PLL2 are not locked. | |
| | | | 1 | PLL1 and PLL2 are locked. | |
| | 2 | Clock outputs phases status | | SYSREF alarm. | |
| | | | 0 | SYSREF of the HMC7044 is not valid; that is, its phase output is not stable. | |
| | | | 1 | SYSREF of the HMC7044 is valid and locked; that is, its phase output is stable. | |
| | 1 | SYSREF sync status | | SYSREF SYNC status alarm. | |
| | | | 0 | The HMC7044 has been synchronized with an external sync pulse or a sync request from the SPI. | |
| | 0 | PLL2 lock detect | 1 | The HMC7044 never synchronized with an external sync pulse or a sync request from the SPI. | |
| | | | | PLL2 near locked. Declare near locked when counter reaches 1/16 of the programmable limit. | |

Table 70. Latched Alarm Readback

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|------|-------------------------------|----------|--|--------|
| 0x007E | 7 | Reserved | | Reserved. | R |
| | 6 | PLL2 lock acquisition latched | | Readback record of PLL2 lock acquisition since the last clear event. | |
| | 5 | PLL1 lock acquisition latched | | Readback record of PLL1 lock acquisition since the last clear event. | |
| | 4 | PLL1 holdover latched | | Readback record of PLL1 holdover since the last clear event. | |

CONTROL REGISTERS

Table 70. Latched Alarm Readback (Continued)

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--------------------------------|----------|--|--------|
| | [3:0] | CLKINx/CLKINx LOS Latched[3:0] | Bit 0 | Readback record of CLKIN0/CLKIN0 LOS since the last clear event. | |
| | | | Bit 1 | Readback record of CLKIN1/CLKIN1 LOS since the last clear event. | |
| | | | Bit 2 | Readback record of CLKIN2/CLKIN2 LOS since the last clear event. | |
| | | | Bit 3 | Readback record of CLKIN3/CLKIN3 LOS since the last clear event. | |

Table 71. Alarm Readback Miscellaneous

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|----------|----------|-------------|--------|
| 0x007F | [7:0] | Reserved | | Reserved. | R |

PLL1 Status Registers (Register 0x0082 to Register 0x0087)

Table 72. PLL1 Status Registers

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--------------------------------------|----------|--|--------|
| 0x0082 | 7 | Reserved | | Reserved | R |
| | [6:5] | PLL1 Best Clock[1:0] | | Indicates which clock the LOS/priority encoder prefers if automode reference switching is used | |
| | [4:3] | PLL1 Active CLKINx/CLKINx [1:0] | | Indicates which CLKINx/CLKINx input is currently in use | |
| | [2:0] | PLL1 FSM State[2:0] | | Sets the state PLL1 is in | |
| | | | 000 | Reset | |
| | | | 001 | Acquisition | |
| | | | 010 | Locked | |
| | | | 011 | Invalid | |
| | | | 100 | Holdover | |
| | | | 101 | DAC assisted holdover exit | |
| 0x0083 | 7 | Reserved | | Reserved | R |
| | [6:0] | Holdover DAC Averaged Value[6:0] | | Average DAC code | |
| 0x0084 | 7 | Holdover comparator value | | Holdover comparator output value (DAC output vs. PLL1 V _{TUNE}) | R |
| | [6:0] | Holdover DAC Current Value[6:0] | | Current DAC code | |
| 0x0085 | [7:4] | Reserved | | Reserved | R |
| | 3 | PLL1 active CLKINx/CLKINx LOS | | LOS of the currently active reference | |
| | 2 | PLL1 VCXO status | | Indicates whether any of the enabled references appears to run faster than the VCXO | |
| | 1 | PLL1 holdover ADC status | 0 | ADC is acquiring | |
| | | | 1 | PLL1 V _{TUNE} is moving quickly | |
| | 0 | PLL1 holdover ADC input range status | 0 | PLL1 V _{TUNE} is in range | |
| | | | 1 | PLL1 V _{TUNE} is out of range | |
| | | | | | |
| 0x0086 | [7:5] | Reserved | | Reserved | R |
| | [4:3] | PLL1 Holdover Exit Phase[1:0] | | The phase of the PLL1 holdover exit | |
| | [2:0] | Reserved | | Reserved | |
| 0x0087 | [7:0] | Reserved | | Reserved | R |

PLL2 Status Registers (Register 0x008C to Register 0x0090)

Table 73. PLL2 Status Registers

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|---------------------|----------|--|--------|
| 0x008C | [7:0] | PLL2 autotune value | | After autotune, this word is populated with the selected capacitor bank of the VCO | R |

CONTROL REGISTERS

Table 73. PLL2 Status Registers (Continued)

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--|----------|--|--------|
| 0x008D | [7:0] | PLL2 Autotune Signed Error[7:0] (LSB) | | 14-bit PLL2 V _{TUNE} error count, LSB | R |
| 0x008E | 7 | PLL2 autotune status | 1 | Autotune busy | R |
| | | | 0 | Done/not working | |
| | 6 | PLL2 autotune error sign | | Sign of PLL2 autotune error | |
| | | | 0 | Positive | |
| | | | 1 | Negative | |
| | [5:0] | PLL2 Autotune Signed Error[13:8] (MSB) | | 14-bit PLL2 V _{TUNE} error count, MSB | |
| 0x008F | [7:4] | PLL2 Autotune FSM State[3:0] | | Autotune FSM state | R |
| | | | 0000 | Idle | |
| | | | 0001 | Startup | |
| | | | 0010 | Startup | |
| | | | 0011 | Reset | |
| | | | 0100 | Reset | |
| | | | 0101 | Reset | |
| | | | 0110 | Measure | |
| | | | 0111 | Wait | |
| | | | 1000 | Wait | |
| | | | 1001 | Update loop to state 18 times | |
| | | | 1010 | Round | |
| | | | 1011 | Finish | |
| | [3:0] | PLL2 SYNC FSM State[3:0] | | PLL2 sync carry FSM state | |
| | | | 0000 | Idle | |
| | | | 0100 | Power up Section A of the FSM | |
| | | | 0110 | Power up Section B of the FSM | |
| | | | 0111 | Sending to N2 | |
| | | | 1110 | Power down Section A of the FSM | |
| | | | 1100 | Power down Section B of the FSM | |
| 0x0090 | [7:0] | Reserved | | Reserved | R |

SYSREF Status Register (Register 0x0091)

Table 74. SYSREF Status Register

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|--------------------------|----------|---|--------|
| 0x0091 | [7:5] | Reserved | | Reserved. | R |
| | 4 | Channel outputs FSM busy | | One of clock outputs FSM requested clock, and it is running. | |
| | [3:0] | SYSREF FSM State[3:0] | | Indicates the current step of the SYSREF reseed process. Note that the three different progressions are caused by different trigger events (reseed, pulse generator, reserved). | |
| | | | 0000 | Reset. | |
| | | | 0010 | Done. | |
| | | | 0100 | Get ready. | |
| | | | 0101 | Get ready. | |
| | | | 0110 | Get ready. | |
| | | | 1010 | Running (pulse generator). | |
| | | | 1011 | Start. | |
| | | | 1100 | Power up. | |

CONTROL REGISTERS

Table 74. SYSREF Status Register (Continued)

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|------|----------|----------|--------------|--------|
| | | | 1101 | Power up. | |
| | | | 1110 | Power up. | |
| | | | 1111 | Clear reset. | |

Other Controls (Register 0x0096 to Register 0x00B8)

For optimum performance of the chip, Register 0x009F, Register 0x00A0, Register 0x00A5, Register 0x00A8, and Register 0x00B0 must be programmed to a different value than their default value (with the values given in the description).

Table 75. Reserved Registers

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|----------|----------|---|--------|
| 0x0096 | [7:0] | Reserved | | Reserved | RW |
| 0x0097 | [7:0] | Reserved | | Reserved | RW |
| 0x0098 | [7:0] | Reserved | | Reserved | RW |
| 0x0099 | [7:0] | Reserved | | Reserved | RW |
| 0x009A | [7:0] | Reserved | | Reserved | RW |
| 0x009B | [7:0] | Reserved | | Reserved | RW |
| 0x009B | [7:0] | Reserved | | Reserved | RW |
| 0x009C | [7:0] | Reserved | | Reserved | RW |
| 0x009D | [7:0] | Reserved | | Reserved | RW |
| 0x009E | [7:0] | Reserved | | Reserved | RW |
| 0x009F | [7:0] | Reserved | | Clock output driver low power setting (set to 0x4D instead of default value) | RW |
| 0x00A0 | [7:0] | Reserved | | Clock output driver high power setting (set to 0xDF instead of default value) | RW |
| 0x00A1 | [7:0] | Reserved | | Reserved | RW |
| 0x00A2 | [7:0] | Reserved | | Reserved | RW |
| 0x00A3 | [7:0] | Reserved | | Reserved | RW |
| 0x00A4 | [7:0] | Reserved | | Reserved | RW |
| 0x00A5 | [7:0] | Reserved | | PLL1 more delay (PFD1, lock detect) (set to 0x06 instead of default value) | RW |
| 0x00A6 | [7:0] | Reserved | | Reserved | RW |
| 0x00A7 | [7:0] | Reserved | | Reserved | RW |
| 0x00A8 | [7:0] | Reserved | | PLL1 holdover DAC g_m setting (set to 0x06 instead of default value) | RW |
| 0x00A9 | [7:0] | Reserved | | Reserved | RW |
| 0x00AB | [7:0] | Reserved | | Reserved | RW |
| 0x00AC | [7:0] | Reserved | | Reserved | RW |
| 0x00AD | [7:0] | Reserved | | Reserved | RW |
| 0x00AE | [7:0] | Reserved | | Reserved | RW |
| 0x00AF | [7:0] | Reserved | | Reserved | RW |
| 0x00B0 | [7:0] | Reserved | | V _{TUNE} preset setting (set to 0x04 instead of default value) | RW |
| 0x00B1 | [7:0] | Reserved | | Reserved | RW |
| 0x00B2 | [7:0] | Reserved | | Table 76 | RW |
| 0x00B3 | [7:0] | Reserved | | Reserved | RW |
| 0x00B4 | [7:0] | Reserved | | Reserved | RW |
| 0x00B5 | [7:0] | Reserved | | Reserved | RW |
| 0x00B6 | [7:0] | Reserved | | Reserved | RW |
| 0x00B7 | [7:0] | Reserved | | Reserved | RW |
| 0x00B8 | [7:0] | Reserved | | Reserved | RW |

CONTROL REGISTERS

Manual VCO Calibration (Register 0x00B2)

The bit descriptions in Table 76 are used for manual capacitor bank selection for PLL2. Capacitor bank value that is selected by autocalibration can be read back with Register 0x008C and the value can be used later for manual VCO calibration. To set capacitor bank manually, enable Register 0x00B2[0] and set the capacitor value to Register 0x00B2[6:2].

Table 76. Manual Capacitor Bank Selection Register

| Address | Bits | Bit Name | Settings | Description | Access |
|---------|-------|-----------------------------------|----------|---|--------|
| 0x00B2 | 7 | Reserved | | Reserved | RW |
| | [6:2] | Forced Capacitor Value | | 5-bit capacitor bank value | |
| | 1 | Reserved | | Reserved | |
| | 0 | Enable Manual Capacitor Selection | | Enable capacitor bank selection from SPI 0: Disable 1: Enable | |

Clock Distribution (Register 0x00C8 to Register 0x0153)

The bit descriptions in Table 77 apply to all 14 channels.

Table 77. Channel 0 to Channel 13 Control

| Address | Bits | Bit Name | Settings ¹ | Description | Access |
|--|-------|------------------------------------|-----------------------|---|--------|
| 0x00C8, 0x00D2, 0x00DC, 0x00E6, 0x00F0, 0x00FA, 0x0104, 0x010E, 0x0118, 0x0122, 0x012C, 0x0136, 0x0140, 0x014A | 7 | High performance mode | | High performance mode. Adjusts the divider and buffer bias to improve swing/phase noise at the expense of power. | RW |
| | 6 | SYNC enable | | Susceptible to SYNC event. The channel can process a SYNC event to reset its phase. | |
| | 5 | Slip enable | | Susceptible to slip event. The channel can process a slip request from SPI or GPI. Note that if slip enable is true but multislip is off, a channel slips by 1 VCO cycle on an explicit slip request broadcast from the SPI/GPI. | |
| | 4 | Reserved | | Reserved. | |
| | [3:2] | Start-Up Mode[1:0] | 00 01 10 11 | Configures the channel to normal mode with asynchronous startup, or to a pulse generator mode with dynamic start-up. Note that this must be set to asynchronous mode if the channel is unused. Asynchronous. Reserved. Reserved. Dynamic. | |
| | 1 | Multislip enable | 0 1 | Allow multislip operation (default = 0 for SYSREF, 1 for DCLK). Do not engage automatic multislip on channel startup. Multislip events after SYNC or pulse generator request, if slip enable, Bit = 1. | |
| | 0 | Channel enable | | Channel enable. If this bit is 0, channel is disabled. | |
| | [7:0] | 12-Bit Channel Divider[7:0] (LSB) | | 12-bit channel divider setpoint LSB. The divider supports even divide ratios from 2 to 4094. The supported odd divide ratios are 1, 3, and 5. All even and odd divide ratios have 50.0% duty cycle. | |
| 0x00CA, 0x00D4, 0x00DE, 0x00E8, 0x00F2, 0x00FC, 0x0106, 0x0110, 0x011A, 0x0124, 0x012E, 0x0138, 0x0142, 0x014C | [7:4] | Reserved | | Reserved. | RW |
| | [3:0] | 12-Bit Channel Divider[11:8] (MSB) | | 12-bit channel divider setpoint MSB. | |
| 0x00CB, 0x00D5, 0x00DF, 0x00E9, 0x00F3, 0x00FD, 0x0107, 0x0111, 0x011B, 0x0125, 0x012F, 0x0139, 0x0143, 0x014D | [7:5] | Reserved | | Reserved. | RW |
| | [4:0] | Fine Analog Delay[4:0] | | 24 fine delay steps. Step size = 25 ps. Values greater than 23 have no effect on analog delay. | |

CONTROL REGISTERS

Table 77. Channel 0 to Channel 13 Control (Continued)

| Address | Bits | Bit Name | Settings ¹ | Description | Access |
|---|-------------------------------------|---|--|---|--------|
| 0x00CC, 0x00D6, 0x00E0, 0x00EA, 0x00F4, 0x00FE, 0x0108, 0x0112, 0x011C, 0x0126, 0x0130, 0x013A, 0x0144, 0x014E | [7:5] [4:0] | Reserved Coarse Digital Delay[4:0] | | Reserved. 17 coarse delay steps. Step size = ½ VCO cycle. This flip flop (FF)-based digital delay does not increase noise level at the expense of power. Values greater than 17 have no effect on coarse delay. | RW |
| 0x00CD, 0x00D7, 0x00E1, 0x00EB, 0x00F5, 0x00FF, 0x0109, 0x0113, 0x011D, 0x0127, 0x0131, 0x013B, 0x0145, 0x014F | [7:0] | 12-Bit Multislip Digital Delay[7:0] (LSB) | | 12-bit multislip digital delay amount LSB. Step size = (delay amount: MSB + LSB) × VCO cycles. If multislip enable bit = 1, any slip events (caused by GPI, SPI, SYNC, or pulse generator events) repeat the number of times set by 12-Bit Multislip Digital Delay[11:0] to adjust the phase by step size. | RW |
| 0x00CE, 0x00D8, 0x00E2, 0x00EC, 0x00F6, 0x0100, 0x010A, 0x0114, 0x011E, 0x0128, 0x0132, 0x013C, 0x0146, 0x0150 | [7:4] [3:0] | Reserved 12-Bit Multislip Digital Delay[11:8] (MSB) | | Reserved. 12-bit multislip digital delay amount MSB. | RW |
| 0x00CF, 0x00D9, 0x00E3, 0x00ED, 0x00F7, 0x0101, 0x010B, 0x0115, 0x011F, 0x0129, 0x0133, 0x013D, 0x0147, 0x0151 | [7:2] [1:0] | Reserved Output Mux Selection[1:0] | 00 01 10 11 | Reserved. Channel output mux selection. Channel divider output. Analog delay output. Other channel of the clock group pair. Input VCO clock (fundamental). Fundamental can also be generated with 12-Bit Channel Divider[11:0] = 1. | RW |
| 0x00D0, 0x00DA, 0x00E4, 0x00EE, 0x00F8, 0x0102, 0x010C, 0x0116, 0x0120, 0x012A, 0x0134, 0x013E, 0x0148, 0x0152 | [7:6] 5 [4:3] [2] [1:0] | Force Mute[1:0] Dynamic driver enable Driver Mode[1:0] Reserved Driver Impedance[1:0] | 00 01 10 11 0 1 00 01 10 11 00 01 10 11 | Idle at Logic 0 selection (pulse generator mode only). Force to Logic 0 or V _{CM} . Normal mode (selection for DCLK). Reserved. Force to Logic 0. Reserved. Dynamic driver enable (pulse generator mode only). Driver is enabled/disabled with channel enable bit. Driver is dynamically disabled with pulse generator events. Output driver mode selection. CML mode. LVPECL mode. LVDS mode. CMOS mode. Reserved. Output driver impedance selection for CML mode. Output enable selection for CMOS mode. CML: internal resistor disable. CMOS: disable both output. CML: internal 100 Ω resistor enable per output pin. CMOS: enable Out_P. ² CML: reserved. CMOS: enable Out_N. ³ CML: internal 50 Ω resistor enable per output pin. CMOS: enable both output. | RW |
| 0x00D1, 0x00DB, 0x00E5, 0x00EF, 0x00F9, 0x0103, 0x010D, 0x0117, 0x0121, 0x012B, 0x0135, 0x013F, 0x0149, 0x0153 | [7:0] | Reserved | | Reserved. | RW |

CONTROL REGISTERS

¹ X means don't care.

² For Channel 0, Channel 3, Channel 5, Channel 6, Channel 9, Channel 10, and Channel 13, setting b'01 enables the OUT_N.

³ For Channel 0, Channel 3, Channel 5, Channel 6, Channel 9, Channel 10, and Channel 13, setting b'10 enables the OUT_P.

EVALUATION PCB SCHEMATIC

EVALUATION PCB

For the circuit board used in the application, use RF circuit design techniques. Ensure that signal lines have 50 Ω impedance. Connect the package ground leads and exposed pad directly to the ground plane (see Figure 55). Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board is available from Analog Devices upon request.

The typical Pb-free reflow solder profile is shown in Figure 54.

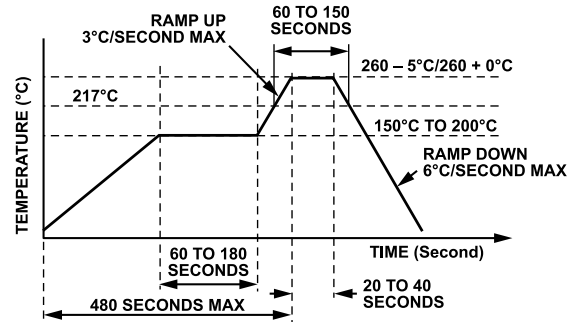


Figure 54. Pb-Free Reflow Solder Profile

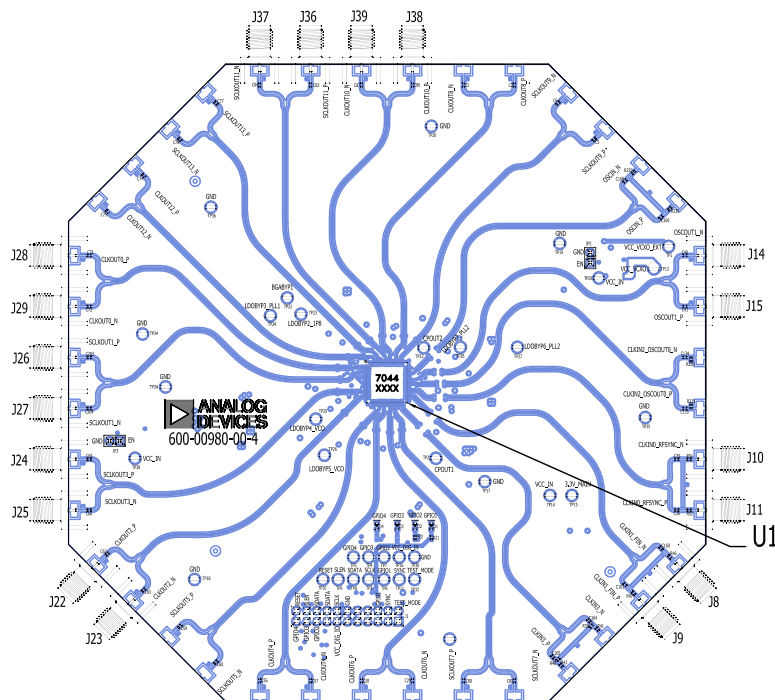


Figure 55. Evaluation PCB Layout, Top Side

EVALUATION PCB SCHEMATIC

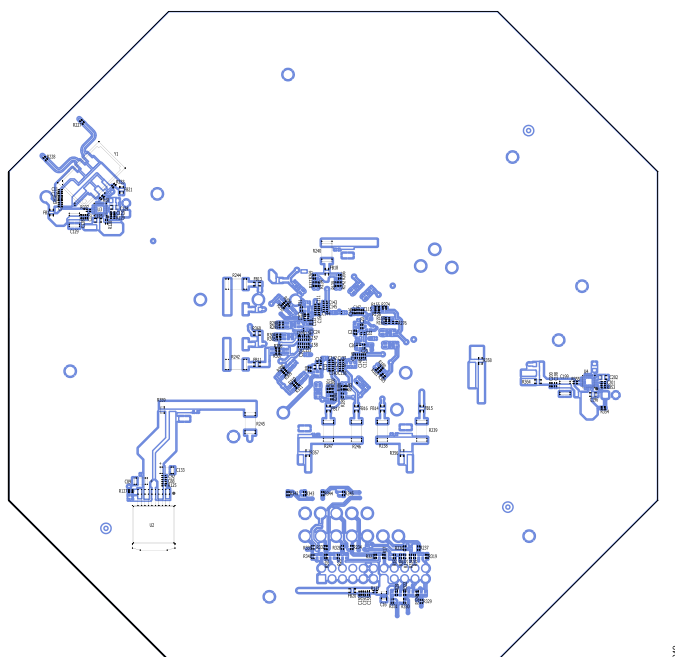


Figure 56. Evaluation PCB Layout, Bottom Side

OUTLINE DIMENSIONS

| Package Drawing (Option) | Package Type | Package Description |
|--------------------------|--------------|---------------------------------------|
| HCP-68-1 | LFCSP_VQ | 68-Lead Lead Frame Chip Scale Package |

For the latest package outline information and land patterns (footprints), go to [Package Index](#).

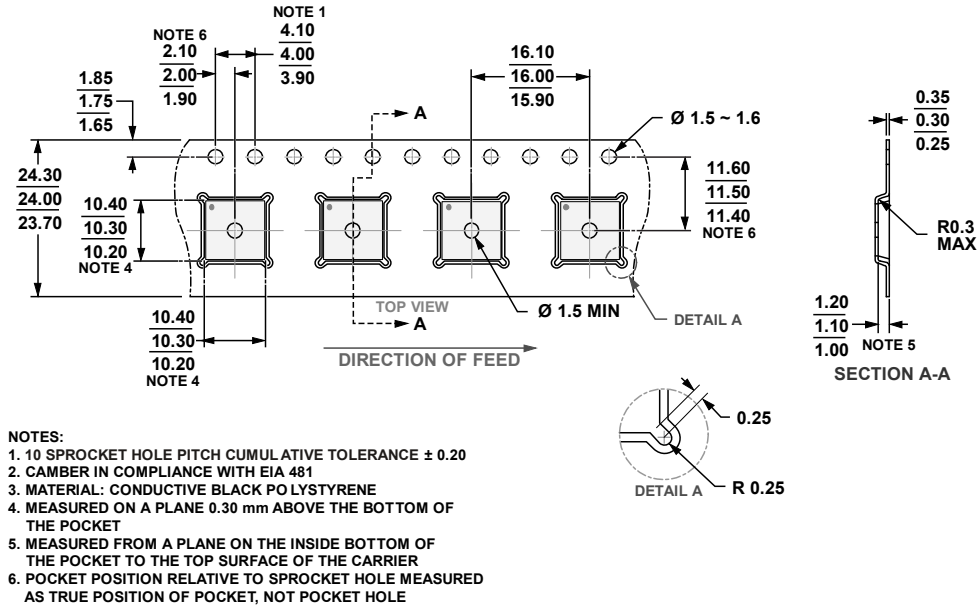


Figure 57. LFCSP Tape and Reel Outline Dimensions
Dimensions shown in millimeters

Updated: February 07, 2024

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Packing Quantity | Package Option |
|--------------------|-------------------|---------------------------------|------------------|----------------|
| HMC7044LP10BE | -40°C to +85°C | 68-Lead QFN (10mm x 10mm w/ EP) | Reel, 500 | HCP-68-1 |
| HMC7044LP10BETR | -40°C to +85°C | 68-Lead QFN (10mm x 10mm w/ EP) | Reel, 500 | HCP-68-1 |

¹ E = RoHS Compliant Part.

LEAD FINISH, MSL RATING, AND BRANDING OPTIONS

| Model ¹ | Lead Finish | MSL Rating | Branding ² |
|--------------------|----------------|------------|-----------------------|
| HMC7044LP10BE | 100% matte tin | MSL-3 | 7044 XXXX |
| HMC7044LP10BETR | 100% matte tin | MSL-3 | 7044 XXXX |

¹ E = RoHS Compliant Part.

² Four-digit lot number represented by XXXX.

OUTLINE DIMENSIONS

EVALUATION BOARDS

| Model ¹ | Description |
|--------------------|----------------|
| EK1HMC7044LP10B | Evaluation Kit |

¹ E = RoHS Compliant Part.