Data Sheet

ADL8107

GaAs, pHEMT, MMIC, Low Noise Amplifier, 6 GHz to 18 GHz

FEATURES

- Single positive supply (self biased)
- Gain: 24 dB typical at 7 GHz to 16 GHz
- OIP3: 29 dBm typical at 7 GHz to 16 GHz
- Noise figure: 1.3 dB typical at 7 GHz to 16 GHz
- 8-lead, 2 mm × 2 mm, LFCSP (see the Outline Dimensions section)

APPLICATIONS

- Test instrumentation
- Military communications
- Radar

GENERAL DESCRIPTION

The ADL8107 is a gallium arsenide (GaAs), monolithic microwave IC (MMIC), pseudomorphic high electron mobility transistor (pHEMT), low noise, wideband, high linearity amplifier that operates from 6 GHz to 18 GHz.

The ADL8107 provides a typical gain of 24 dB at 7 GHz to 16 GHz, a 1.3 dB typical noise figure at 7 GHz to 16 GHz, a 18.5 dBm typical output power for 1 dB compression (OP1dB) at 7 GHz to 16 GHz, and a typical output third-order intercept (OIP3) of 29 dBm at 7 GHz to 16 GHz, requiring only 90 mA from a 5 V drain supply voltage. This low noise amplifier has a high output second-order intercept (OIP2) of 30.5 dBm typical at 7 GHz to 16 GHz, making the ADL8107 suitable for military and test instrumentation applications.

The ADL8107 also features inputs and outputs that are internally matched to 50 Ω. The RFIN and RFOUT pins are internally ac-coupled, and the bias inductor is also integrated, making the ADL8107 ideal for surface-mounted technology (SMT)-based, high density applications.

The ADL8107 is housed in a RoHS-compliant, 2 mm × 2 mm, 8-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM

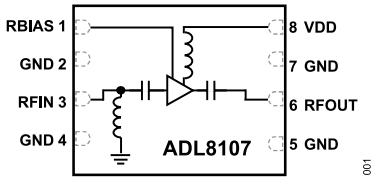

Figure 1.

Rev. C

DOCUMENT FEEDBACK

TECHNICAL SUPPORT

TABLE OF CONTENTS

REVISION HISTORY

10/2024—Rev. B to Rev. C

Changes to Figure 1 ... 1
Change to 6 GHz to 7 GHz Frequency Range Section ... 3
Change to 7 GHz to 16 GHz Frequency Range Section ... 3
Change to 16 GHz to 18 GHz Frequency Range Section ... 4
Changes to Table 8 ... 6
Changes to Figure 4 ... 6
Changes to Typical Performance Characteristics Section ... 7
Changes to Figure 78 ... 19
Changes to Applications Information Section and Figure 79 ... 20
Changes to Table 9 ... 20
Changes to Recommended Power Management Circuit Section, Table 10, and Figure 80 ... 21
Change to Figure 81 ... 22

8/2023—Rev. A to Rev. B

Deleted Figure 73, Figure 74, Figure 76, and Figure 77; Renumbered Sequentially ... 18
Added Figure 73 and Figure 76; Renumbered Sequentially ... 18

10/2022—Rev. 0 to Rev. A

Change to Using the RBIAS Pin to Enable and Disable ADL8107 Section ... 22

1/2022—Revision 0: Initial Version

SPECIFICATIONS

6 GHZ TO 7 GHZ FREQUENCY RANGE

VDD = 5 V, total supply current (I_{DQ}) = 90 mA, RBIAS = 7.15 kΩ, and T_{CASE} = 25°C, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	6		7	GHz	
GAIN	19.5	22.5		dB	
Gain Variation over Temperature		0.03		dB/°C	
NOISE FIGURE		1.9		dB	
RETURN LOSS					
Input		12		dB	
Output		13		dB	
OUTPUT					
OP1dB	15	18		dBm	
Saturated Output Power (P_{SAT})		19.5		dBm	
OIP3		28		dBm	Measurement taken at output power (P_{OUT}) per tone = 6 dBm
OIP2		27		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
POWER ADDED EFFICIENCY (PAE)		16		%	Measured at P_{SAT}

7 GHZ TO 16 GHZ FREQUENCY RANGE

VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ, and T_{CASE} = 25°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	7		16	GHz	
GAIN	21.5	24		dB	
Gain Variation over Temperature		0.048		dB/°C	
NOISE FIGURE		1.3		dB	
RETURN LOSS					
Input		12		dB	
Output		13.5		dB	
OUTPUT					
OP1dB	16.5	18.5		dBm	
Saturated Output Power (P_{SAT})		20		dBm	
OIP3		29		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
OIP2		30.5		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
POWER ADDED EFFICIENCY (PAE)		18		%	Measured at P_{SAT}

SPECIFICATIONS

16 GHZ TO 18 GHZ FREQUENCY RANGE

VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ, and T_{CASE} = 25°C, unless otherwise noted.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	16		18	GHz	
GAIN	18	20.5		dB	
Gain Variation over Temperature		0.046		dB/°C	
NOISE FIGURE		1.7		dB	
RETURN LOSS					
Input		8		dB	
Output		7		dB	
OUTPUT					
OP1dB	14	17		dBm	
Saturated Output Power (P_{SAT})		19		dBm	
OIP3		28.5		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
OIP2		33		dBm	Measurement taken at P_{OUT} per tone = 6 dBm
POWER ADDED EFFICIENCY (PAE)		12		%	Measured at P_{SAT}

DC SPECIFICATIONS

Table 4.

Parameter	Min	Typ	Max	Unit
SUPPLY CURRENT				
I_{DQ}		90		mA
Amplifier Current (I_{DQ_AMP})		89.4		mA
RBIAS Current (I_{RBIAS})		0.6		mA
SUPPLY VOLTAGE				
VDD	3	5	5.5	V

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
VDD	6 V
Continuous RF Input Power (RFIN)	22 dBm
Pulsed RFIN (Duty Cycle = 10%, Pulse Width = 100 µs)	24 dBm
Continuous Power Dissipation (P_{DISS}), T_{CASE} = 85°C (Derate 14.5 mW/°C Above 85°C)	1.3 W
Temperature	
Storage Range	−65°C to +150°C
Operating Range	−40°C to +85°C
Nominal Junction (T_{CASE} = 85°C, VDD = 5 V, I_{DQ} = 90 mA, Input Power (P_{IN}) = Off)	116°C
Maximum Junction	175°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Overall thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-8-30	69	°C/W

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

ESD Ratings for ADL8107

Table 7. ADL8107, 8-Lead LFCSP

ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

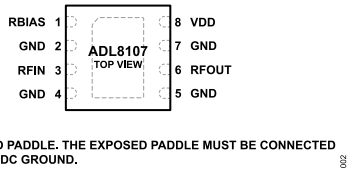

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	RBIAS	Bias Setting Resistor. Connect a resistor between RBIAS and VDD to set the I_{DQ}. See Figure 79 and Table 9 for more details. See Figure 3 for the interface schematic.
2, 4, 5, 7	GND	Ground. Connect the GND pins to a ground plane that has low electrical and thermal impedance. See Figure 6 for the interface schematic.
3	RFIN	RF Input. The RFIN pin has a DC path to ground followed by an AC-coupling capacitor in the RF signal path and matched to 50 Ω. When the DC bias level of the input signal is not equal to 0 V, externally AC-couple the RFIN pin. See Figure 4 for the interface schematic.
6	RFOUT	RF Output. The RFOUT pin is ac-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
8	VDD	Drain Bias. Connect the VDD pin to the supply voltage. See Figure 5 for the interface schematic.
	GROUND PADDLE	Exposed Paddle. Connect the exposed paddle to a ground plane that has low electrical and thermal impedance.

INTERFACE SCHEMATICS

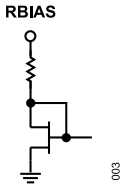

Figure 3. RBIAS Interface Schematic

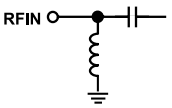

Figure 4. RFIN Interface Schematic

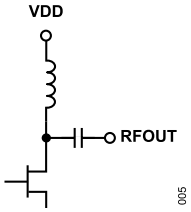

Figure 5. VDD and RFOUT Interface Schematic

Figure 6. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

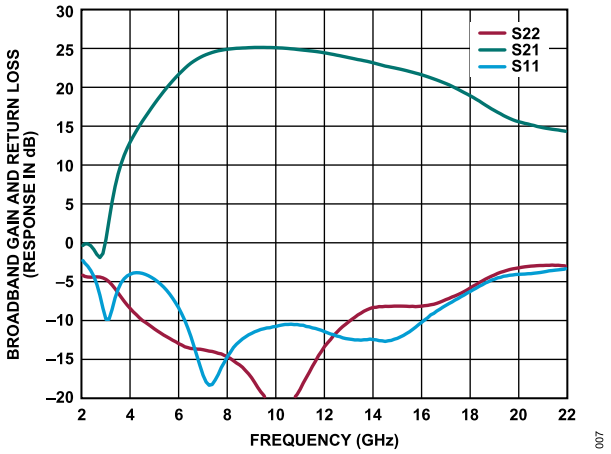

Figure 7. Broadband Gain and Return Loss vs. Frequency, VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ (S22 Is the Output Return Loss, S21 Is the Gain, and S11 Is the Input Return Loss)

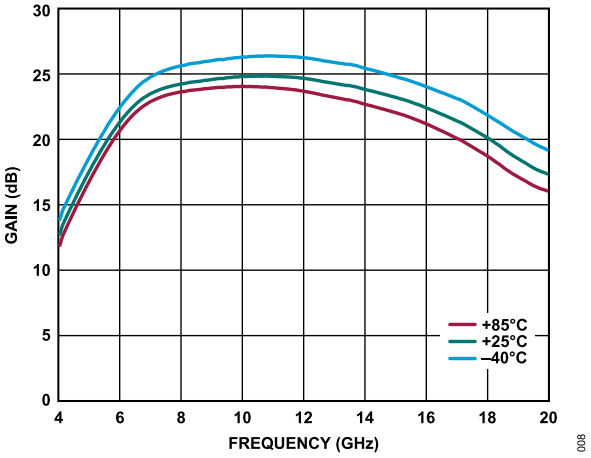

Figure 8. Gain vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 3 V, I_{DQ} = 90 mA, RBIAS = 2.7 kΩ

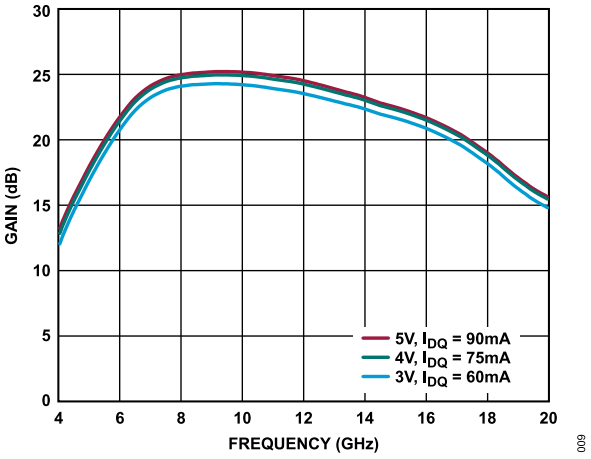

Figure 9. Gain vs. Frequency for Various Supply Voltages and I_{DQ}, RBIAS = 7.15 kΩ

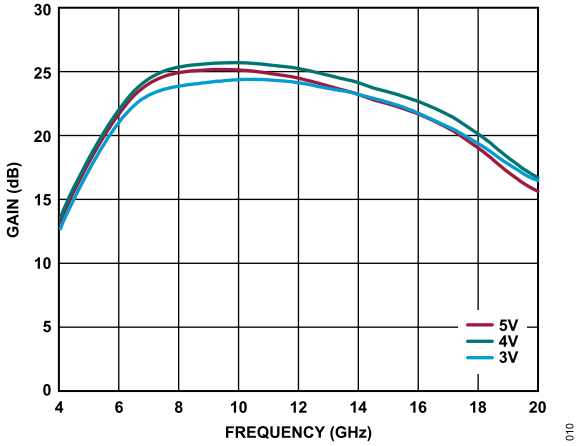

Figure 10. Gain vs. Frequency for Various Supply Voltages, I_{DQ} = 90 mA

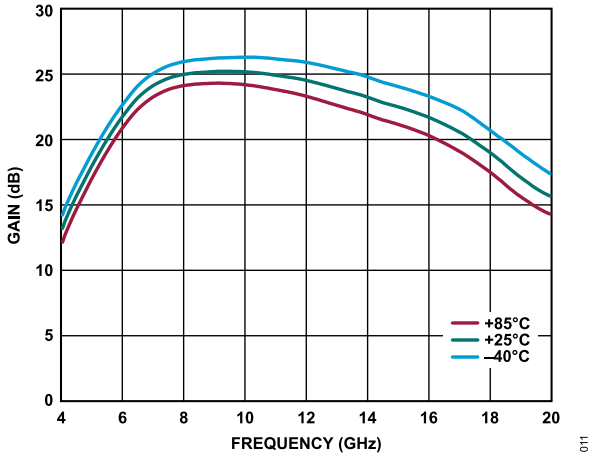

Figure 11. Gain vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ

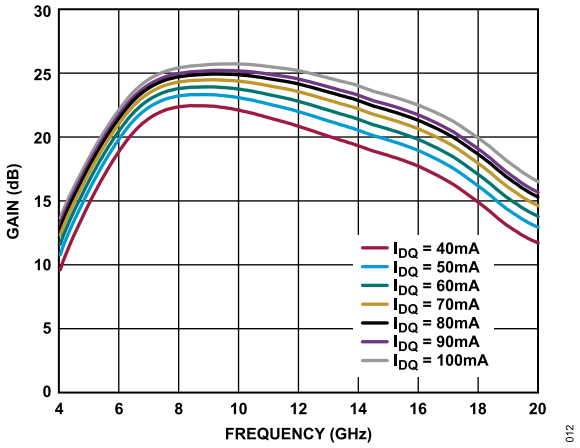

Figure 12. Gain vs. Frequency for Various I_{DQ}, VDD = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

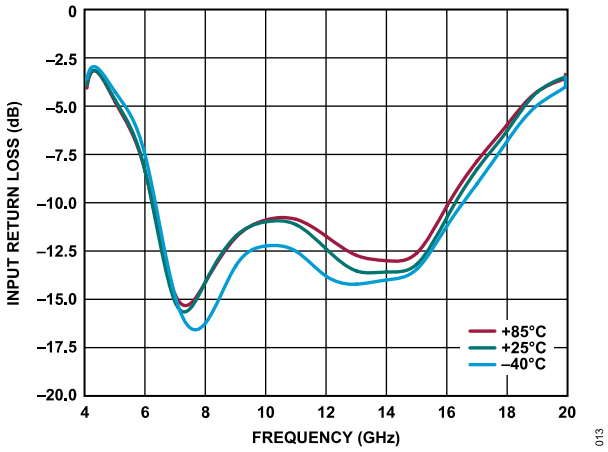

Figure 13. Input Return Loss vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 3 V, I_{DQ} = 90 mA, RBIAS = 2.7 kΩ

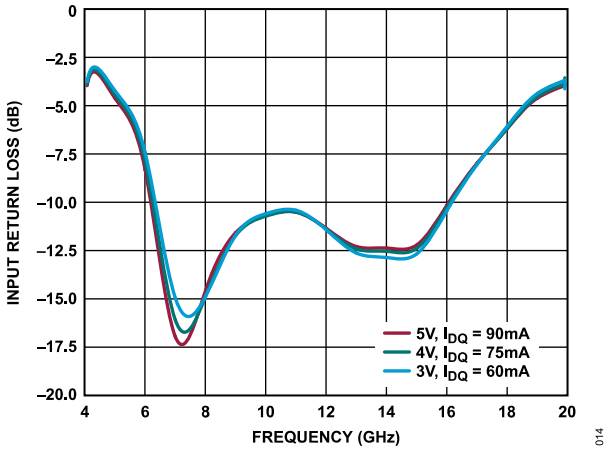

Figure 14. Input Return Loss vs. Frequency for Various Supply Voltages and I_{DQ}, RBIAS = 7.15 kΩ

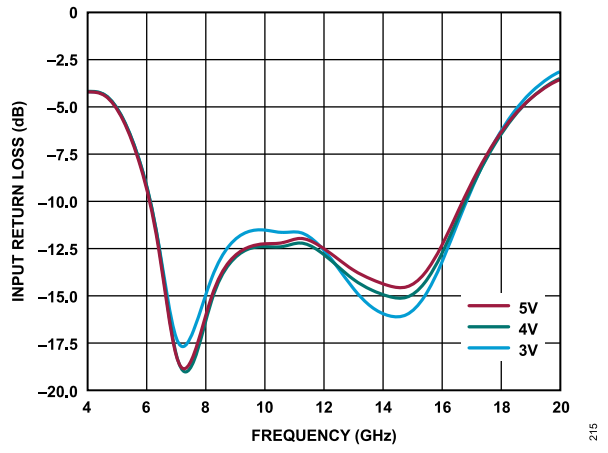

Figure 15. Input Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 90 mA

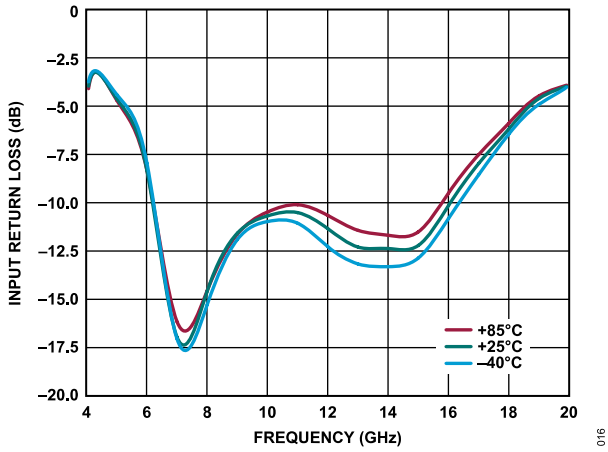

Figure 16. Input Return Loss vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ

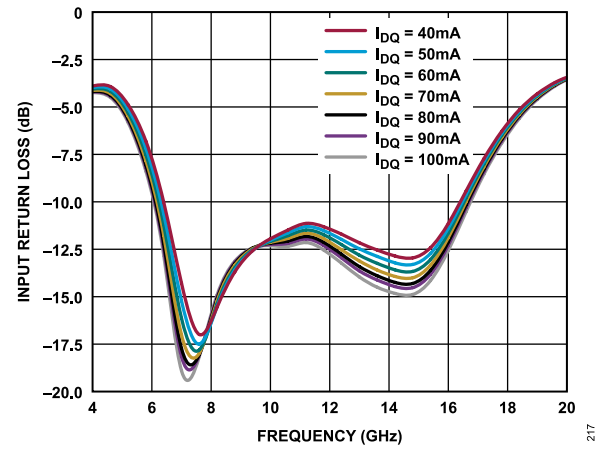

Figure 17. Input Return Loss vs. Frequency for Various I_{DQ}, VDD = 5 V

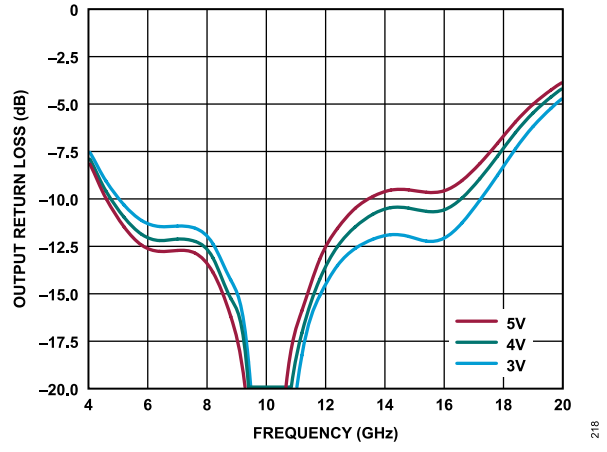

Figure 18. Output Return Loss vs. Frequency for Various Supply Voltages, I_{DQ} = 90 mA

TYPICAL PERFORMANCE CHARACTERISTICS

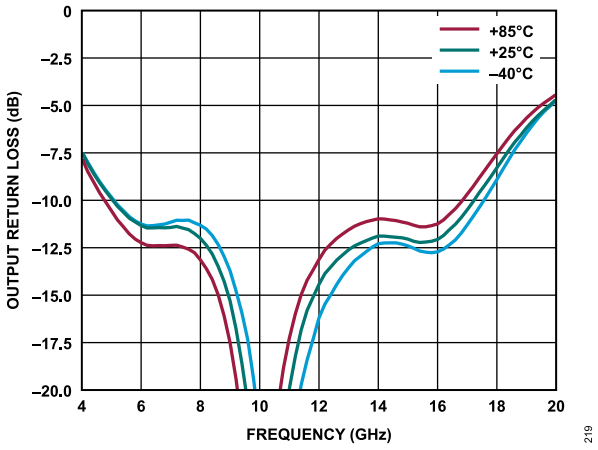

Figure 19. Output Return Loss vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 3 V, I_{DQ} = 90 mA, RBIAS = 2.7 kΩ

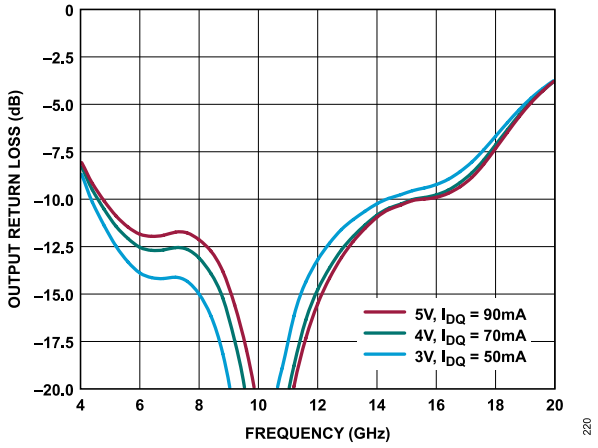

Figure 20. Output Return Loss vs. Frequency for Various Supply Voltages and I_{DQ}, RBIAS = 7.15 kΩ

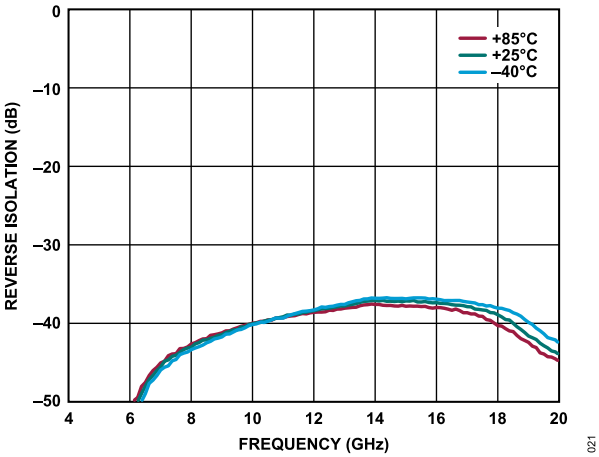

Figure 21. Reverse Isolation vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 3 V, I_{DQ} = 90 mA, RBIAS = 2.7 kΩ

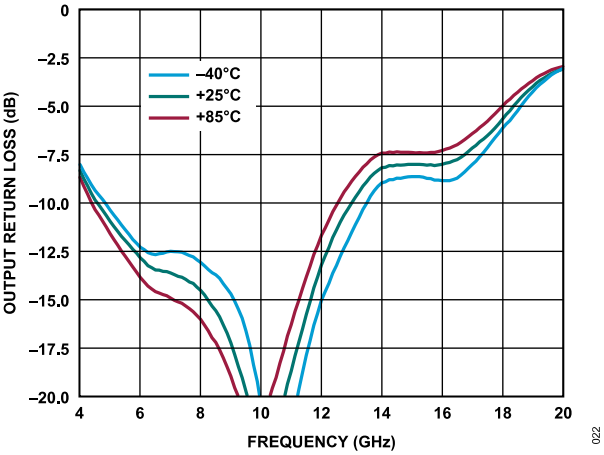

Figure 22. Output Return Loss vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ

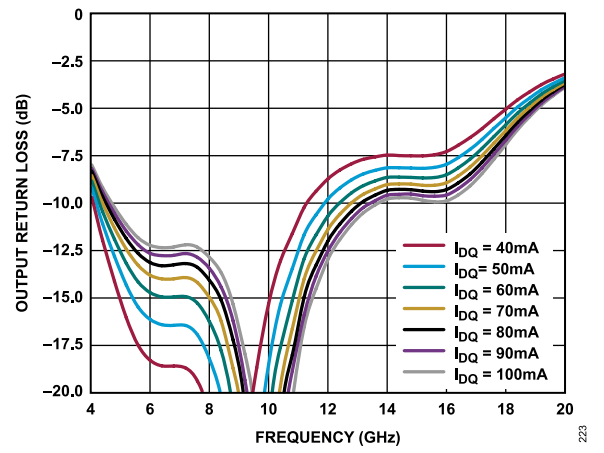

Figure 23. Output Return Loss vs. Frequency for Various I_{DQ}, VDD = 5 V

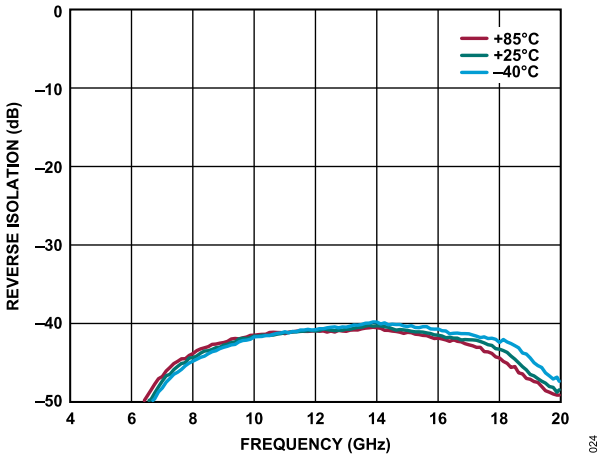

Figure 24. Reverse Isolation vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

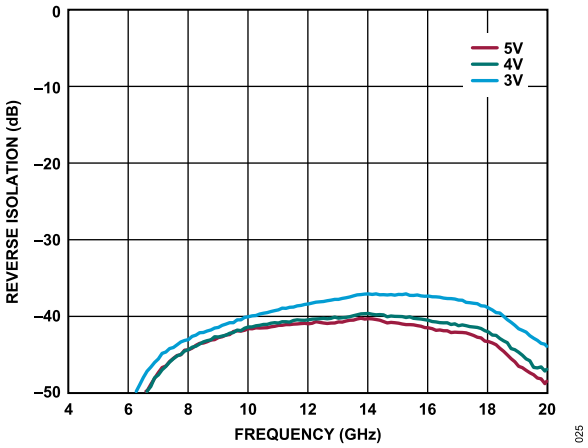

Figure 25. Reverse Isolation vs. Frequency for Various Supply Voltages, I_{DQ} = 90 mA

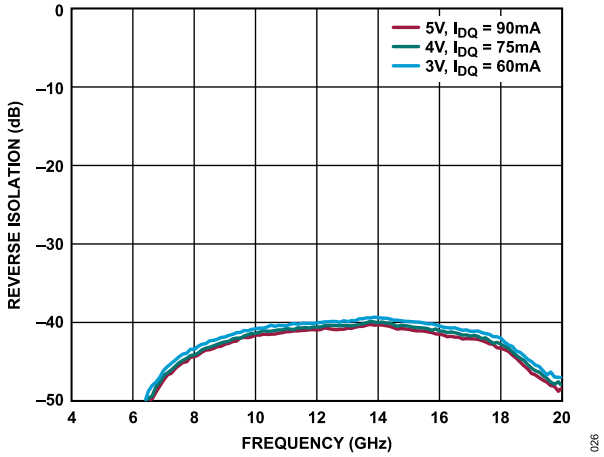

Figure 26. Reverse Isolation vs. Frequency for Various Supply Voltages and I_{DQ}, RBIAS = 7.15 kΩ

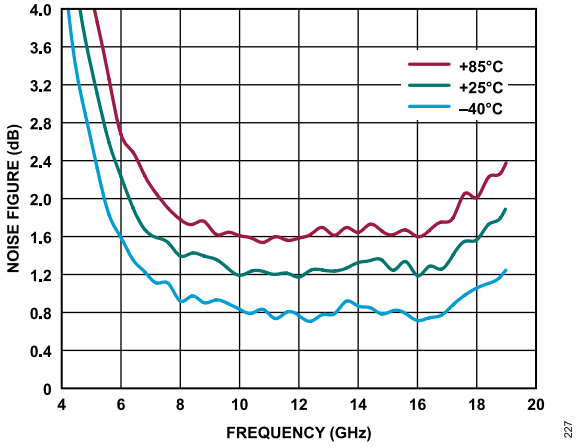

Figure 27. Noise Figure vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 3 V, I_{DQ} = 90 mA, RBIAS = 2.7 kΩ

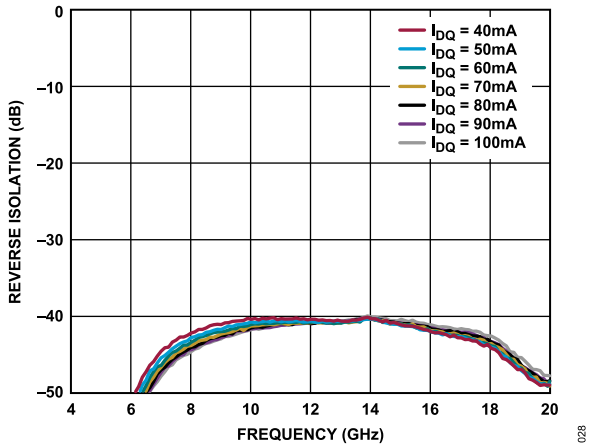

Figure 28. Reverse Isolation vs. Frequency for Various I_{DQ}, VDD = 5 V

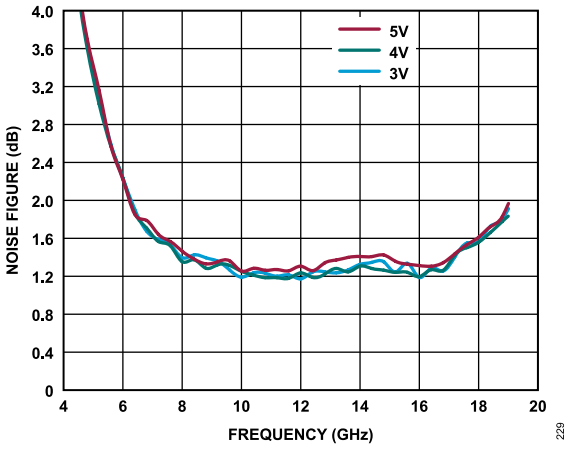

Figure 29. Noise Figure vs. Frequency for Various Supply Voltages, I_{DQ} = 90 mA

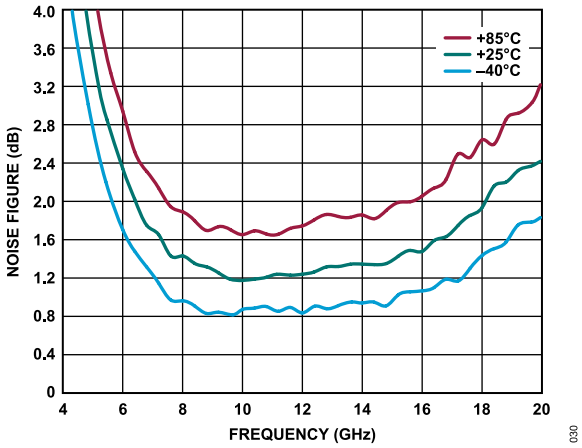

Figure 30. Noise Figure vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

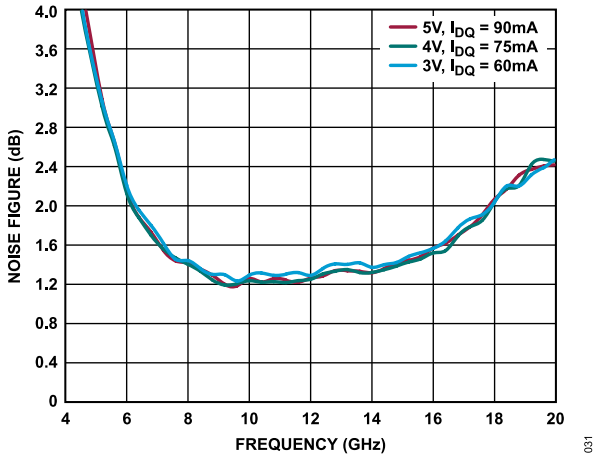

Figure 31. Noise Figure vs. Frequency for Various Supply Voltages and I_{DQ}, RBIAS = 7.15 kΩ

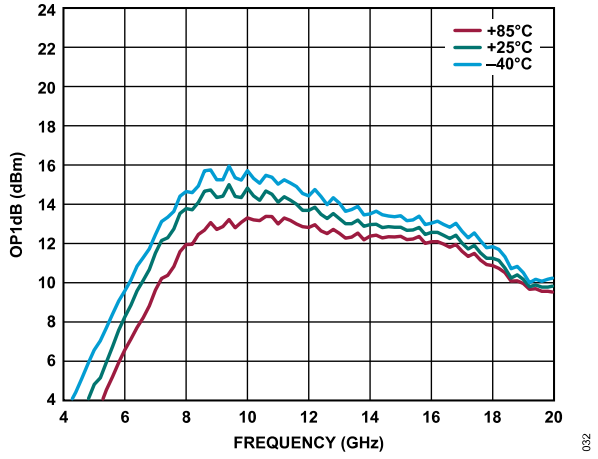

Figure 32. OP1dB vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 3 V, I_{DQ} = 90 mA, RBIAS = 2.7 kΩ

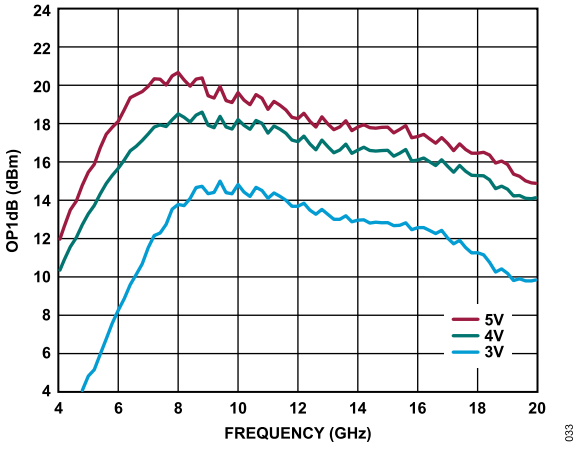

Figure 33. OP1dB vs. Frequency for Various Supply Voltages, I_{DQ} = 90 mA

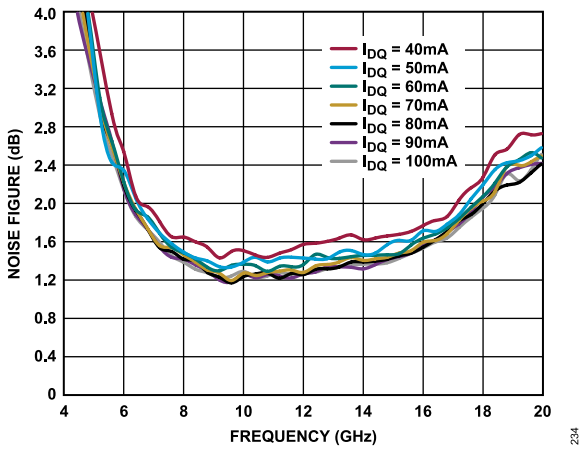

Figure 34. Noise Figure vs. Frequency for Various I_{DQ}, VDD = 5 V

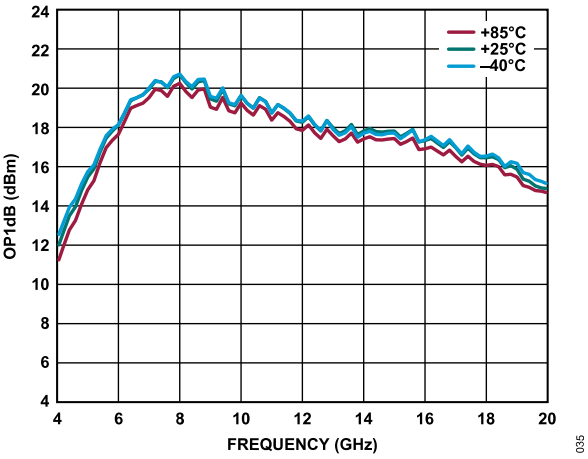

Figure 35. OP1dB vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ

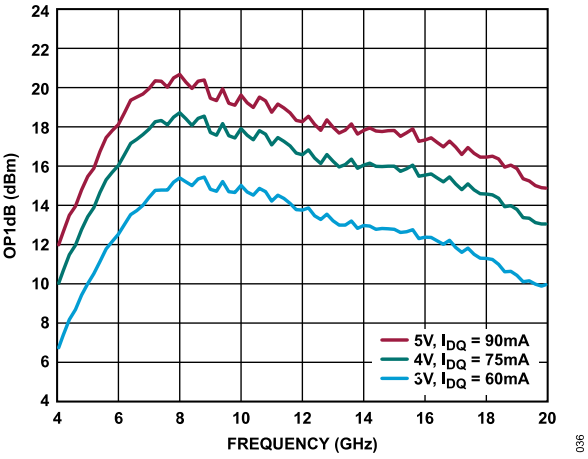

Figure 36. OP1dB vs. Frequency for Various Supply Voltages and I_{DQ}, RBIAS = 7.15 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

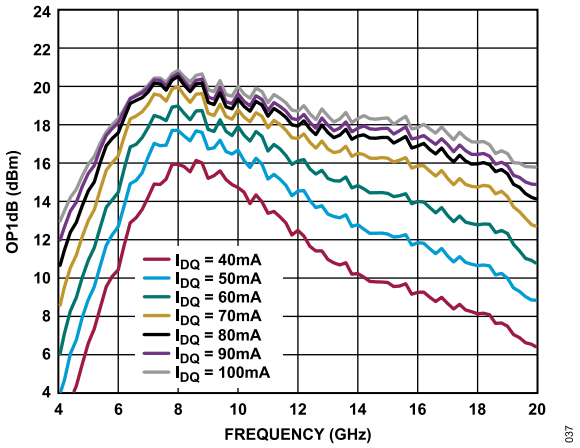

Figure 37. OP1dB vs. Frequency for Various I_{DQ}, VDD = 5 V

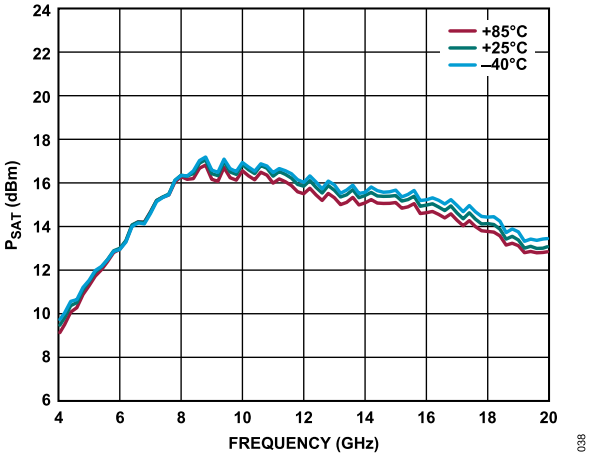

Figure 38. P_{SAT} vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 3 V, I_{DQ} = 90 mA, RBIAS = 2.7 kΩ

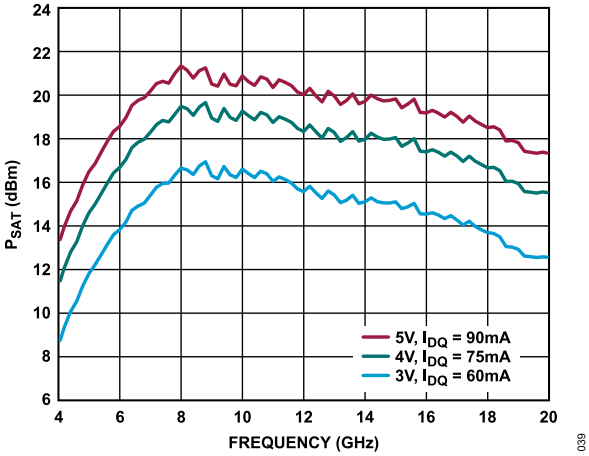

Figure 39. P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ}, RBIAS = 7.15 kΩ

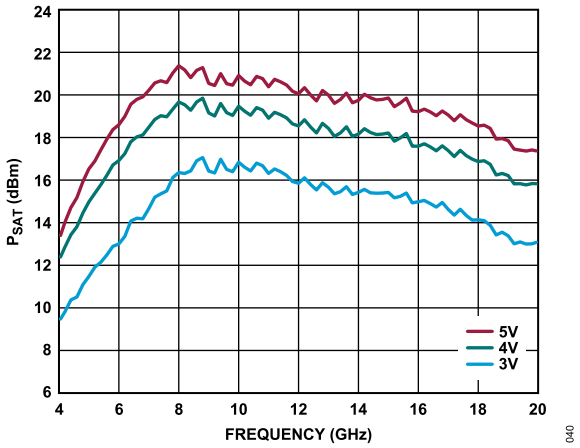

Figure 40. P_{SAT} vs. Frequency for Various Supply Voltages, I_{DQ} = 90 mA

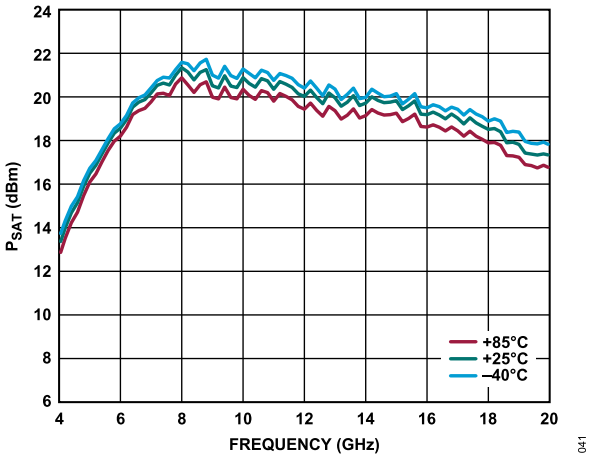

Figure 41. P_{SAT} vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ

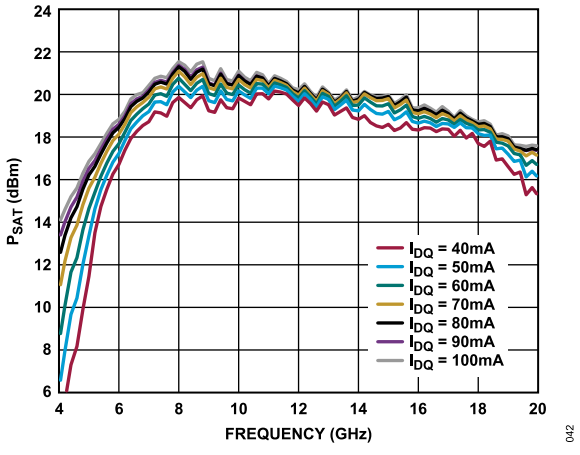

Figure 42. P_{SAT} vs. Frequency for Various I_{DQ}, VDD = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

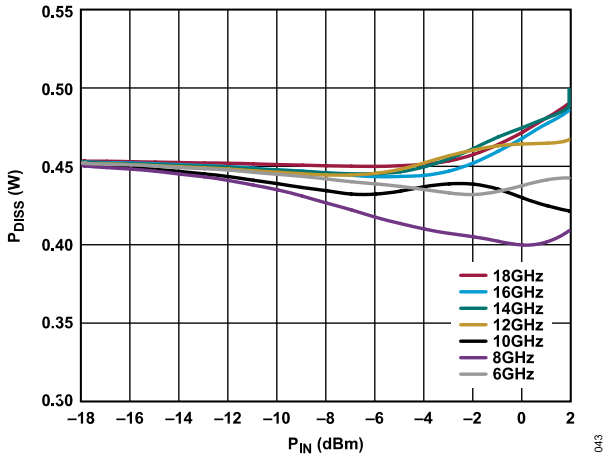

Figure 43. P_{DISS} vs. P_{IN} at T_A = 85°C, VDD = 5 V, I_{DD} = 90 mA

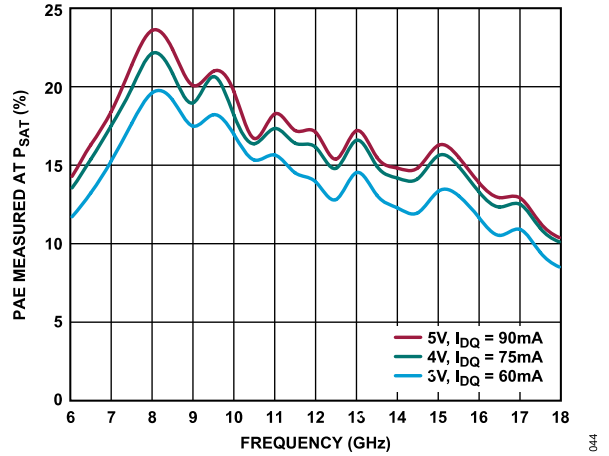

Figure 44. PAE Measured at P_{SAT} vs. Frequency for Various Supply Voltages and I_{DQ}, RBIAS = 7.15 kΩ

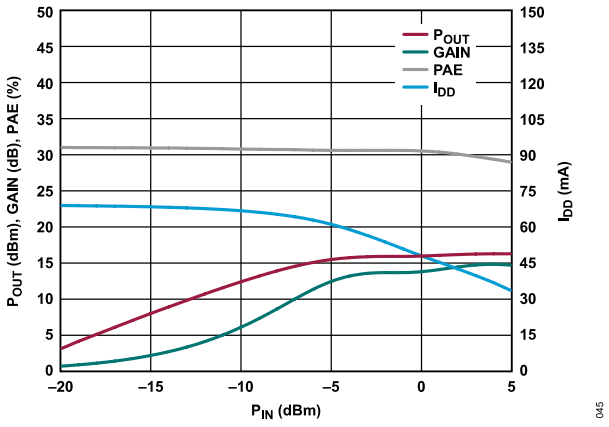

Figure 45. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 8 GHz, VDD = 3 V, RBIAS = 2.7 kΩ

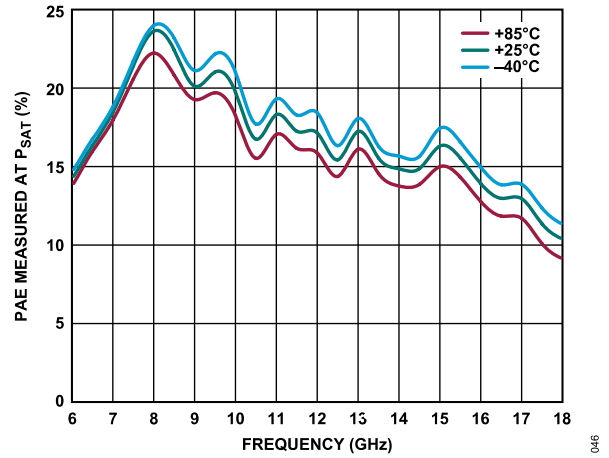

Figure 46. PAE Measured at P_{SAT} vs. Frequency for Various Temperatures, 6 GHz to 18 GHz, VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ

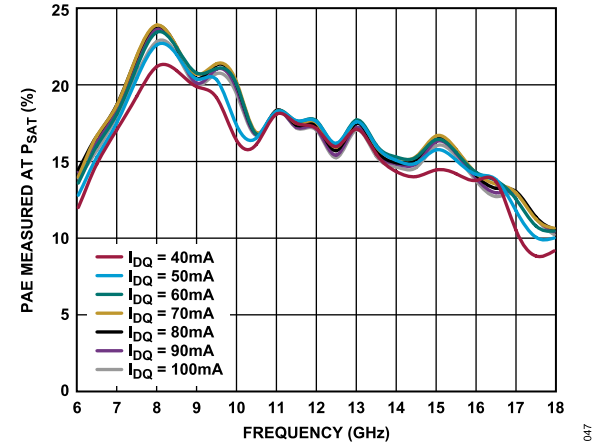

Figure 47. PAE Measured at P_{SAT} vs. Frequency for Various I_{DQ}, VDD = 5 V

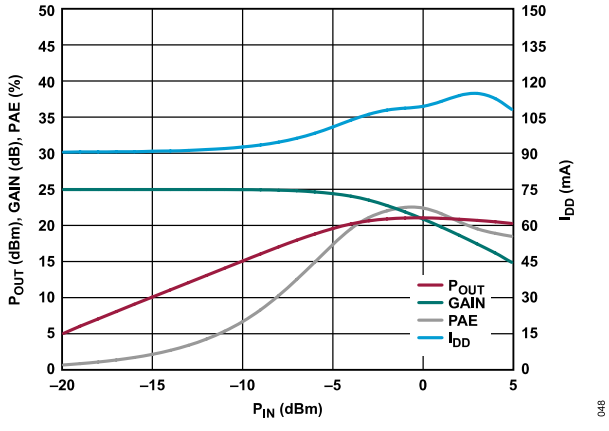

Figure 48. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 8 GHz, VDD = 5 V, RBIAS = 7.15 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

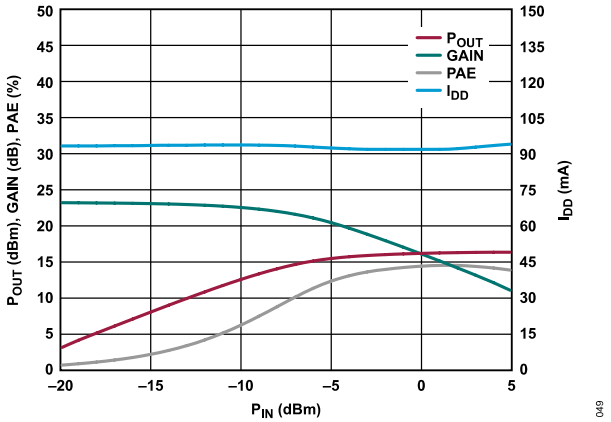

Figure 49. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 12 GHz, VDD = 3 V, RBIAS = 2.7 kΩ

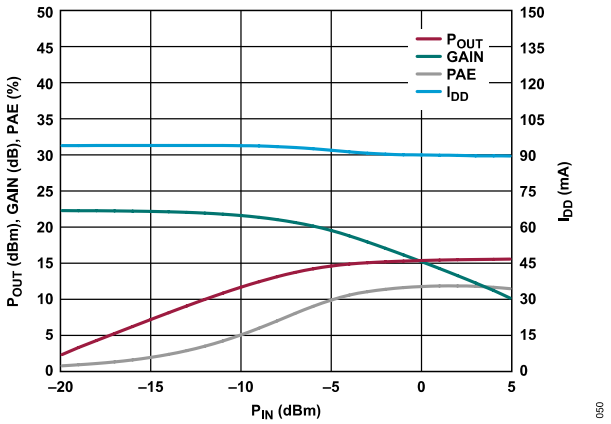

Figure 50. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 16 GHz, VDD = 3 V, RBIAS = 2.7 kΩ

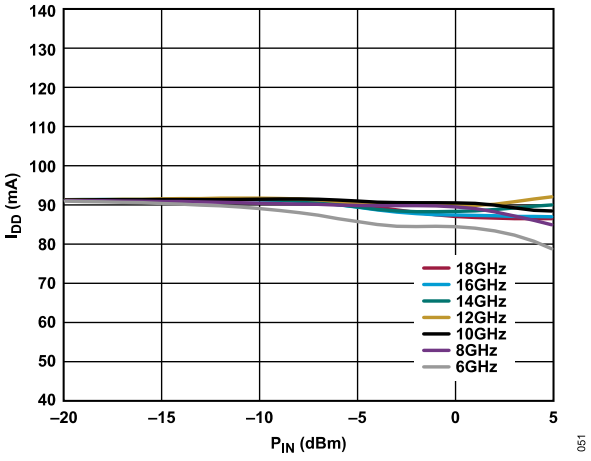

Figure 51. I_{DD} vs. P_{IN} for Various Frequencies, VDD = 3 V, RBIAS = 2.7 kΩ

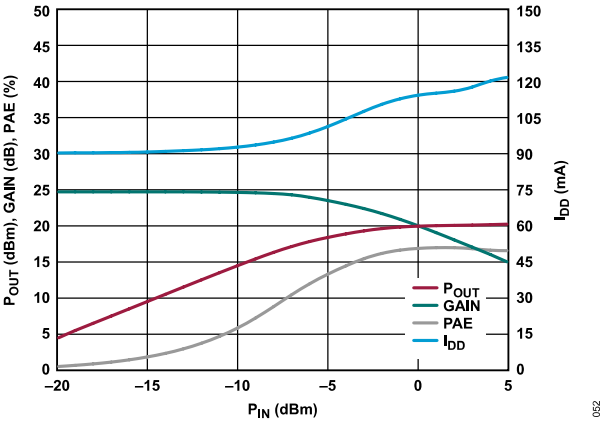

Figure 52. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 12 GHz, VDD = 5 V, RBIAS = 7.15 kΩ

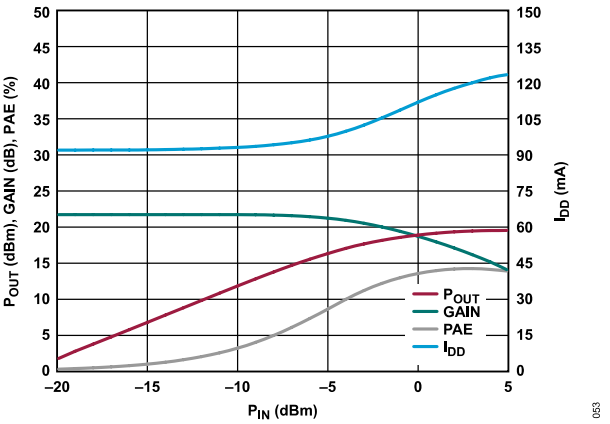

Figure 53. P_{OUT}, Gain, PAE, and I_{DD} vs. P_{IN}, Power Compression at 16 GHz, VDD = 5 V, RBIAS = 7.15 kΩ

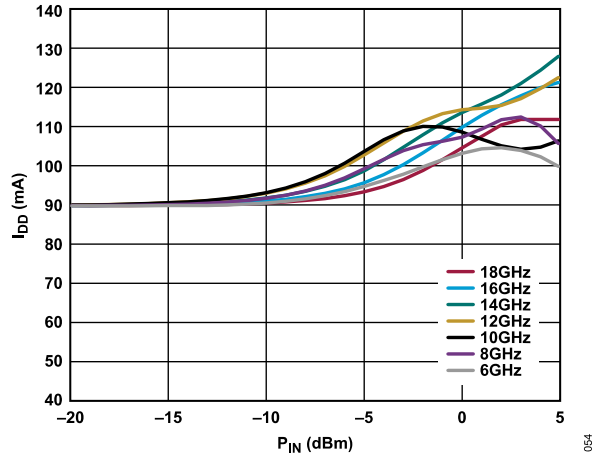

Figure 54. I_{DD} vs. P_{IN} for Various Frequencies, VDD = 5 V, RBIAS = 7.15 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

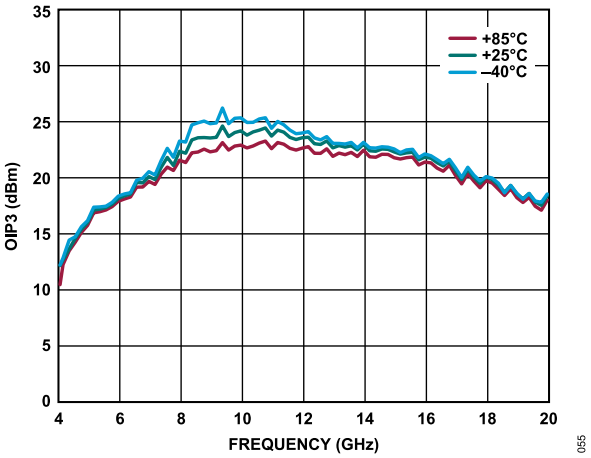

Figure 55. OIP3 vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 3 V, I_{DQ} = 90 mA, RBIAS = 2.7 kΩ

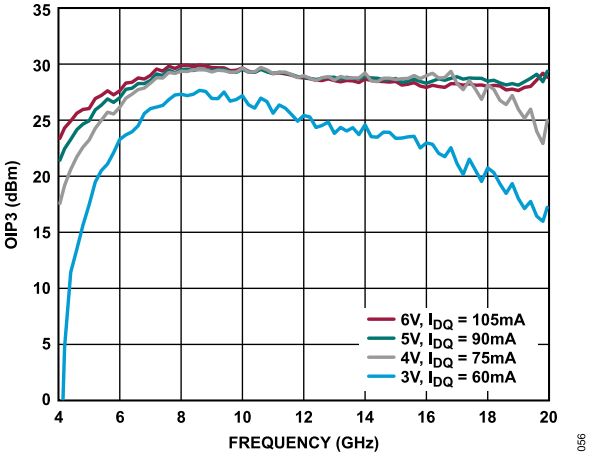

Figure 56. OIP3 vs. Frequency for Various Supply Voltages and I_{DQ}, RBIAS = 7.15 kΩ

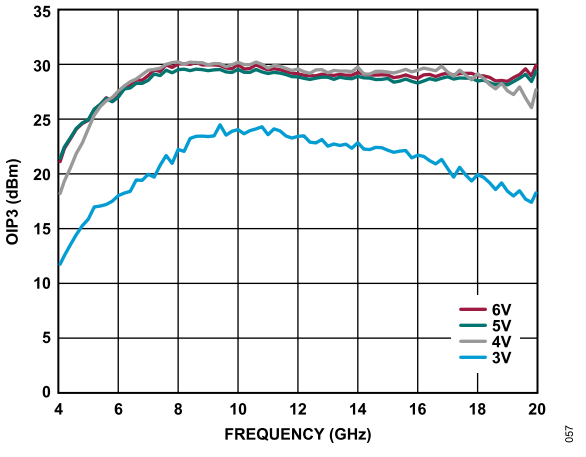

Figure 57. OIP3 vs. Frequency for Various Supply Voltages, I_{DQ} = 90 mA

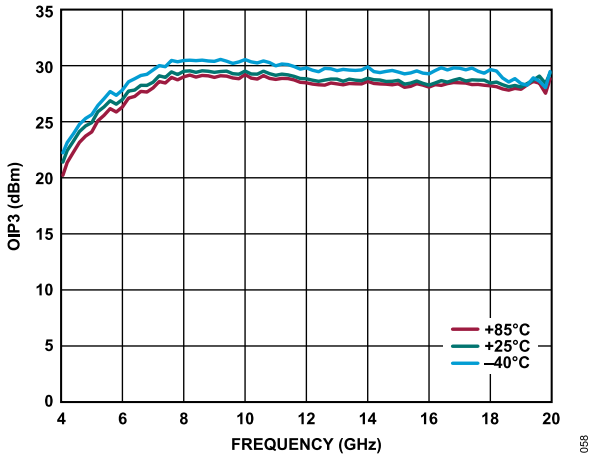

Figure 58. OIP3 vs. Frequency for Various Temperature, 4 GHz to 20 GHz, VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ

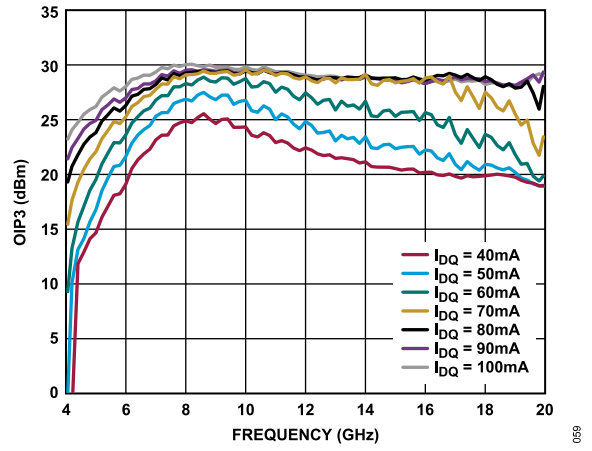

Figure 59. OIP3 vs. Frequency for Various I_{DQ}, VDD = 5 V

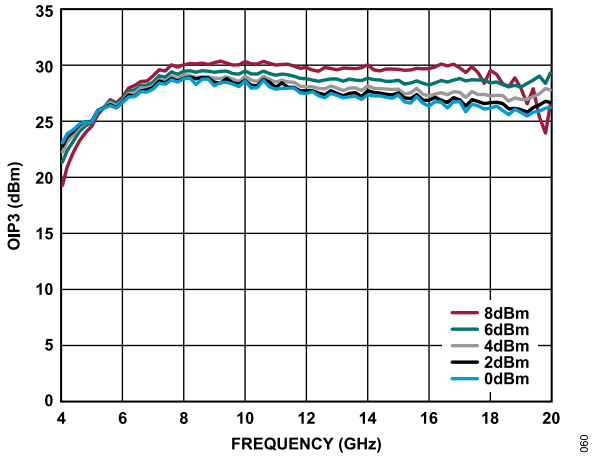

Figure 60. OIP3 vs. Frequency for Various P_{OUT} per Tone, 4 GHz to 20 GHz, VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ

TYPICAL PERFORMANCE CHARACTERISTICS

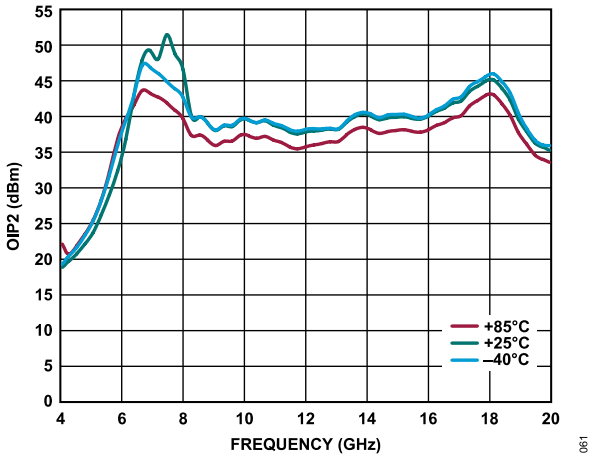

Figure 61. OIP2 vs. Frequency for Various Temperatures, 4 GHz to 20 GHz, VDD = 3 V, I_{DQ} = 90 mA, RBIAS = 2.7 kΩ

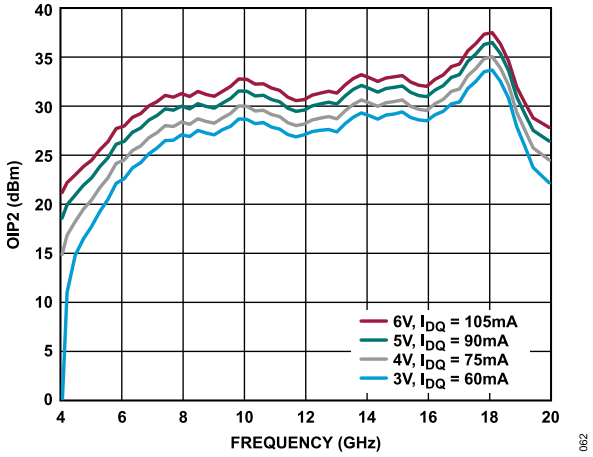

Figure 62. OIP2 vs. Frequency for Various Supply Voltages and I_{DQ}, RBIAS = 7.15 kΩ

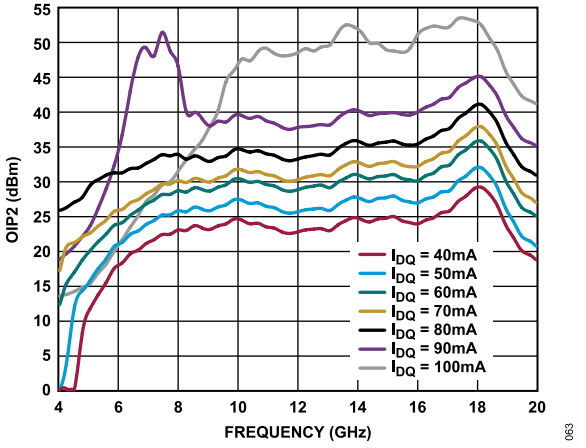

Figure 63. OIP2 vs. Frequency for Various I_{DQ}, VDD = 3 V

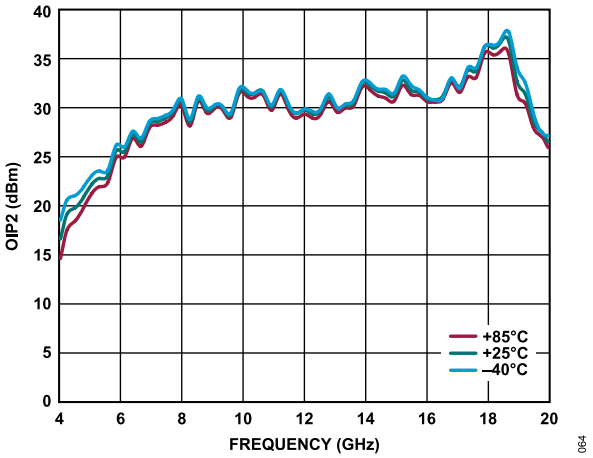

Figure 64. OIP2 vs. Frequency for Various Temperature, 4 GHz to 20 GHz, VDD = 5 V, I_{DQ} = 90 mA, RBIAS = 7.15 kΩ

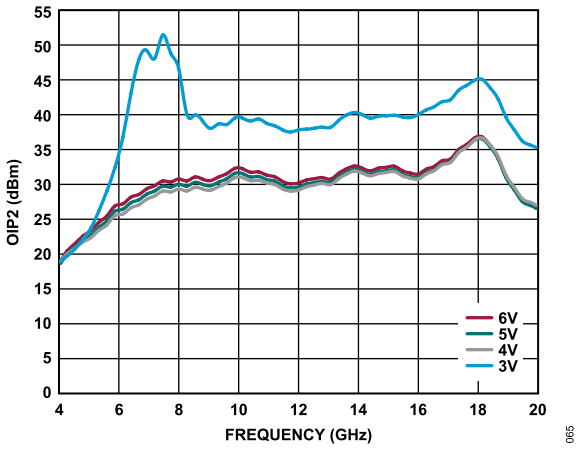

Figure 65. OIP2 vs. Frequency for Various Supply Voltages, I_{DQ} = 90 mA

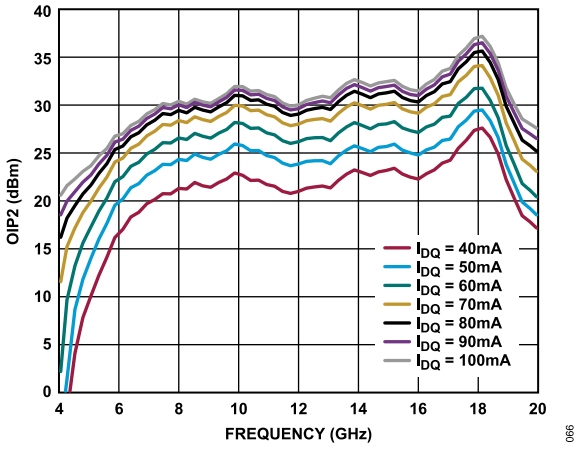

Figure 66. OIP2 vs. Frequency for Various I_{DQ}, VDD = 5 V

TYPICAL PERFORMANCE CHARACTERISTICS

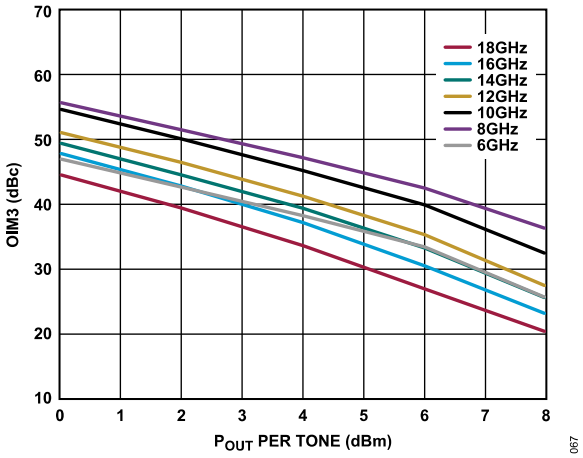

Figure 67. Output Third-Order Intermodulation (OIM3) vs. P_{OUT} per Tone for Various Frequencies, VDD = 3 V

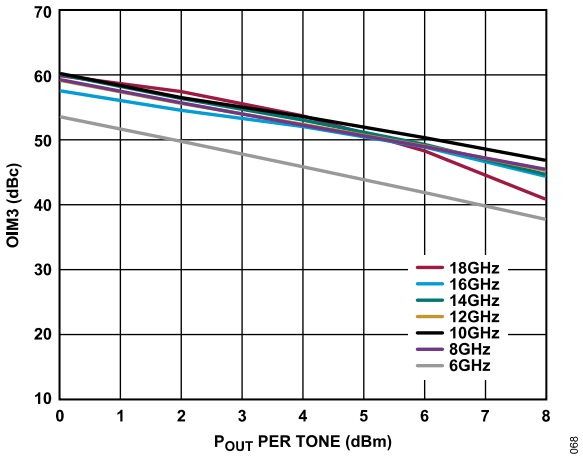

Figure 68. OIM3 vs. P_{OUT} per Tone for Various Frequencies, VDD = 5 V

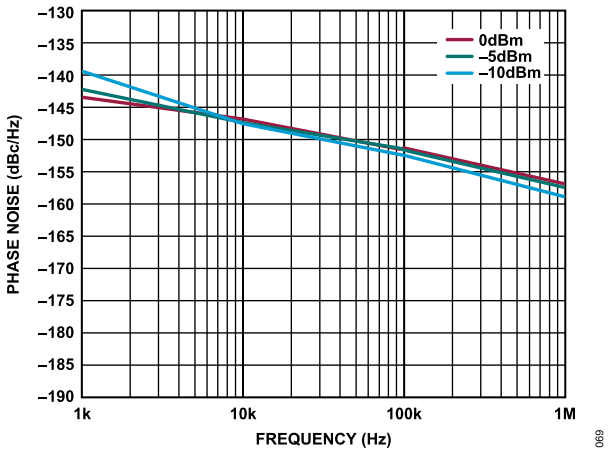

Figure 69. Phase Noise vs. Frequency at 10 GHz for Various P_{IN}

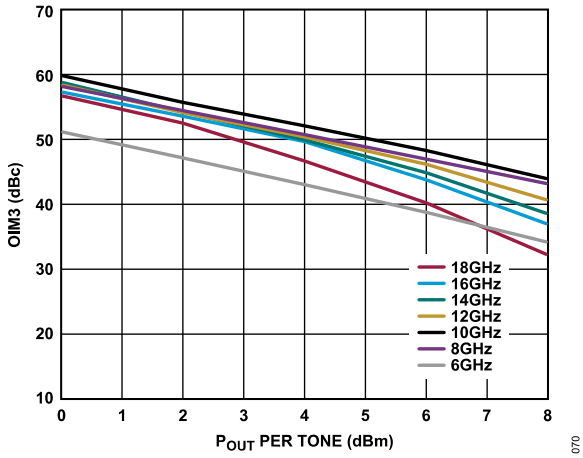

Figure 70. OIM3 vs. P_{OUT} per Tone for Various Frequencies, VDD = 4 V

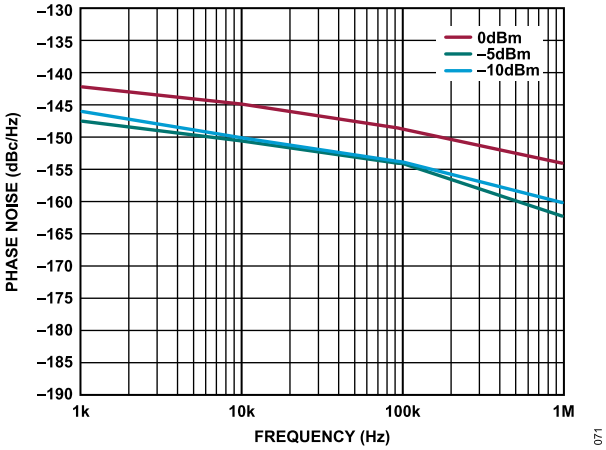

Figure 71. Phase Noise vs. Frequency at 8 GHz for Various P_{IN}

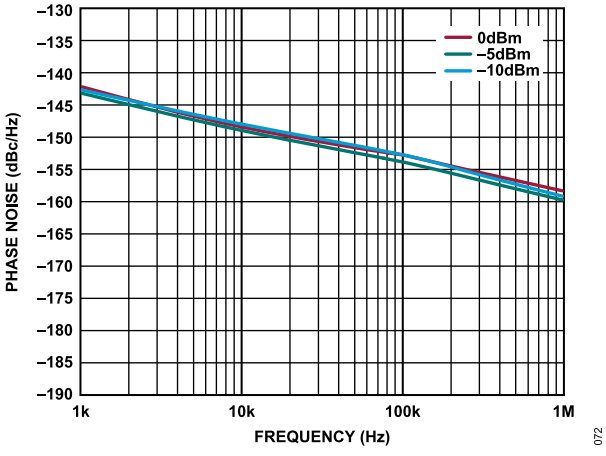

Figure 72. Phase Noise vs. Frequency at 12 GHz for Various P_{IN}

TYPICAL PERFORMANCE CHARACTERISTICS

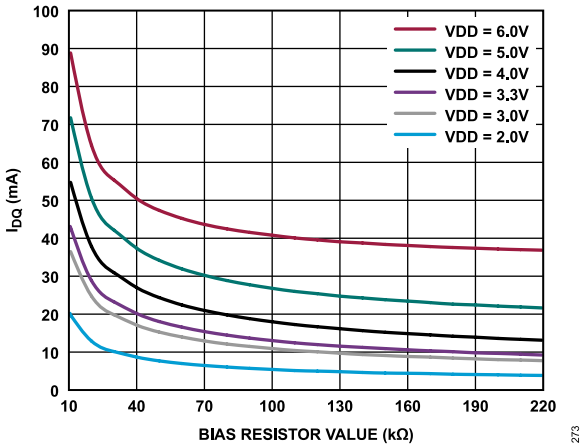

Figure 73. I_{DQ} vs. Bias Resistor Value, 10 kΩ to 220 kΩ, Various Supply Voltages

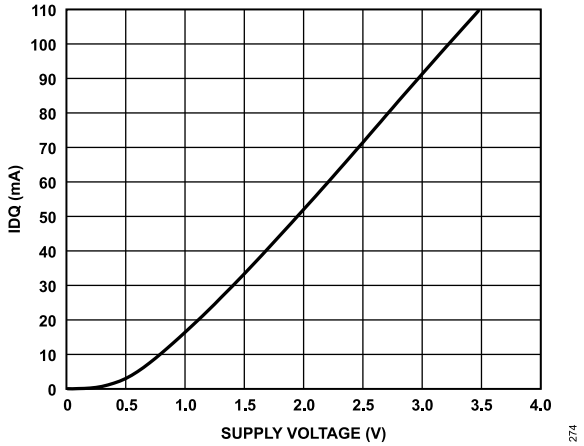

Figure 74. I_{DQ} vs. Supply Voltage, RBIAS = 2.7 kΩ

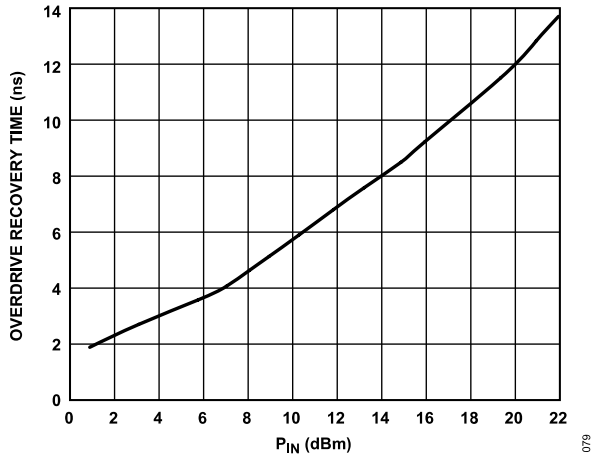

Figure 75. Overdrive Recovery Time vs. P_{IN} at 7 GHz, Recovery to Within 90% of Small Signal Gain Value, VDD = 5 V, RBIAS = 7.15 kΩ

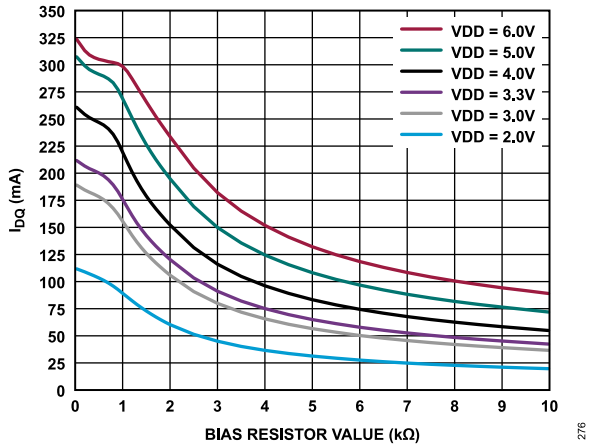

Figure 76. I_{DQ} vs. Bias Resistor Value, 1 Ω to 10 kΩ, Various Supply Voltages

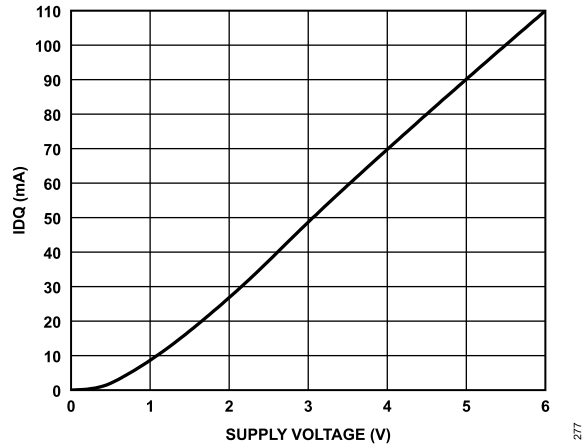

Figure 77. I_{DQ} vs. Supply Voltage, RBIAS = 7.15 kΩ

THEORY OF OPERATION

The ADL8107 is a GaAs, MMIC, pHEMT, low noise wideband amplifier with integrated ac coupling capacitors and a bias inductor. Figure 78 shows a simplified schematic.

The ADL8107 has ac-coupled, single-ended input and output ports with impedances that are nominally equal to 50 Ω over the 6 GHz to 18 GHz frequency range. No external matching components are required. To adjust I_{DQ}, connect an external resistor between the RBIAS and VDD pins.

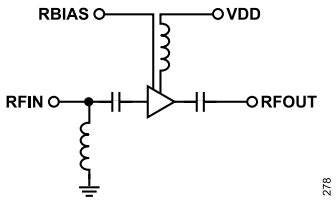

Figure 78. Simplified Schematic

APPLICATIONS INFORMATION

The basic connections for operating the ADL8107 over the specified frequency range are shown in Figure 79. No external biasing inductor is required, allowing the 5 V supply to be connected to the VDD pin. It is recommended to use 0.1 µF and 100 pF power supply decoupling capacitors. The power supply decoupling capacitors shown in Figure 79 represent the configuration used to characterize and qualify the ADL8107.

To set I_{DQ}, connect a resistor (R2) between the RBIAS and VDD pins. A default value of 7.15 kΩ is recommended, which results in a nominal I_{DQ} of 90 mA. Table 9 shows how the I_{DQ} and I_{DQ_AMP} varies vs. the RBIAS. The RBIAS pin also draws a current that varies with the value of RBIAS (see Table 9). Do not leave the RBIAS pin open.

Correct sequencing of the dc and RF power is required to safely operate the ADL8107. During power up, apply VDD before the RF power is applied to RFIN, and during power off, remove the RF power from RFIN before VDD is powered off.

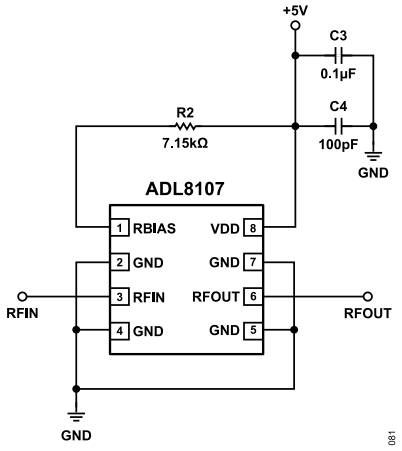

Figure 79. Typical Application Circuit

RECOMMENDED BIAS SEQUENCING

See the ADL8107-EVALZ user guide for the recommended bias sequencing information.

Table 9. Recommended Bias Resistor Values for VDD = 5 V

R_{BIAS} (kΩ)	I_{DQ} (mA)	I_{DQ_AMP} (mA)	I_{RBIAS} (mA)
4.49	110	109.1	0.9
5.49	105	104.2	0.8
5.9	100	99.23	0.77
6.49	95	94.3	0.7
7.15	90	89.4	0.6
7.68	85	84.42	0.58
8.66	80	79.5	0.5
9.76	75	74.55	0.45
11	70	69.6	0.4
12.7	65	64.65	0.35
14.7	60	59.7	0.3
17.4	55	54.75	0.25
21.5	50	49.8	0.2
26.7	45	44.83	0.17
34.8	40	39.87	0.13
48.7	35	34.9	0.1
73.2	30	29.94	0.06

RECOMMENDED POWER MANAGEMENT CIRCUIT

Figure 80 shows a recommended power management circuit for the ADL8107. The LT8607 step-down regulator is used to step down a 12 V rail to 5.5 V, which is then applied to the LT3042 low dropout (LDO) linear regulator to generate a low noise 5 V output. While the circuit shown in Figure 80 has an input voltage of 12 V, the input range to the LT8607 can be as high as 42 V.

The 5.5 V regulator output of the LT8607 is set by the R4A and R5A resistors according to the following equation:

$$R5A = R4A((VREG/0.778\ V) - 1)$$

The switching frequency is set to 2 MHz by the 18.2 kΩ resistor (R2A) on the RT pin. The LT8607 data sheet provides a table of resistor values that can be used to select other switching frequencies ranging from 0.2 MHz to 2.2 MHz.

The output voltage of the LT3042 is set by the R3B resistor connected to the SET pin according to the following equation:

$$VOUT = 100\ \mu A \times R3B$$

The PGFB resistors are chosen to trigger the power-good (PG) signal when the output is just under 95% of the target voltage of 5 V. The output of the LT3042 has 1% initial tolerance and another 1% variation over temperature. The PGFB tolerance is roughly 3% over temperature, and adding resistors results in a bit more (5%), therefore, putting 5% between the output and PGFB works well. In addition, the PG open-collector is pulled up to the 5 V output to give a convenient 0 V to 5 V voltage range. Table 10 provides the recommended resistor values for operation at 5 V, 3.3 V, and 3 V.

Table 10. Recommended Resistor Values for Operating at 5 V, 3.3 V, and 3 V

LT3042 LDO Output Voltage and Power Good Threshold				LT8607 Regulator Output Voltage		
VOUT (V)	R3B (kΩ)	R5B (kΩ)	R6B (kΩ)	Recommended VREG (V)	R4A (MΩ)	R5A (kΩ)
5	49.9	453	32.4	5.5	1	165
3.3	33.2	453	51.1	3.8	1	255
3	30.1	453	56.2	3.5	1	287

The LT8607 can source a maximum current of 750 mA, and the LT3042 can source a maximum current of 200 mA. If the 5 V power supply voltage is being developed as a bus supply to serve another component, higher current devices can be used. The LT8608 and LT8609 step-down regulators can source a maximum current to 1.5 A and 3 A, respectively, and these devices are pin compatible with the LT8607. The LT3045 linear regulator, which is pin compatible with LT3042, can source a maximum current to 500 mA.

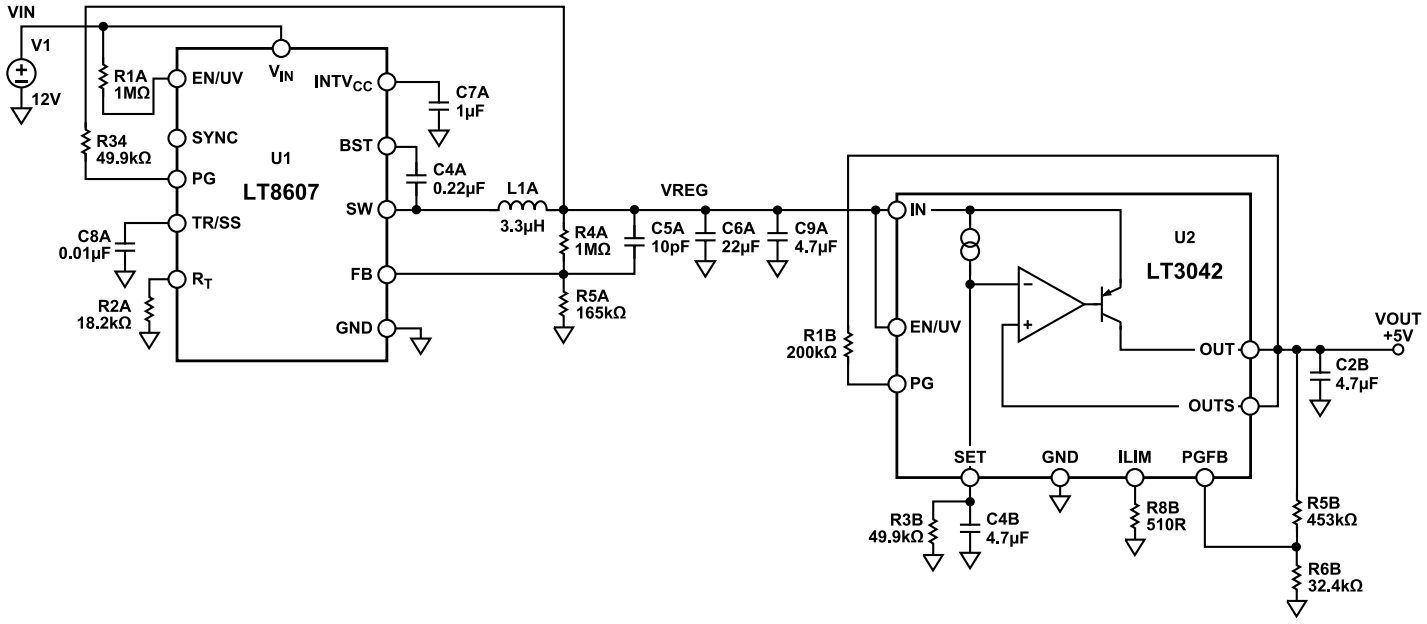

Figure 80. Recommended Power Management Circuit

USING THE RBIAS PIN TO ENABLE AND DISABLE ADL8107

By attaching a single-pole, double throw (SPDT) switch to the RBIAS pin, an enable and/or disable circuit can be implemented as shown in Figure 81. The ADG719 CMOS switch is used to connect the RBIAS resistor either to supply or ground. When the RBIAS resistor is connected to ground, the overall current consumption reduces to 4.73 mA with no RF signal present and 4.92 mA when the RF input level is −10 dBm.

Figure 82 shows a plot of the turn on and/or turn off response time of the RF output envelope when the IN pin of the ADG719 is pulsed.

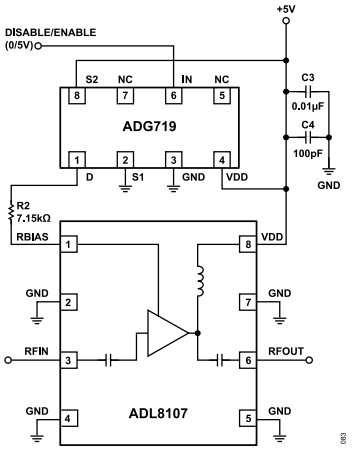

Figure 81. Fast Enable and/or Disable Circuit Using an SPDT

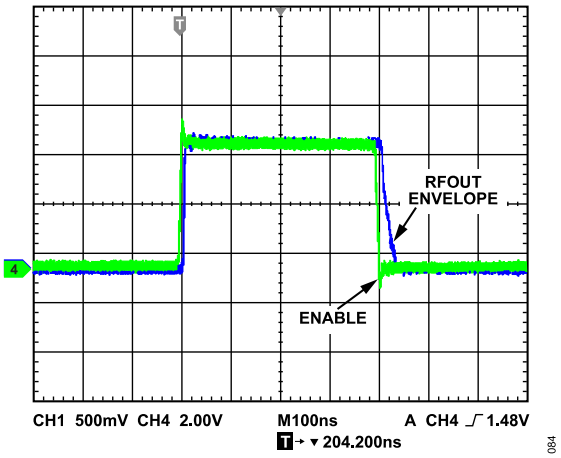

Figure 82. On and/or Off Response of the RF Output Envelope When the IN Pin of the ADG719 Is Pulsed

OUTLINE DIMENSIONS

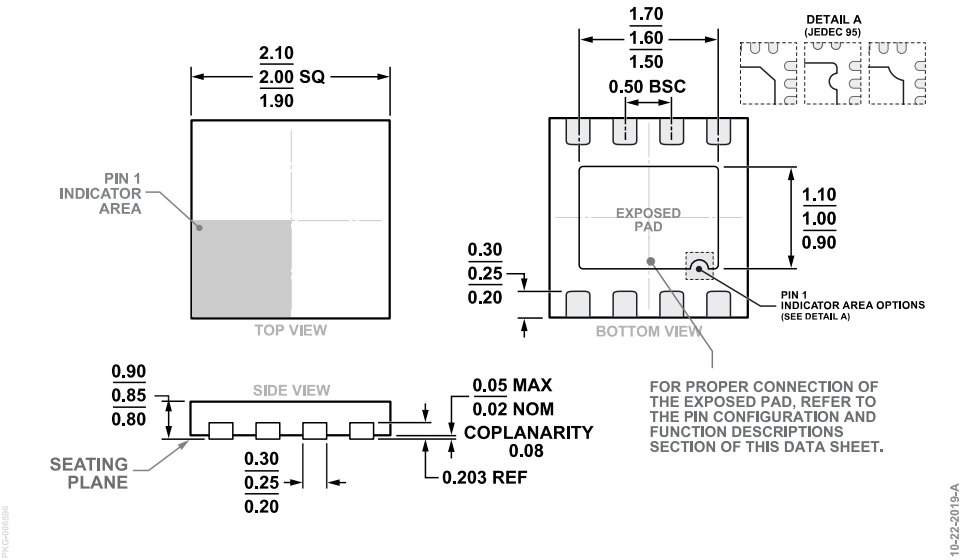

Figure 83. 8-Lead Lead Frame Chip Scale Package [LFCSP]
2 mm × 2 mm Body and 0.85 mm Package Height
(CP-8-30)
Dimensions shown in millimeters

Updated: September 06, 2023

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADL8107ACPZN	-40°C to +85°C	8-lead LFCSP 2 mm × 2 mm × 0.85	Reel, 500	CP-8-30
ADL8107ACPZN-R7	-40°C to +85°C	8-lead LFCSP 2 mm × 2 mm × 0.85	Reel, 500	CP-8-30

[1] Z = RoHS Compliant Part.

EVALUATION BOARDS

Model[1]	Description
ADL8107-EVALZ	Evaluation Board

[1] Z = RoHS Compliant Part.