FINAL

COM'L: H-5/7/10/15/25, Q-10/15/25
IND: H-10/15/20/25

MIL: H-10/15/20/25/30

PALCE22V10 Family

24-Pin EE CMOS Versatile PAL Device

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- As fast as 5 ns propagation delay and 142.8 MHz f_{MAX} (external)
- Low-power EE CMOS
- 10 macrocells programmable as registered or combinatorial, and active high or active low to match application needs
- Varied product term distribution allows up to 16 product terms per output for complex functions
- Global asynchronous reset and synchronous preset for initialization
- Power-up reset for initialization and register preload for testability
- Extensive third-party software and programmer support through FusionPLD partners
- 24-pin SKINNYDIP, 24-pin SOIC, 24-pin Flat-pack and 28-pin PLCC and LCC packages save space
- 5 ns and 7.5 ns versions utilize split leadframes for improved performance

GENERAL DESCRIPTION

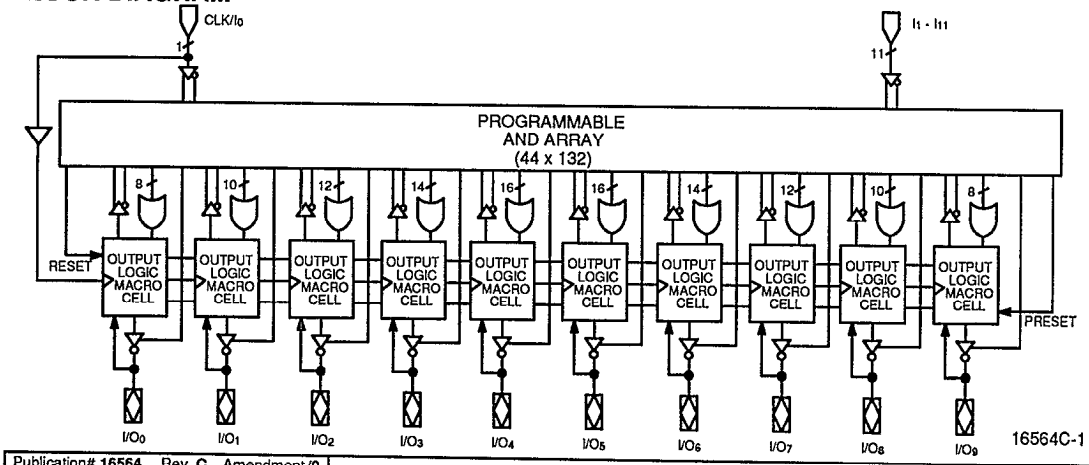
The PALCE22V10 provides user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

The product terms are connected to the fixed OR array with a varied distribution from 8 to16 across the outputs (see Block Diagram). The OR sum of the products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial, and active high or active low. The output configuration is determined by two bits controlling two multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE22V10 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar. Please refer to the PLD Software Reference Guide for certified development systems and the Programmer Reference Guide for approved programmers.

BLOCK DIAGRAM



Publication# 16564 Rev. C Amendment/0
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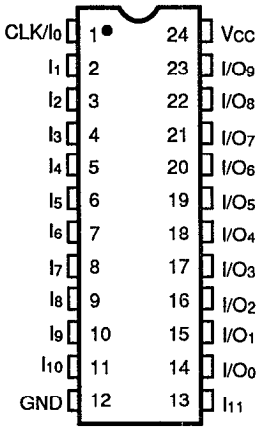
CONNECTION DIAGRAMS

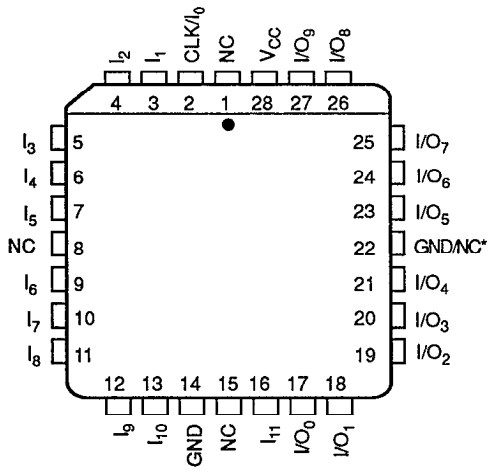
Top View

SKINNYDIP/SOIC/FLATPACK



16564C-2

PLCC/LCC



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**For -5, this pin must be grounded for guaranteed data sheet performance. If not grounded, AC timing may degrade by about 10%.*

Note:
Pin 1 is marked for orientation.

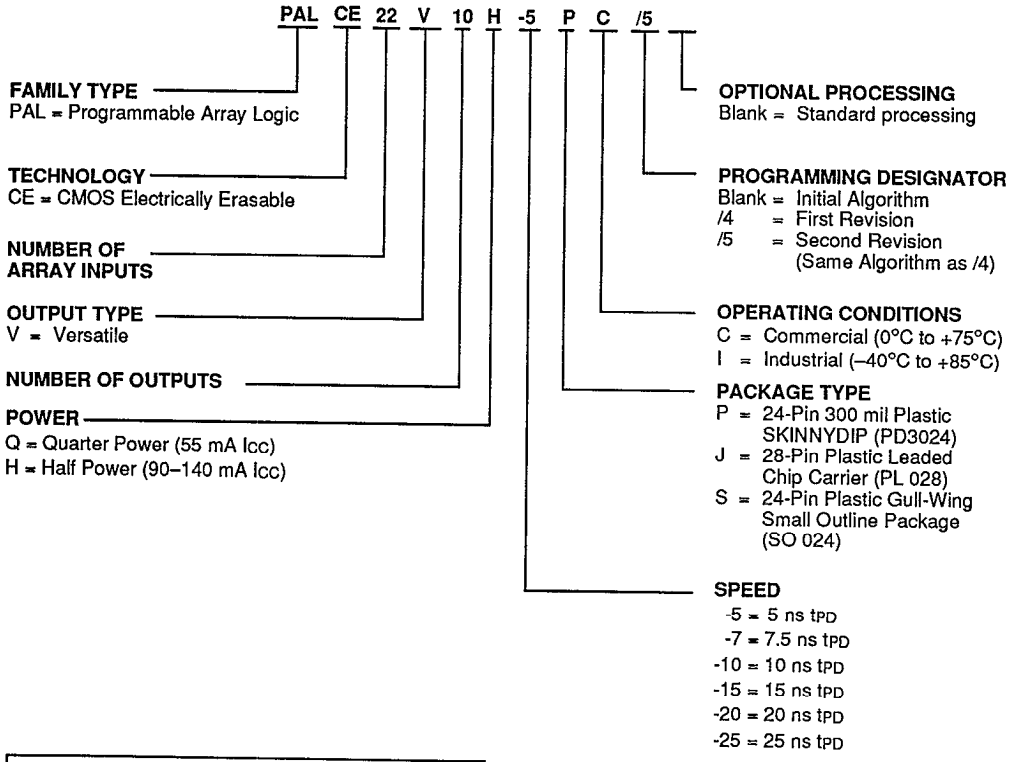
PIN DESIGNATIONS

CLK = Clock
GND = Ground
I = Input
I/O = Input/Output
NC = No Connect
Vcc = Supply Voltage

ORDERING INFORMATION

Commercial and Industrial Products

AMD programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE22V10-5	JC	/5
PALCE22V10H-7	PC, JC, SC	
PALCE22V10H-10	PC, JC, SC, PI, JI	
PALCE22V10Q-10	PC, JC, SC	
PALCE22V10H-15	PC, JC, SC, PI, JI	Blank, /5, /4
PALCE22V10Q-15	PC, JC	/5
PALCE22V10H-20	PI, JI	/4
PALCE22V10H-25	PC, JC, SC, PI, JI	Blank, /4
PALCE22V10Q-25	PC, JC	

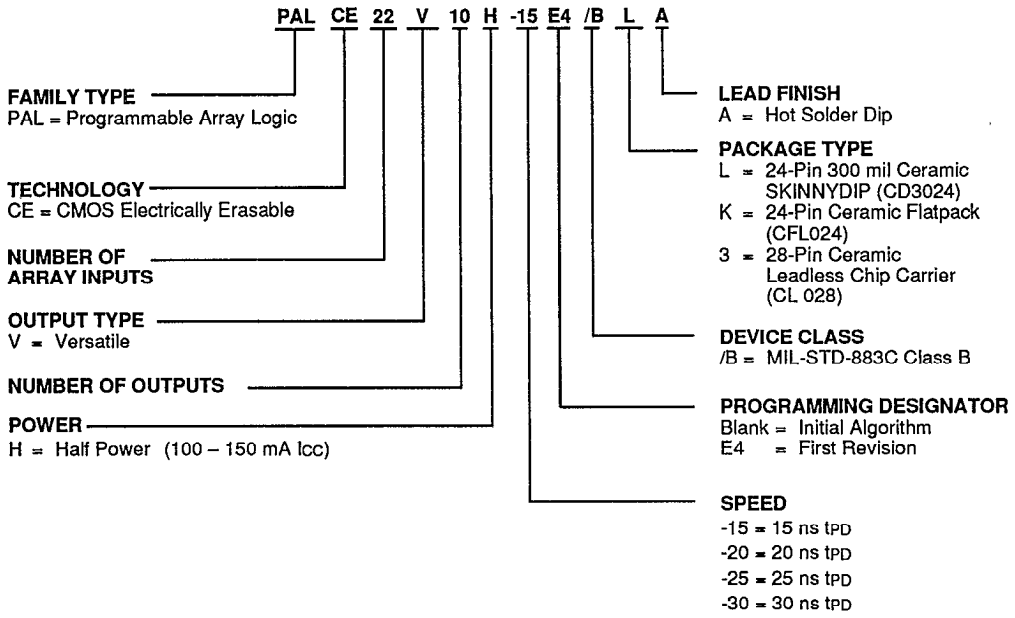
Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

ORDERING INFORMATION

APL Products

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations		
PALCE22V10H-15	E4	/BLA, /BKA, /B3A
PALCE22V10H-20	Blank, E4	
PALCE22V10H-25		
PALCE22V10H-30		

Valid Combinations

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Group A Tests

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

FUNCTIONAL DESCRIPTION

The PALCE22V10 allows the systems engineer to implement the design on-chip, by programming EE cells to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

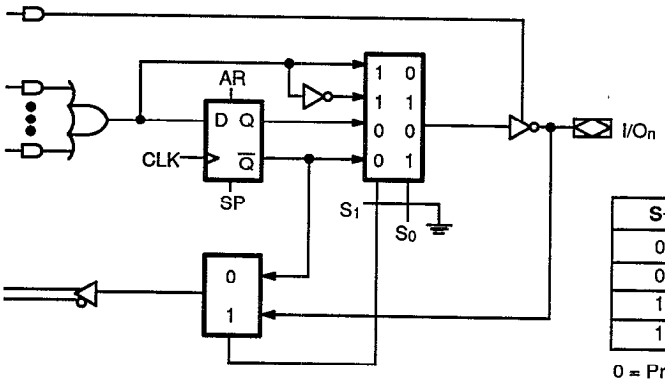
Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state.

The PALCE22V10 has 12 inputs and 10 I/O macrocells. The macrocell Figure 1allows one of four potential output configurations; registered output or combinatorial I/O, active high or active low (see Figure 1). The configuration choice is made according to the user's design specification and corresponding programming of the configuration bits S_0 – S_1. Multiplexer controls are connected to ground (0) through a programmable bit, selecting the "0" path through the multiplexer. Erasing the bit disconnects the control line from GND and it is driven to a high level, selecting the "1" path.

The device is produced with a EE cell link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern.

Variable Input/Output Pin Ratio

The PALCE22V10 has twelve dedicated input lines, and each macrocell output can be an I/O pin. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to V_{CC} or GND.



S_1	S_0	Output Configuration
0	0	Registered/Active Low
0	1	Registered/Active High
1	0	Combinatorial/Active Low
1	1	Combinatorial/Active High

0 = Programmed EE bit
1 = Erased (charged) EE bit

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Figure 1. Output Logic Macrocell Diagram

Registered Output Configuration

Each macrocell of the PALCE22V10 includes a D-type flip-flop for data storage and synchronization. The flip-flop is loaded on the LOW-to-HIGH transition of the clock input. In the registered configuration ($S_1 = 0$), the array feedback is from $\overline{Q}$ of the flip-flop.

Combinatorial I/O Configuration

Any macrocell can be configured as combinatorial by selecting the multiplexer path that bypasses the flip-flop ($S_1 = 1$). In the combinatorial configuration the feedback is from the pin.

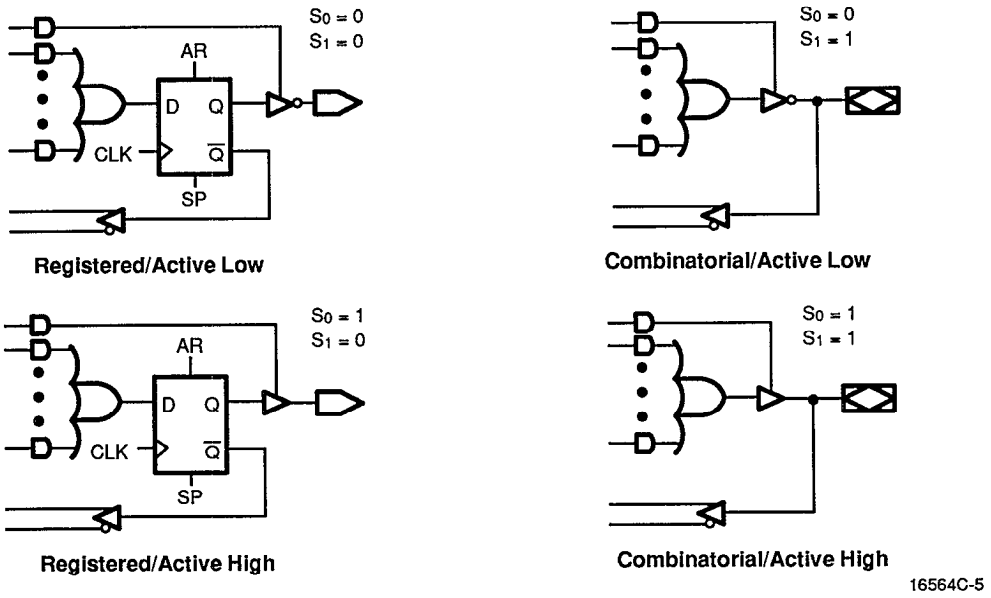


Figure 2. Macrocell Configuration Options

Programmable Three-State Outputs

Each output has a three-state output buffer with three-state control. A product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled.

Programmable Output Polarity

The polarity of each macrocell output can be active high or active low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save "DeMorganizing" efforts.

Selection is controlled by programmable bit S_0 in the output macrocell, and affects both registered and combinatorial outputs. Selection is automatic, based on the design specification and pin definitions. If the pin definition and output equation have the same polarity, the output is programmed to be active high ($S_0 = 1$).

Preset/Reset

For initialization, the PALCE22V10 has Preset and Reset product terms. These terms are connected to all registered outputs. When the Synchronous Preset (SP) product term is asserted high, the output registers will be loaded with a HIGH on the next LOW-to-HIGH clock transition. When the Asynchronous Reset (AR) product term is asserted high, the output registers will be immediately loaded with a LOW independent of the clock.

Note that preset and reset control the flip-flop, not the output pin. The output level is determined by the output polarity selected.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PALCE22V10 will depend on the programmed output polarity. The Vcc rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

The register on the PALCE22V10 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Bit

After programming and verification, a PALCE22V10 design can be secured by programming the security EE bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security bit is programmed, the array will read as if every bit is erased, and preload will be disabled.

The bit can only be erased in conjunction with erasure of the entire pattern.

Programming and Erasing

The PALCE22V10 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

Quality and Testability

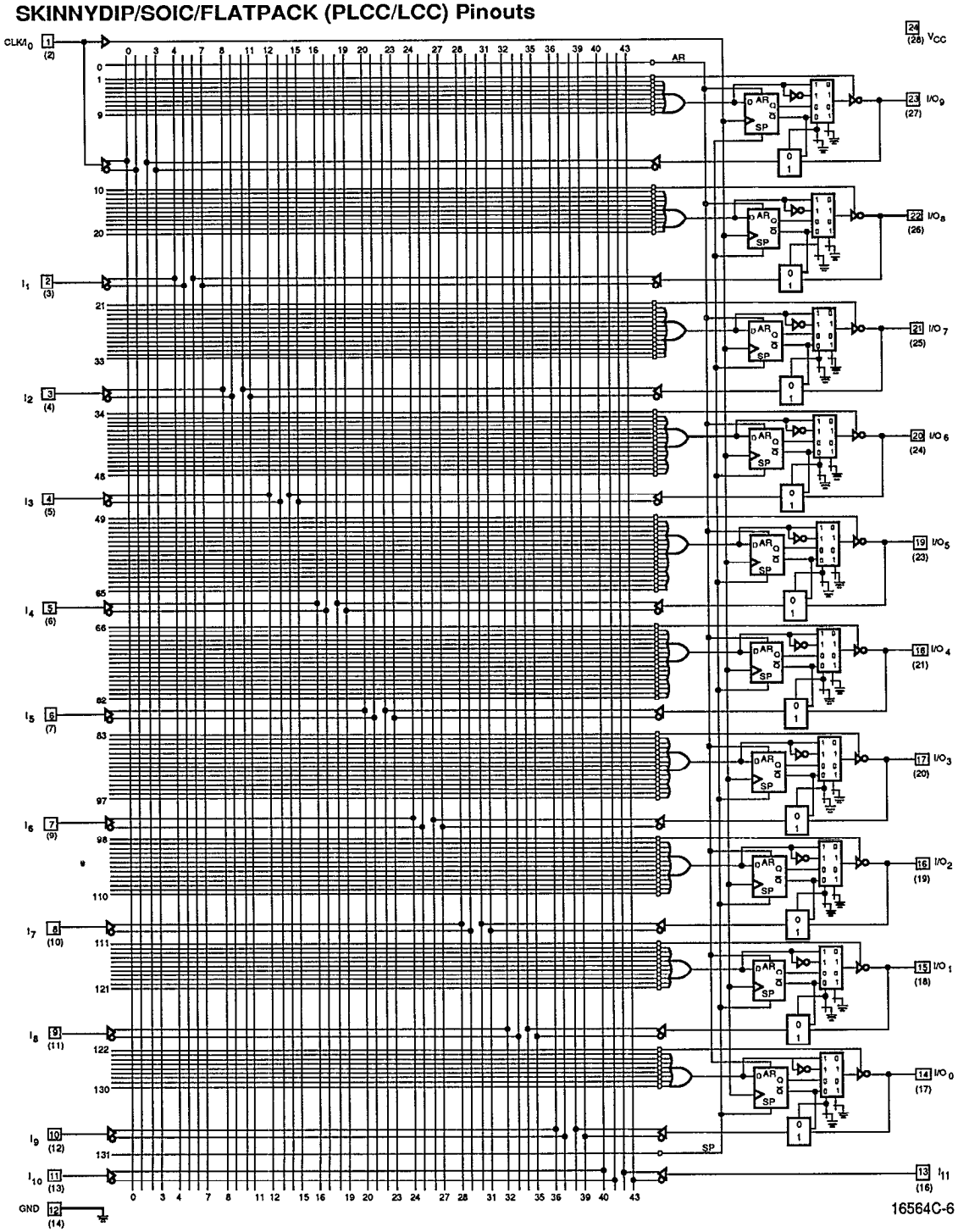
The PALCE22V10 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

Technology

The high-speed PALCE22V10 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clear switching.

LOGIC DIAGRAM

SKINNYDIP/SOIC/FLATPACK (PLCC/LCC) Pinouts



ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage with Respect to Ground ..... −0.5 V to +7.0 V

DC Input Voltage ..... −0.5 V to V_{CC} + 1.0 V

DC Output or I/O Pin Voltage ..... −0.5 V to V_{CC} + 1.0 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground ..... +4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = −3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min		0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)		−100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)		−100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max T_A = 25°C (Note 3)	−30	−130	mA
I_{CC} (Static)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max		115	mA
I_{CC} (Dynamic)	Supply Current	Outputs Open, (I_{OUT} = 0 mA), V_{CC} = Max, f = 25 MHz		140	mA

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-7 PDIP Min	-7 PDIP Max	-7 PLCC Min	-7 PLCC Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output			1	7.5	1	7.5	ns
t_{S1}	Setup Time from Input or Feedback			5		4.5		ns
t_{S2}	Setup Time from SP to Clock			6		6		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output			1	5	1	4.5	ns
t_{SKEWR}	Skew Between Registered Outputs (Note 3)				1		1	ns
t_{AR}	Asynchronous Reset to Registered Output				10		10	ns
t_{ARW}	Asynchronous Reset Width			7		7		ns
t_{ARR}	Asynchronous Reset Recovery Time			7		7		ns
t_{SPR}	Synchronous Preset Recovery Time			7		7		ns
t_{WL}	Clock Width	LOW		3.5		3.0		ns
t_{WH}		HIGH		3.5		3.0		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	$1/(t_S + t_{CO})$	100		111		MHz
		Internal Feedback (f_{CNT})		125		133		MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	142.8		166		MHz
t_{EA}	Input to Output Enable Using Product Term Control				7.5		7.5	ns
t_{ER}	Input to Output Disable Using Product Term Control				7.5		7.5	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *Skew is measured with all outputs switching in the same direction.*
4. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage with Respect to Ground ..... –0.5 V to +7.0 V

DC Input Voltage ..... –0.5 V to V_{CC} + 0.5 V

DC Output or I/O Pin Voltage ..... –0.5 V to V_{CC} + 0.5 V

Static Discharge Voltage ..... 2001 V

Latchup Current (T_A = 0°C to +75°C) ..... 100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air ..... 0°C to +75°C

Supply Voltage (V_{CC}) with Respect to Ground (H/Q-15) .... +4.75 V to +5.25 V

Supply Voltage (V_{CC}) with Respect to Ground (H/Q-25) ..... +4.5 V to +5.5 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min			0.4	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)		2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)			0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = V_{CC}, V_{CC} = Max (Note 2)			10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max (Note 2)			–100	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = V_{CC}, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)			10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max, V_{IN} = V_{IL} or V_{IH} (Note 2)			–100	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = 5 V T_A = 25°C (Note 3)		–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA), V_{CC} = Max	H		90	mA
			Q		55	

Notes:

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V T_A = 25°C f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description			-15 Min	-15 Max	-25 Min	-25 Max	Unit
t_{PD}	Input or Feedback to Combinatorial Output				15		25	ns
t_S	Setup Time from Input, Feedback or SP to Clock			10		15		ns
t_H	Hold Time			0		0		ns
t_{CO}	Clock to Output				10		15	ns
t_{AR}	Asynchronous Reset to Registered Output				20		25	ns
t_{ARW}	Asynchronous Reset Width			15		25		ns
t_{ARR}	Asynchronous Reset Recovery Time			10		25		ns
t_{SPR}	Synchronous Preset Recovery Time			10		25		ns
t_{WL}	Clock Width	LOW		8		13		ns
t_{WH}		HIGH		8		13		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	1/(ts + tco)	50		33.3		MHz
		Internal Feedback (f_{CNT})		58.8		35.7		MHz
t_{EA}	Input to Output Enable Using Product Term Control				15		25	ns
t_{ER}	Input to Output Disable Using Product Term Control				15		25	ns

Notes:

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.*