



LC²MOS 4-/8-Channel High Performance Analog Multiplexers

ADG408/ADG409

FEATURES

44 V Supply Maximum Ratings
V_{SS} to V_{DD} Analog Signal Range
Low On Resistance (100 Ω max)
Low Power (I_{SUPPLY} < 75 μ A)
Fast Switching
Break-Before-Make Switching Action
Plug-in Replacement for DG408/DG409

APPLICATIONS

Audio and Video Routing
Automatic Test Equipment
Data Acquisition Systems
Battery-Powered Systems
Sample-and-Hold Systems
Communication Systems

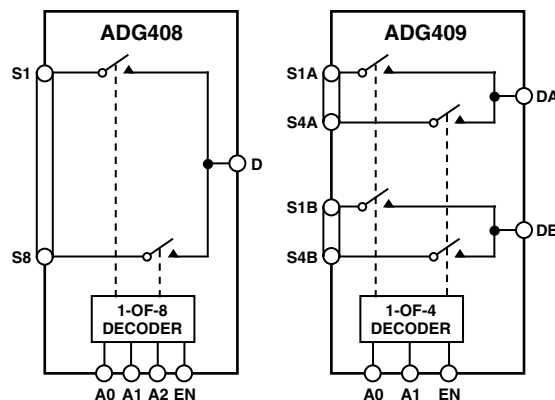
GENERAL DESCRIPTION

The ADG408 and ADG409 are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels, respectively. The ADG408 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1, and A2. The ADG409 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF.

The ADG408/ADG409 are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance. Each channel conducts equally well in both directions when ON and has an input signal range that extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action, preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

The ADG408/ADG409 are improved replacements for the DG408/DG409 analog multiplexers.

FUNCTIONAL BLOCK DIAGRAMS



PRODUCT HIGHLIGHTS

1. Extended Signal Range.
The ADG408/ADG409 are fabricated on an enhanced LC²MOS process, giving an increased signal range that extends to the supply rails.
2. Low Power Dissipation.
3. Low R_{ON}.
4. Single-Supply Operation.
For applications where the analog signal is unipolar, the ADG408/ADG409 can be operated from a single rail power supply. The parts are fully specified with a single 12 V power supply and will remain functional with single supplies as low as 5 V.

REV. B

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ADG408/ADG409—SPECIFICATIONS

DUAL SUPPLY¹ ($V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.)

Parameter	B Version –40°C to +85°C		T Version –55°C to +125°C		Unit	Test Conditions/Comments
	+25°C		+25°C			
ANALOG SWITCH						
Analogue Signal Range		V _{SS} to V _{DD}		V _{SS} to V _{DD}	V	
R _{ON}	40		40		Ω typ	V _D = ±10 V, I _S = –10 mA
	100	125	100	125	Ω max	
ΔR _{ON}	15		15		Ω max	V _D = +10 V, –10 V
LEAKAGE CURRENTS						
Source OFF Leakage I _S (OFF)	±0.5	±50	±0.5	±50	nA max	V _D = ±10 V, V _S = ∓10 V; Test Circuit 2
Drain OFF Leakage I _D (OFF)						V _D = ±10 V; V _S = ∓10 V; Test Circuit 3
ADG408	±1	±100	±1	±100	nA max	
ADG409	±1	±50	±1	±50	nA max	
Channel ON Leakage I _D , I _S (ON)						V _S = V _D = ±10 V; Test Circuit 4
ADG408	±1	±100	±1	±100	nA max	
ADG409	±1	±50	±1	±50	nA max	
DIGITAL INPUTS						
Input High Voltage, V _{INH}		2.4		2.4	V min	
Input Low Voltage, V _{INL}		0.8		0.8	V max	
Input Current						
I _{INL} or I _{INH}		±10		±10	μA max	V _{IN} = 0 or V _{DD}
C _{IN} , Digital Input Capacitance	8		8		pF typ	f = 1 MHz
DYNAMIC CHARACTERISTICS ²						
t _{TRANSITION}		120		120	ns typ	R _L = 300 Ω, C _L = 35 pF; V _{S1} = ±10 V, V _{S8} = ∓10 V; Test Circuit 5
		250		250	ns max	
t _{OPEN}	10	10	10	10	ns min	R _L = 300 Ω, C _L = 35 pF; V _S = 5 V; Test Circuit 6
t _{ON} (EN)	85	125	85	125	ns typ	R _L = 300 Ω, C _L = 35 pF; V _S = 5 V; Test Circuit 7
	150	225	150	225	ns max	R _L = 300 Ω, C _L = 35 pF; V _S = 5 V; Test Circuit 7
t _{OFF} (EN)		65		65	ns typ	R _L = 300 Ω, C _L = 35 pF; V _S = 5 V; Test Circuit 7
		150		150	ns max	V _S = 0 V, R _S = 0 Ω, C _L = 10 nF; Test Circuit 8
Charge Injection	20		20		pC typ	
OFF Isolation	–75		–75		dB typ	R _L = 1 kΩ, f = 100 kHz; V _{EN} = 0 V; Test Circuit 9
Channel-to-Channel Crosstalk	85		85		dB typ	R _L = 1 kΩ, f = 100 kHz; Test Circuit 10
C _S (OFF)	11		11		pF typ	f = 1 MHz
C _D (OFF)						f = 1 MHz
ADG408	40		40		pF typ	
ADG409	20		20		pF typ	
C _D , C _S (ON)						f = 1 MHz
ADG408	54		54		pF typ	
ADG409	34		34		pF typ	
POWER REQUIREMENTS						
I _{DD}		1		1	μA typ	V _{IN} = 0 V, V _{EN} = 0 V
		5		5	μA max	
I _{SS}		1		1	μA typ	
		5		5	μA max	
I _{DD}	100		100		μA typ	V _{IN} = 0 V, V _{EN} = 2.4 V
	200	500	200	500	μA max	

NOTES

¹Temperature ranges are as follows: B Version: –40°C to +85°C; T Version: –55°C to +125°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

SINGLE SUPPLY¹ ($V_{DD} = 12\text{ V}$, $V_{SS} = 0\text{ V}$, $GND = 0\text{ V}$, unless otherwise noted.)

Parameter	B Version		T Version		Unit	Test Conditions/Comments
	+25°C	−40°C to +85°C	+25°C	−55°C to +125°C		
ANALOG SWITCH						
Analog Signal Range	0 to V _{DD}		0 to V _{DD}		V	V _D = 3 V, 10 V, I _S = −1 mA
R _{ON}	90		90		Ω typ	
LEAKAGE CURRENTS						
Source OFF Leakage I _S (OFF)	±0.5	±50	±0.5	±50	nA max	V _D = 8 V/0 V, V _S = 0 V/8 V; Test Circuit 2
Drain OFF Leakage I _D (OFF)						V _D = 8 V/0 V, V _S = 0 V/8 V; Test Circuit 3
ADG408	±1	±100	±1	±100	nA max	V _S = V _D = 8 V/0 V; Test Circuit 4
ADG409	±1	±50	±1	±50	nA max	
Channel ON Leakage I _D , I _S (ON)						
ADG408	±1	±100	±1	±100	nA max	
ADG409	±1	±50	±1	±50	nA max	
DIGITAL INPUTS						
Input High Voltage, V _{INH}	2.4		2.4		V min	V _{IN} = 0 or V _{DD} f = 1 MHz
Input Low Voltage, V _{INL}	0.8		0.8		V max	
Input Current						
I _{INL} or I _{INH}	±10		±10		μA max	
C _{IN} , Digital Input Capacitance	8		8		pF typ	
DYNAMIC CHARACTERISTICS ²						
t _{TRANSITION}	130		130		ns typ	R _L = 300 Ω, C _L = 35 pF; V _{S1} = 8 V/0 V, V _{S8} = 0 V/8 V; Test Circuit 5
t _{OPEN}	10		10		ns typ	R _L = 300 Ω, C _L = 35 pF; V _S = 5 V; Test Circuit 6
t _{ON} (EN)	140		140		ns typ	R _L = 300 Ω, C _L = 35 pF; V _S = 5 V; Test Circuit 7
t _{OFF} (EN)	60		60		ns typ	R _L = 300 Ω, C _L = 35 pF; V _S = 5 V; Test Circuit 7
Charge Injection	5		5		pC typ	V _S = 0 V, R _S = 0 Ω, C _L = 10 nF; Test Circuit 8
OFF Isolation	−75		−75		dB typ	R _L = 1 kΩ, f = 100 kHz; V _{EN} = 0 V; Test Circuit 9
Channel-to-Channel Crosstalk	85		85		dB typ	R _L = 1 kΩ, f = 100 kHz; Test Circuit 10
C _S (OFF)	11		11		pF typ	f = 1 MHz
C _D (OFF)						f = 1 MHz
ADG408	40		40		pF typ	
ADG409	20		20		pF typ	
C _D , C _S (ON)						f = 1 MHz
ADG408	54		54		pF typ	
ADG409	34		34		pF typ	
POWER REQUIREMENTS						
I _{DD}	1		1		μA typ	V _{IN} = 0 V, V _{EN} = 0 V
	5		5		μA max	
I _{DD}	100		100		μA typ	V _{IN} = 0 V, V _{EN} = 2.4 V
	200	500	200	500	μA max	

NOTES

¹Temperature ranges are as follows: B Version: -40°C to +85°C; T Version: -55°C to +125°C.²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG408/ADG409

ABSOLUTE MAXIMUM RATINGS¹

(T_A = 25°C, unless otherwise noted.)

V _{DD} to V _{SS}	44 V
V _{DD} to GND	–0.3 V to +25 V
V _{SS} to GND	+0.3 V to –25 V
Analog, Digital Inputs ²	V _{SS} – 2 V to V _{DD} + 2 V or 20 mA, Whichever Occurs First
Continuous Current, S or D	20 mA
Peak Current, S or D	
(Pulsed at 1 ms, 10% Duty Cycle max)	40 mA
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Extended (T Version)	–55°C to +125°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
CERDIP Package, Power Dissipation	900 mW
θ _{JA} , Thermal Impedance	76°C/W
Lead Temperature, Soldering (10 sec)	300°C
PDIP Package, Power Dissipation	470 mW
θ _{JA} , Thermal Impedance	117°C/W
Lead Temperature, Soldering (10 sec)	260°C
TSSOP Package, Power Dissipation	450 mW
θ _{JA} , Thermal Impedance	155°C/W
θ _{JC} , Thermal Impedance	50°C/W
SOIC Package, Power Dissipation	600 mW
θ _{JA} , Thermal Impedance	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

NOTES

¹ Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

² Overvoltages at A, EN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

ORDERING GUIDE

Model ¹	Temperature Range	Package Option ²
ADG408BN	–40°C to +85°C	N-16
ADG408BR	–40°C to +85°C	R-16A
ADG408BRU	–40°C to +85°C	RU-16
ADG408TQ	–55°C to +125°C	Q-16
ADG409BN	–40°C to +85°C	N-16
ADG409BR	–40°C to +85°C	R-16A
ADG409BRU	–40°C to +85°C	RU-16
ADG409TQ	–55°C to +125°C	Q-16

NOTES

¹ To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.

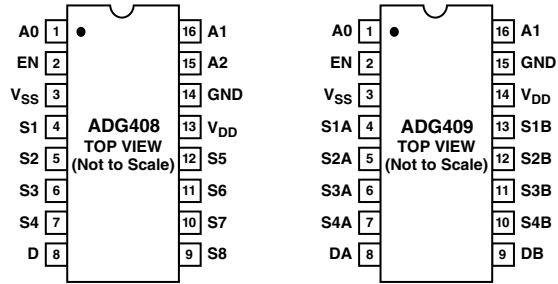
² N = PDIP; Q = CERDIP; R = 0.15" Small Outline IC (SOIC);
RU = Thin Shrink Small Outline Package (TSSOP).

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG408/ADG409 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



PIN CONFIGURATIONS (DIP/SOIC/TSSOP)



ADG408 Truth Table

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

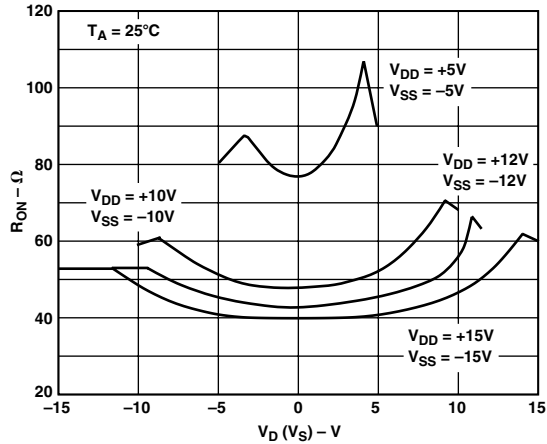
ADG409 Truth Table

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

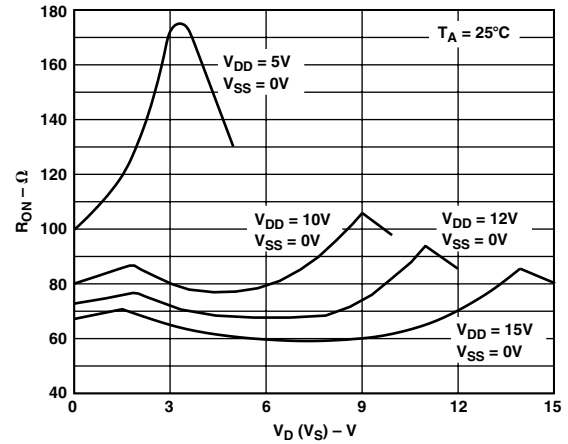
TERMINOLOGY

V_{DD}	Most positive power supply potential.
V_{SS}	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to ground.
GND	Ground (0 V) reference.
R_{ON}	Ohmic resistance between D and S.
ΔR_{ON}	Difference between the R_{ON} of any two channels.
I_S (OFF)	Source leakage current when the switch is off.
I_D (OFF)	Drain leakage current when the switch is off.
I_D, I_S (ON)	Channel leakage current when the switch is on.
V_D (V_S)	Analog voltage on terminals D, S.
C_S (OFF)	Channel input capacitance for OFF condition.
C_D (OFF)	Channel output capacitance for OFF condition.
C_D, C_S (ON)	ON switch capacitance.
C_{IN}	Digital input capacitance.
t_{ON} (EN)	Delay time between the 50% and 90% points of the digital input and switch ON condition.
t_{OFF} (EN)	Delay time between the 50% and 90% points of the digital input and switch OFF condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch ON condition when switching from one address state to another.
t_{OPEN}	OFF time measured between the 80% point of both switches when switching from one address state to another.
V_{INL}	Maximum input voltage for Logic 0.
V_{INH}	Minimum input voltage for Logic 1.
I_{INL} (I_{INH})	Input current of the digital input.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an OFF channel.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
I_{DD}	Positive supply current.
I_{SS}	Negative supply current.

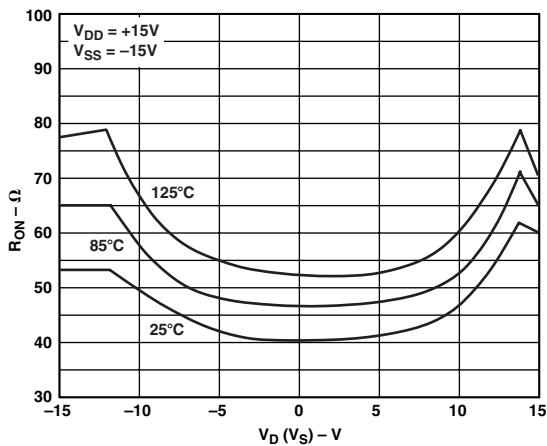
ADG408/ADG409—Typical Performance Characteristics



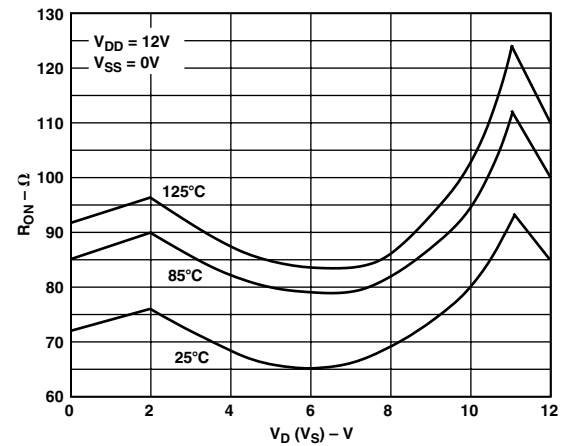
TPC 1. R_{ON} as a Function of V_D (V_S): Dual Supply Voltage



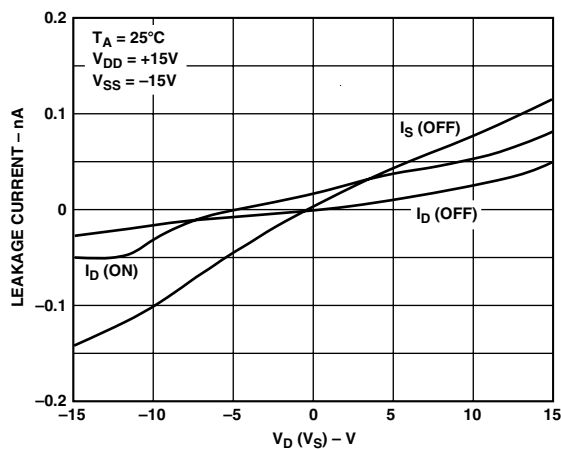
TPC 4. R_{ON} as a Function of V_D (V_S): Single Supply Voltage



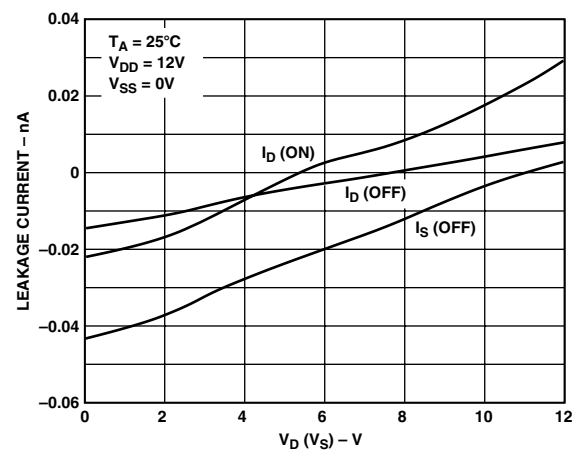
TPC 2. R_{ON} as a Function of V_D (V_S) for Different Temperatures



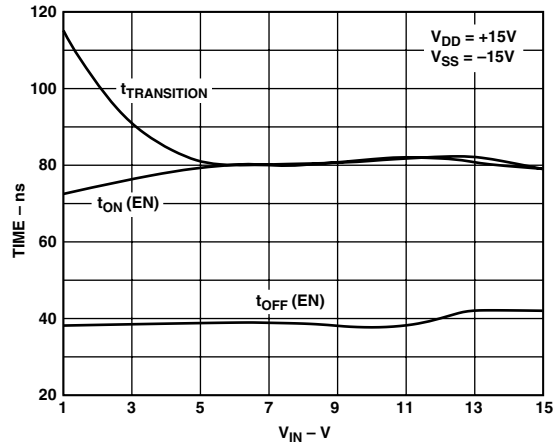
TPC 5. R_{ON} as a Function of V_D (V_S) for Different Temperatures



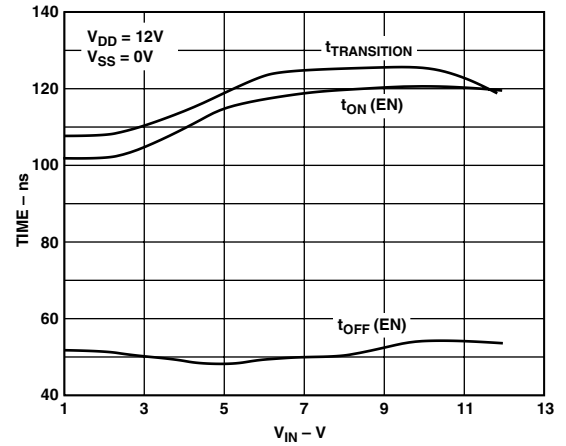
TPC 3. Leakage Currents as a Function of V_D (V_S)



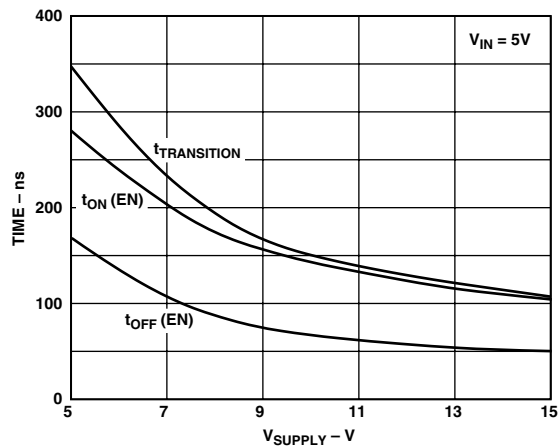
TPC 6. Leakage Currents as a Function of V_D (V_S)



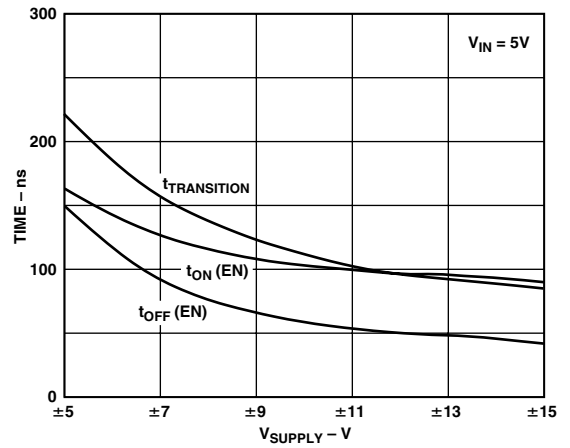
TPC 7. Switching Time vs. V_{IN} (Bipolar Supply)



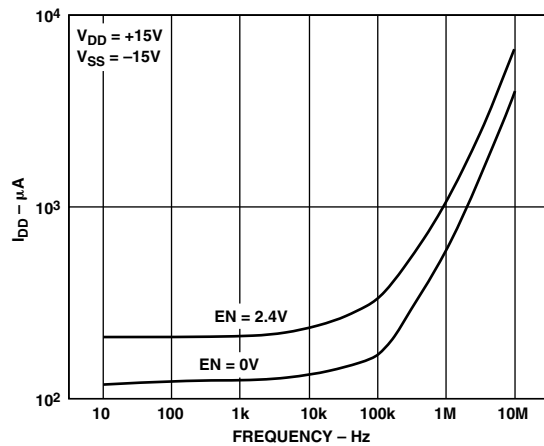
TPC 10. Switching Time vs. V_{IN} (Single Supply)



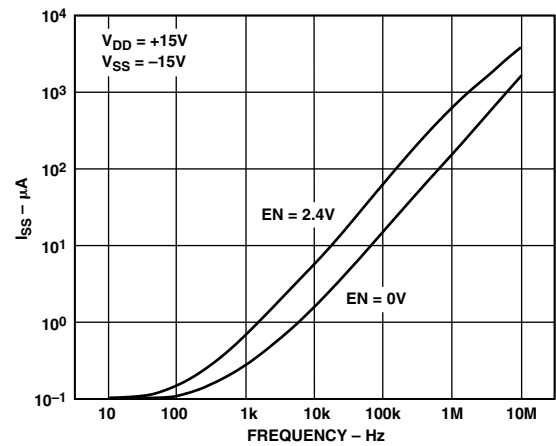
TPC 8. Switching Time vs. Single Supply



TPC 11. Switching Time vs. Bipolar Supply

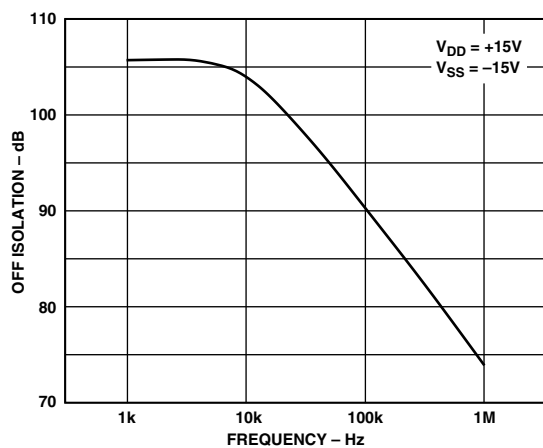


TPC 9. Positive Supply Current vs. Switching Frequency

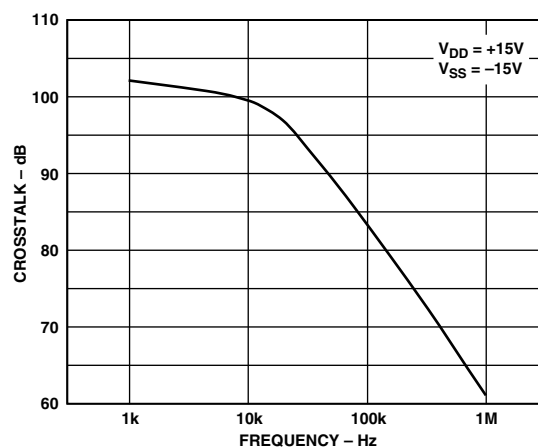


TPC 12. Negative Supply Current vs. Switching Frequency

ADG408/ADG409

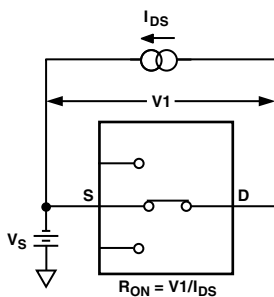


TPC 13. Off Isolation vs. Frequency

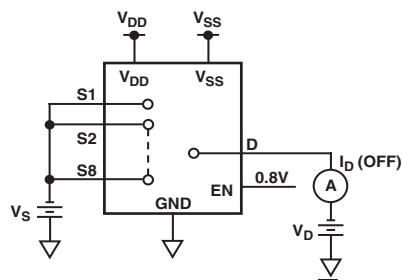


TPC 14. Crosstalk vs. Frequency

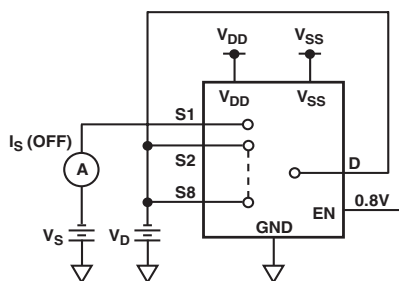
Test Circuits



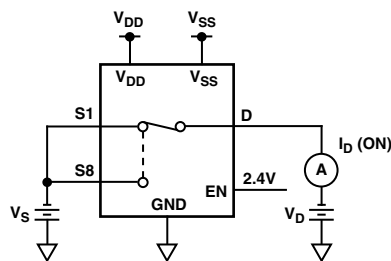
Test Circuit 1. On Resistance



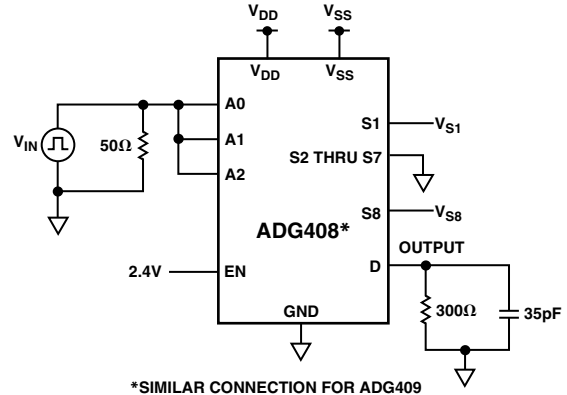
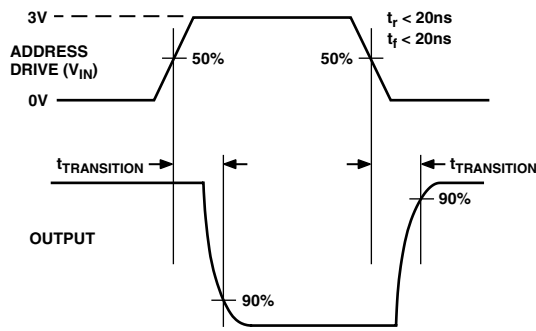
Test Circuit 3. I_D (OFF)



Test Circuit 2. I_S (OFF)

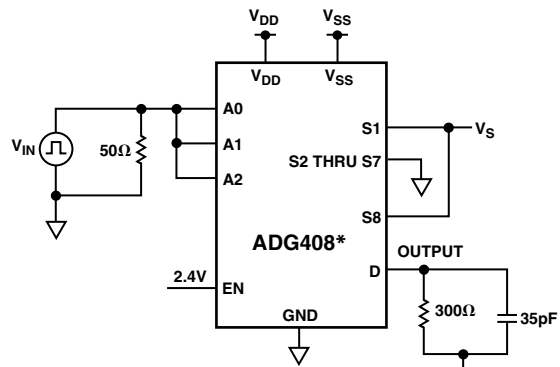
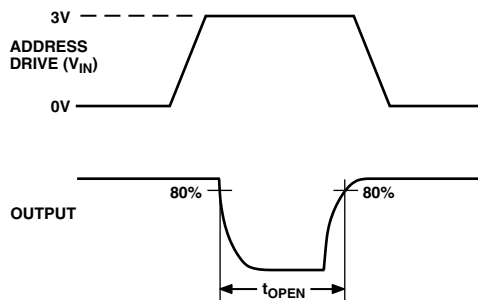


Test Circuit 4. I_D (ON)



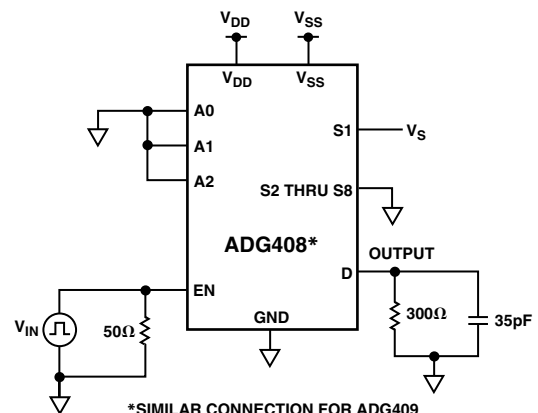
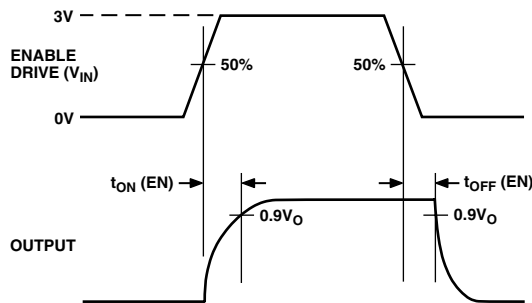
*SIMILAR CONNECTION FOR ADG409

Test Circuit 5. Switching Time of Multiplexer, $t_{\text{TRANSITION}}$



*SIMILAR CONNECTION FOR ADG409

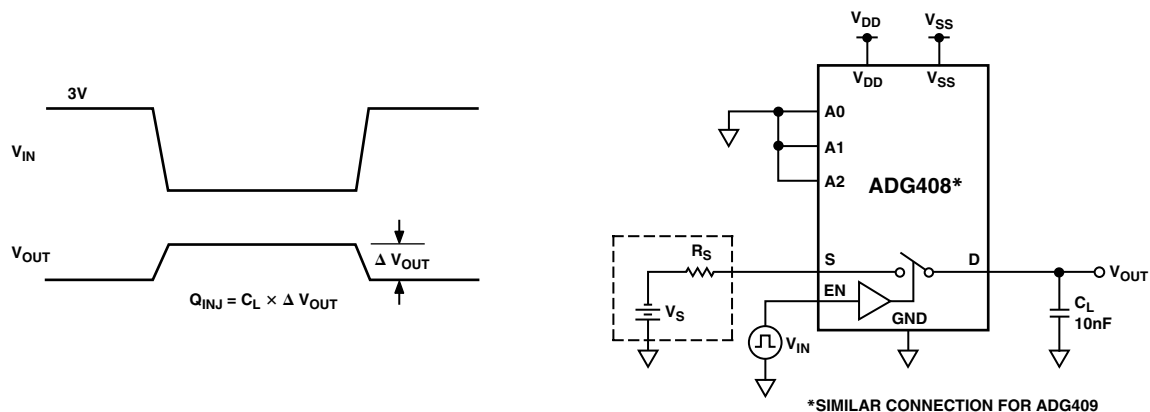
Test Circuit 6. Break-Before-Make Delay, t_{OPEN}



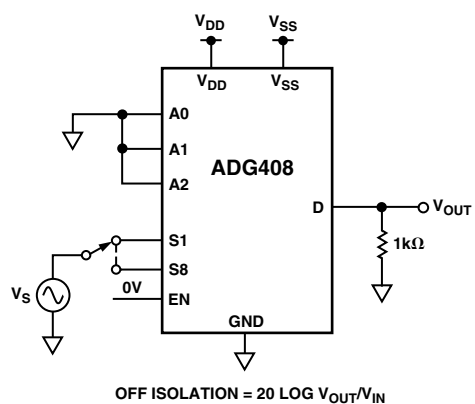
*SIMILAR CONNECTION FOR ADG409

Test Circuit 7. Enable Delay, $t_{\text{ON}}(\text{EN})$, $t_{\text{OFF}}(\text{EN})$

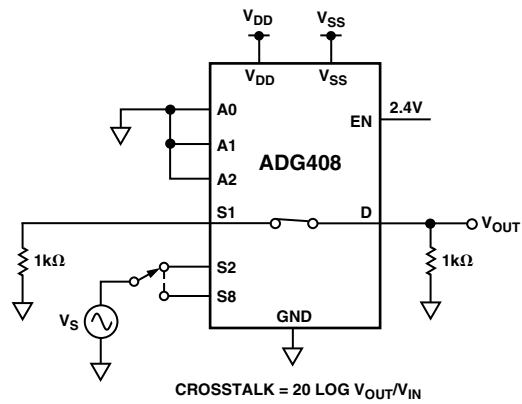
ADG408/ADG409



Test Circuit 8. Charge Injection



Test Circuit 9. OFF Isolation

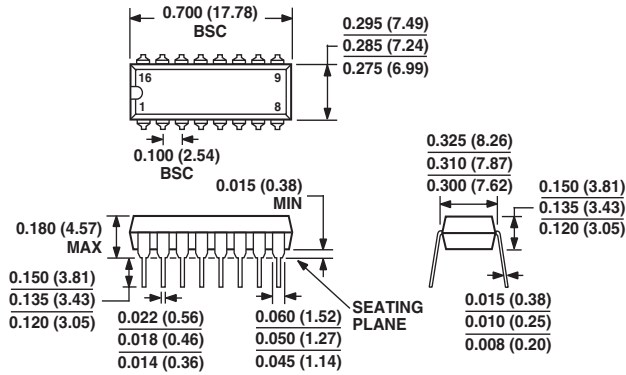


Test Circuit 10. Channel-to-Channel Crosstalk

OUTLINE DIMENSIONS

16-Lead Plastic Dual In-Line Package [PDIP] (N-16)

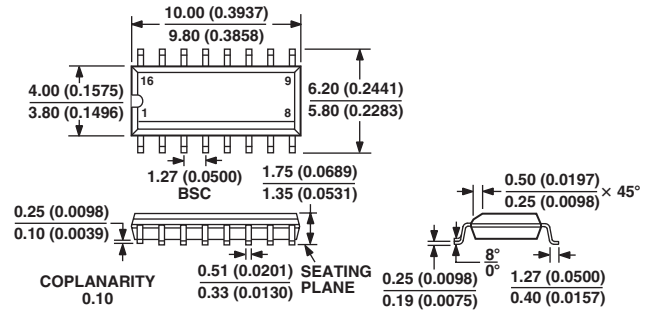
Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-095AC
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

16-Lead Standard Small Outline Package [SOIC] Narrow Body (R-16)

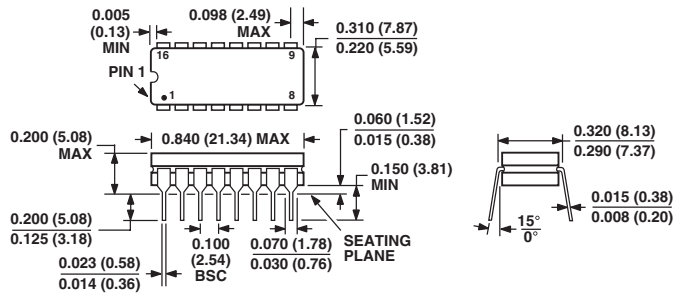
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MS-012AC
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

16-Lead Ceramic Dual In-Line Package [CERDIP] (Q-16)

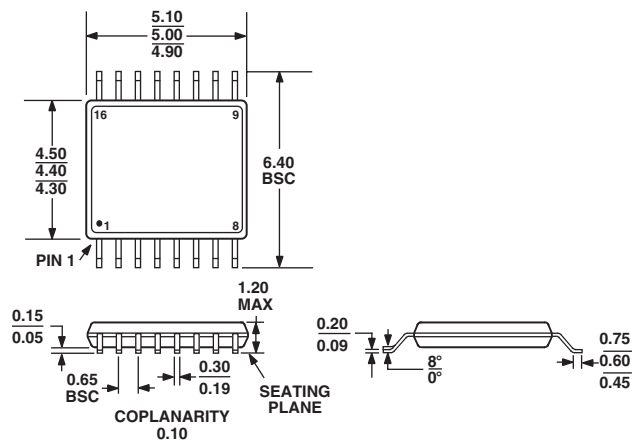
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

16-Lead Thin Shrink Small Outline Package [TSSOP] (RU-16)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-153AB

ADG408/ADG409

Revision History

Location	Page
3/03—Data Sheet changed from REV. A to REV. B.	
Changes to Ordering Guide	4
Updated OUTLINE DIMENSIONS	11

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