

Low-Additive Jitter, Four LVDS Outputs Clock Buffer Evaluation Board

This user's guide describes how to use the CDCLVD1204/CDCLVD2102 evaluation module (EVM) and provides users with guidelines to build their own systems. The EVM schematics and bill of materials are included.

1 Features

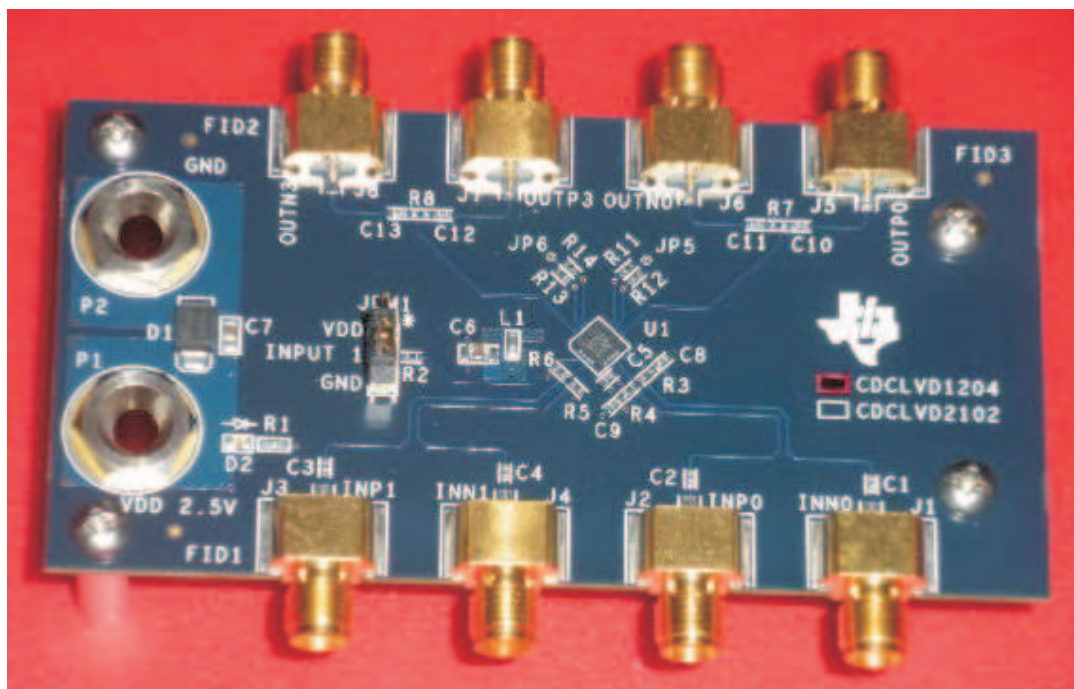


Figure 1. CDCLVD1204/CDCLVD2102 Evaluation Board

- Easy-to-use evaluation board to fan out low-phase noise clocks
- Easy device setup
- Fast configuration
- Control pins configurable through jumpers
- Board powered at 2.5 V
- Single-ended or differential input clocks
- Device supports four LVDS outputs, EVM supports two LVDS outputs

2 General Description

The CDCLVD1204/CDCLVD2102 are high-performance, low-additive jitter clock buffers. They have two universal input buffers that support single-ended or differential clock inputs and are selectable through a control pin (for CDCLVD1204 only). The devices also feature on-chip bias generators that can provide the LVDS common-mode voltage to the device inputs.

The evaluation module (EVM) is designed to demonstrate the electrical performance of the CDCLVD1204 or CDCLVD2102. This fully assembled and factory-tested evaluation board allows complete validation of device functionalities. For optimum performance, the board is equipped with SMA connectors and well-controlled 50-Ω impedance microstrip transmission lines.

3 Signal Path and Control Circuitry

The CDCLVD1204/CDCLVD2102 support single-ended inputs up to 200 MHz and differential inputs up to 800 MHz. Each device provides up to four LVDS outputs operating at the input frequency or frequencies.

For more information, see the CDCLVD1204 ([SCAS898](#)) or CDCLVD2102 ([SCAS904](#)) product data sheet for details.

4 Getting Started

The EVM has self-explanatory labeling and offers almost the same naming convention as used in the data sheets. The labeling words appearing in ***bold italic*** type in this document duplicate the same spelling as the actual labeling on the EVM board. The EVM can be used with single-ended or differential inputs.

5 Device Selection

The same EVM is used for both CDCLVD1204 (2:4 single buffer) and CDCLVD2102 (1:2 dual buffer). The selected box is highlighted in silkscreen for the particular device.

6 Power Supply Connection

Connect the power supply source to the banana plug labeled ***VDD (P1)*** and connect the ground of the power supply source to the ***GND (P2)***. The decoupling capacitors and ferrite bead isolate the EVM power from the device's power pins.

Supply voltage of 2.375 V to 2.625 V can be used for this EVM.

7 Input Clock Selection

The CDCLVD1204/CDCLVD2102EVM offers options of receiving either a differential or a single-ended clock as clock input. The default option is for the differential signal at both device inputs. The inputs can be applied through the SMAs, ***J1, J2*** and/or ***J3, J4***. These inputs are ac coupled to the device inputs and the common-mode voltage for these inputs after the ac-coupling capacitors are provided by 50 Ω (***R3, R4*** and ***R5, R6***) to the device on-chip bias generator (V_{AC_REF}) pins.

CDCLVD1204: Either of the two input clocks can be selected using the jumper ***JPM1***. When ***Input 1 of JPM1*** is connected to ***GND***, IN0 is selected. When Input 1 is connected to ***VDD***, IN1 is selected.

7.1 Configuring Single-Ended Input

For the single-ended clock applied to IN0, remove the capacitors ***C1*** and ***C2***, and replace them with 0-Ω resistors of the same footprint and also remove ***the biasing resistors R3 and R4***. The single-ended signal must be applied to ***INP0 (J2)***, and the DC bias voltage must be applied to ***INN0 (J1)***.

For the single-ended clock applied to IN1, remove the capacitors ***C3*** and ***C4***, replace them with 0-Ω resistors of the same footprint, and also remove ***the biasing resistors R5 and R6***. The single-ended signal must be applied to ***INP1 (J3)***, and the DC bias voltage must be applied to ***INN1 (J4)***.

8 Output Clock

The CDCLVD1204 generates up to four LVDS outputs, and two outputs are available on the EVM (OUT0 and OUT3) through the following SMAs: ***J5*** and ***J6*** for OUT0; ***J7*** and ***J8*** for OUT3. The LVDS outputs are ac coupled to the respective SMAs. Each output pair has an option of 100-Ω termination on the board (***R7*** and ***R8*** – not populated).

Test points are available for OUT1 and OUT2 outputs.

CDCLVD2102: Using the control pin EN (labeled as ***Input 1***), outputs can be disabled or enabled

Table 1. Output Control Table for CDCLVD2102

EN (Input 1)	Clock Outputs
0 (GND)	All outputs disabled (static "0")
OPEN	All outputs enabled
1 (VDD)	OUT0, OUT1 enabled and OUT2, OUT3 disabled (static "0")

9 The EVM Board Schematic

Figure 2 and Figure 3 show the printed circuit board (PCB) schematics .

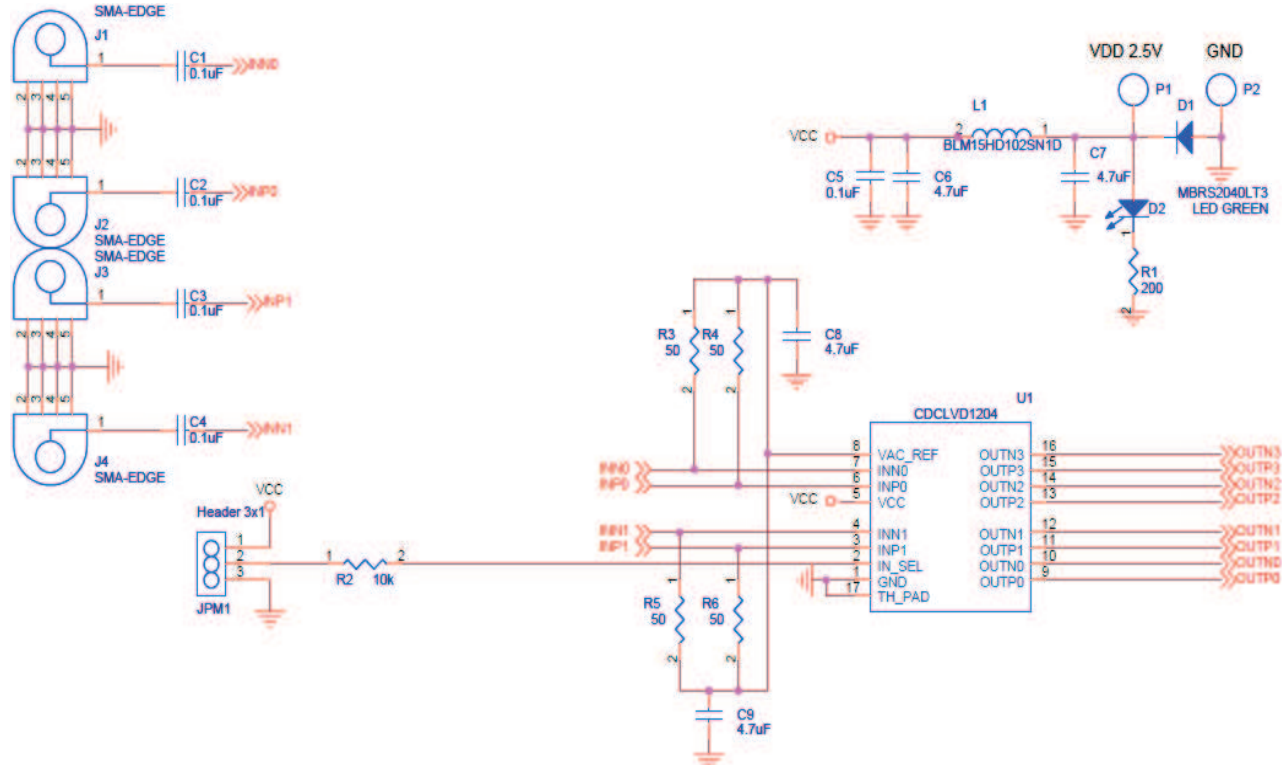


Figure 2. CDCLVD1204/CDCLVD2102EVM Schematic, Sheet 1 of 2

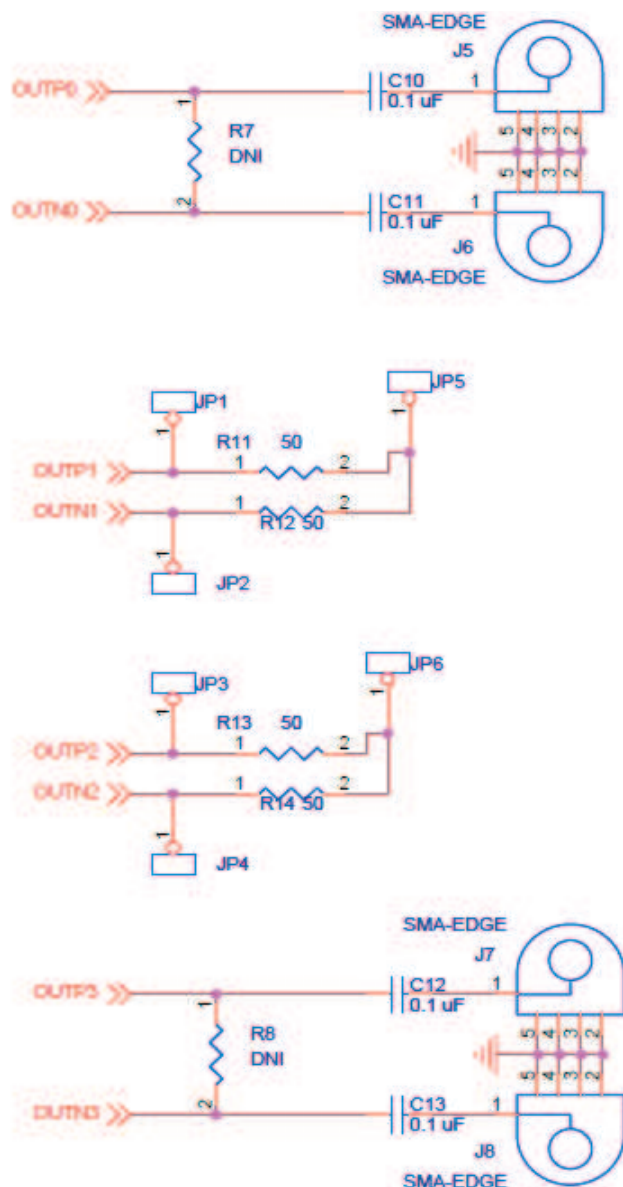


Figure 3. CDCLVD1204/CDCLVD2102EVM Schematic, Sheet 2 of 2

10 Bill of Materials

Table 2. Bill of Materials

Qty	Value	Ref Des	Footprint	Part Category	Manufacturer	Manufacturer Part No
5	0.1 μ F	C1–C5	0402	Capacitors	Venkel	C0402X7R160-104KNE
4	0.1 μ F	C10–C13	0402	Capacitors	Venkel	C0402X7R160-104KNE
2	4.7 μ F	C8, C9	0402	Capacitors	Taiyo Yuden	AMK105BJ475MV-F
2	4.7 μ F	C6, C7	0805	Capacitors	Murata Electronics North America	GRM21BR71C475KA73L
1	10.0K	R2	0402	Resistors	Rohm	MCR01MZPF1002
8	49.9	R3–,R6, R11–,R14	0402	Resistors	Venkel	CR0402-16W-49R9FT
1	200	R1	0603	Resistors	Venkel	CR0603-16W-2000FT
1	1000	L1	0603	Filters	Murata Electronics North America	BLM18HE102SN1D
1	MBRS240LT3G	D1	SMB	Discrete Semiconductor Products	ON Semiconductor	MBRS240LT3G
1	LED - Green	D2	0603	Optoelectronics	Lite-On	LTST-C190GKT
1	CDCLVD2102/ CDCLVD1204	U1	16-HQFN	Integrated Circuits	Texas Instruments	CDCLVD2102/ CDCLVD1204
2	Banana Plug - Metal	P1, P2	4mm	Connectors	Emerson Network Power Connectivity Solutions	108-0740-001
1	1 x 3	JPM1	0.1"	Connectors	Samtec	HTSW-150-07-G-S
8	142-0721-881	J1–J8	RF SMA Edge mount	Connectors	Emerson Network Power Connectivity Solutions	142-0721-881
4	0.75"	Standoffs	Round Threaded	Hardware	Keystone Electronics	2029
4	4-40/0.25"- Screws	Screws	Philips	Hardware	Building Fasteners	PMSSS 440 0025 PH
6	DNI	JP1–JP6				DNI
2	DNI	R7, R8				DNI

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of -0.2 V to Vcc +0.2 V and the output voltage range of -0.2 V to Vcc +0.2 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 120° C. The EVM is designed to operate properly with certain components above 85° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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