

TENTATIVE

TC74HC109P DUAL J-K FLIP FLOP WITH PRESET AND CLEAR

The TC74HC109 is a high speed CMOS DUAL J-K FLIP FLOP fabricated with silicon gate CMOS technology.

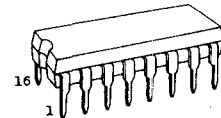
It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

In accordance with the logic level given J and $\bar{K}$ input this device changes state on positive going transition of the clock pulse. CLEAR and PRESET are independent of the clock and accomplished by a low logic level on the corresponding input.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

FEATURES:

- High Speed..... $f_{MAX}=60\text{MHz(Typ.)}$ at $V_{CC}=5\text{V}$
- Low Power Dissipation..... $I_{CC}=2\mu\text{A(Max.)}$ at $T_a=25^\circ\text{C}$
- High Noise Immunity..... $V_{NIH}=V_{NIL}=28\% V_{CC}(\text{Min.})$
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}|=I_{OL}=4\text{mA}(\text{Min.})$
- Balanced Propagation Delays... $t_{PLH}=t_{PHL}$
- Wide Operating Voltage Range... $V_{CC}(\text{opr})=2\text{V} \sim 6\text{V}$
- Pin and Function Compatible with 74LS109



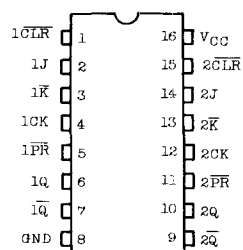
DIP (5-22B)

TRUTH TABLE

INPUTS					OUTPUTS		FUNCTION
CLR	PR	J	$\bar{K}$	CK	Q	$\bar{Q}$	
L	H	X	X	X	L	H	CLEAR
H	L	X	X	X	H	L	PRESET
L	L	X	X	X	H	H	
H	H	L	H	$\downarrow$	Q_n	$\bar{Q}_n$	NO CHANGE
H	H	L	L	$\downarrow$	L	H	
H	H	H	H	$\downarrow$	H	L	
H	H	H	L	$\downarrow$	$\bar{Q}_n$	Q_n	TOGGLE
H	H	X	X	$\downarrow$	Q_n	$\bar{Q}_n$	NO CHANGE

X : Don't care

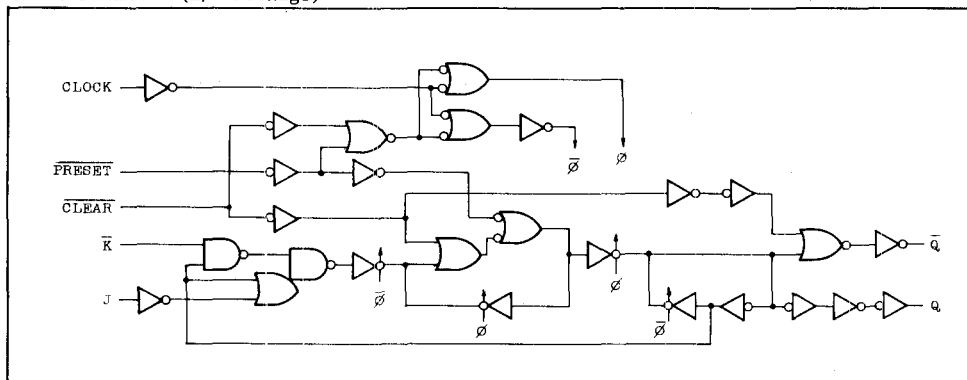
PIN ASSIGNMENT



(Top View)

TC74HC109P

LOGIC DIAGRAM (1/2 Package)



ABSOLUTE MAXIMUM RATINGS

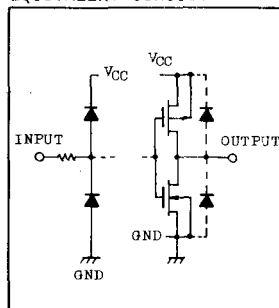
PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V _{CC}	-0.5~7	V
DC Input Voltage	V _{IN}	-0.5~V _{CC} +0.5	V
DC Output Voltage	V _{OUT}	-0.5~V _{CC} +0.5	V
Input Diode Current	I _{IK}	±20	mA
Output Diode Current	I _{OK}	±20	mA
DC Output Current	I _{OUT}	±25	mA
DC V _{CC} /Ground Current	I _{CC}	±50	mA
Power Dissipation	P _D	500*	mW
Storage Temperature	T _{stg}	-65~150	°C
Lead Temperature 10sec	T _L	300	°C

* 500mW in the range of Ta=-40°C~65°C, and from Ta=65°C up to 85°C derating factor of -10mW/°C shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	LIMIT	UNIT
Supply Voltage	V _{CC}	2~6	V
Input Voltage	V _{IN}	0~V _{CC}	V
Output Voltage	V _{OUT}	0~V _{CC}	V
Operating Temperature	T _{opr}	-40~85	°C
Input Rise and Fall Time	t _r , t _f	0~1000 (V _{CC} =2.0V)	ns
		0~500 (V _{CC} =4.5V)	
		0~400 (V _{CC} =6.0V)	

INPUT and OUTPUT EQUIVALENT CIRCUIT



DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C				Ta=-40~85°C		UNIT
				V _{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Input Voltage	V _{IH}			2.0	1.5	-	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	
				6.0	4.2	-	-	4.2	-	
Low-Level Input Voltage	V _{IL}			2.0	-	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	
				6.0	-	-	1.8	-	1.8	
High-Level Output Voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} =-20μA	2.0	1.9	2.0	-	1.9	-	V
				4.5	4.4	4.5	-	4.4	-	
				6.0	5.9	6.0	-	5.9	-	
			I _{OH} =-4mA	4.5	4.18	4.31	-	4.13	-	
			I _{OH} =-5.2mA	6.0	5.68	5.80	-	5.63	-	
Low-Level Output Voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} =20μA	2.0	-	0.0	0.1	-	0.1	V
				4.5	-	0.0	0.1	-	0.1	
				6.0	-	0.0	0.1	-	0.1	
			I _{OL} =4mA	4.5	-	0.17	0.32	-	0.37	
			I _{OL} =5.2mA	6.0	-	0.18	0.32	-	0.37	
Input Leakage Current	I _{IN}	V _{IN} =V _{CC} or GND		6.0	-	-	±0.1	-	±1.0	μA
Quiescent Supply Current	I _{CC}	V _{IN} =V _{CC} or GND		6.0	-	-	2.0	-	20.0	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta=25°C			Ta=-40~85°C		UNIT
			V _{CC}	MIN.	TYP.	MAX.	MIN.	MAX.
Output Transition Time	t _{TLH} t _{THL}		2.0	-	30	75	-	90
			4.5	-	8	15	-	18
			6.0	-	7	13	-	16
Propagation Delay Time (CLOCK - Q, $\bar{Q}$)	t _{pLH} t _{pHL}		2.0	-	80	165	-	200
			4.5	-	21	33	-	40
			6.0	-	18	28	-	34
Propagation Delay Time ($\overline{\text{CLR}}$, $\overline{\text{PR}}$ - Q, $\bar{Q}$)	t _{pLH} t _{pHL}		2.0	-	90	190	-	230
			4.5	-	24	38	-	46
			6.0	-	21	33	-	40

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AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION	Ta=25°C				Ta=-40~85°C		UNIT
			V _{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Maximum Clock Frequency	f _{MAX}		2.0	6	15	-	5	-	MHz
			4.5	30	57	-	25	-	
			6.0	35	65	-	29	-	
Minimum Pulse Width (CLOCK)	t _w (L) t _w (H)		2.0	-	30	75	-	90	ns
			4.5	-	8	15	-	18	
			6.0	-	7	13	-	16	
Minimum Pulse Width (CLR, PR)	t _w (L)		2.0	-	30	75	-	90	
			4.5	-	8	15	-	18	
			6.0	-	7	13	-	16	
Minimum Set-up Time	t _s		2.0	-	35	75	-	90	
			4.5	-	8	15	-	18	
			6.0	-	5	13	-	16	
Minimum Hold Time	t _h		2.0	-	-	0	-	0	
			4.5	-	-	0	-	0	
			6.0	-	-	0	-	0	
Minimum Removal Time (CLR, PR)	t _{rem}		2.0	-	40	100	-	120	
			4.5	-	10	20	-	24	
			6.0	-	9	17	-	21	
Input Capacitance	C _{IN}			-	5	10	-	10	pF
Power Dissipation Capacitance	C _{PD} (1)			-	47	-	-	-	

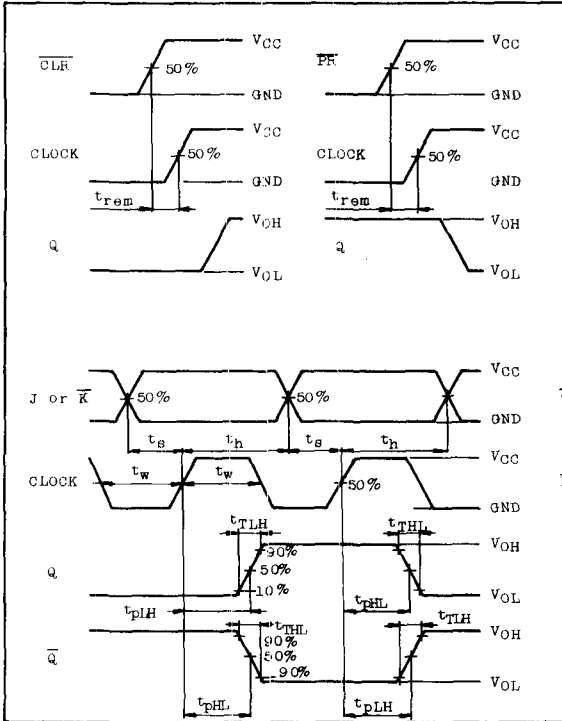
Note (1) C_{PD} is defined as the value of internal equivalent capacitance of IC which is calculated from the operating current consumption without load (refer to Test Circuit).

Average operating current can be obtained by the equation hereunder.

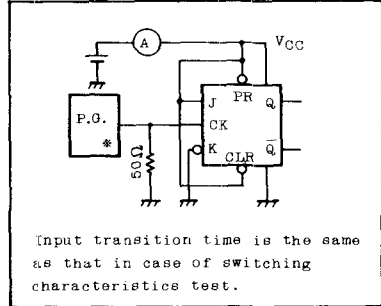
$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \quad (\text{Per FF})$$

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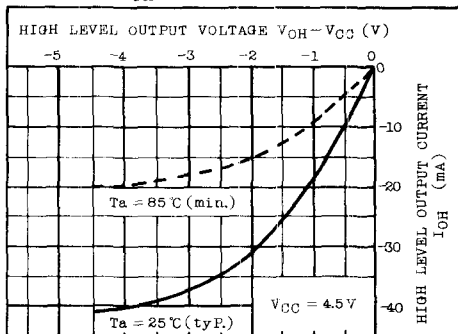
SWITCHING CHARACTERISTICS TEST WAVEFORM



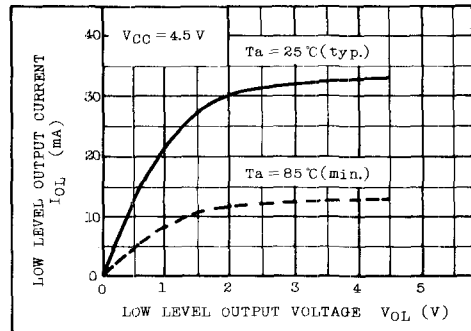
$I_{CC(opr)}$ TEST CIRCUIT



I_{OH} CHARACTERISTICS

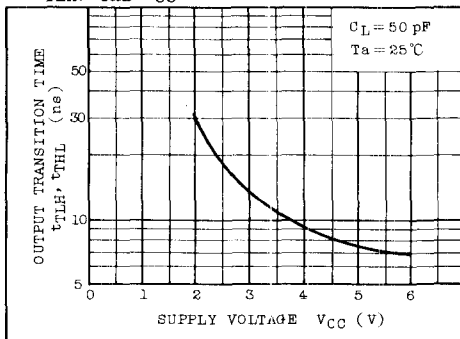


I_{OL} CHARACTERISTICS

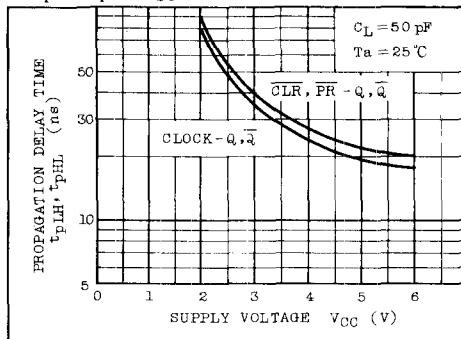


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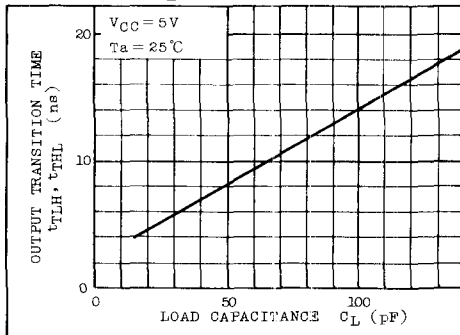
$t_{TLH}, t_{THL}-V_{CC}$ CHARACTERISTICS (TYP.)



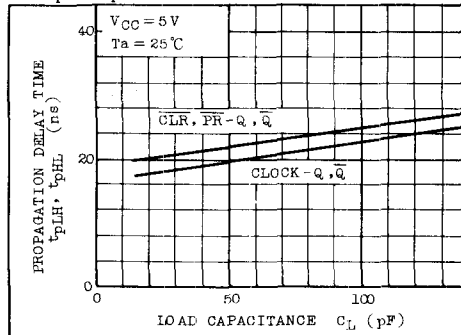
$t_{PLH}, t_{PHL}-V_{CC}$ CHARACTERISTICS (TYP.)



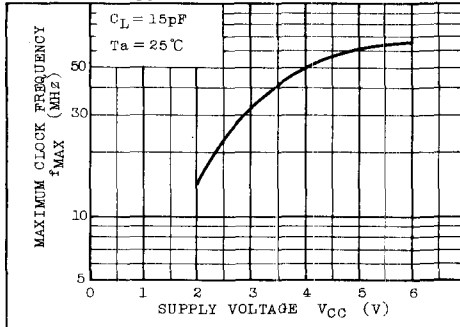
$t_{TLH}, t_{THL}-C_L$ CHARACTERISTICS (TYP.)



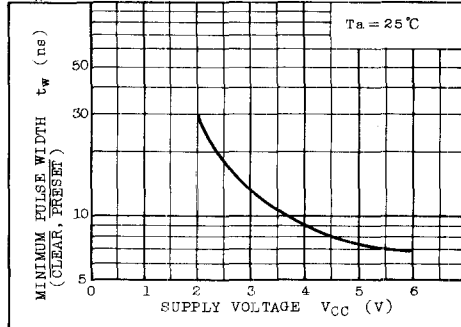
$t_{PLH}, t_{PHL}-C_L$ CHARACTERISTICS (TYP.)



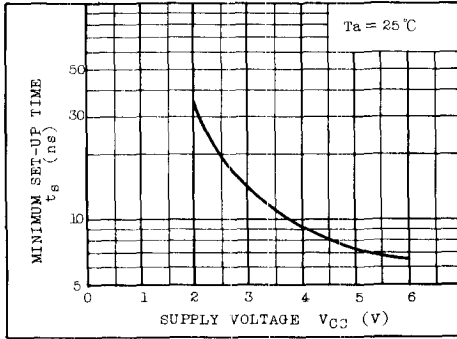
$f_{MAX}-V_{CC}$ CHARACTERISTICS (TYP.)



$t_W(\overline{CL}, \overline{PR})-V_{CC}$ CHARACTERISTICS (TYP.)



$t_{S-V_{CC}}$ CHARACTERISTICS (TYP.)



$t_{rem}(\overline{CL}, \overline{PR}) - V_{CC}$ CHARACTERISTICS (TYP.)

