MOSFET

Metal Oxide Semiconductor Field Effect Transistor

OptiMOS™

OptiMOS™ Power-Transistor, 60 V

IPD025N06N

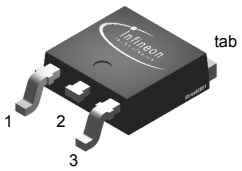
Data Sheet

Rev. 2.5
Final

Power Management & Multimarket

1 Description

D-PAK



Features

- Optimized for synchronous rectification
- 100% avalanche tested
- Superior thermal resistance
- N-channel, normal level
- Qualified according to JEDEC[1] for target applications
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

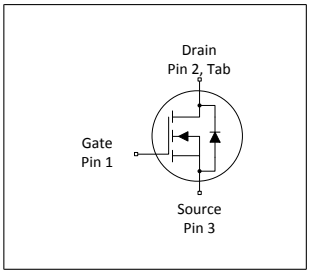


Table 1 Key Performance Parameters

Parameter	Value	Unit
V_{DS}	60	V
$R_{DS(on),max}$	2.5	mΩ
I_D	90	A
Q_{OSS}	81	nC
Q_G(0V..10V)	71	nC

Type / Ordering Code	Package	Marking	Related Links
IPD025N06N	PG-TO252-3	025N06N	-

[1] J-STD20 and JESD22

Table of Contents

2 Maximum ratings

at T_j = 25 °C, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	- - -	- - -	90 90 26	A	V_{GS}=10 V, T_C=25 °C V_{GS}=10 V, T_C=100 °C V_{GS}=10 V, T_C=25 °C, R_{thJA} =50K/W
Pulsed drain current[1]	$I_{D,pulse}$	-	-	360	A	T_C=25 °C
Avalanche energy, single pulse[2]	E_{AS}	-	-	210	mJ	I_D=90 A, R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	- -	- -	167 3.0	W	T_C=25 °C T_A=25 °C, R_{thJA}=50 K/W
Operating and storage temperature	T_j, T_{stg}	-55	-	175	°C	IEC climatic category; DIN IEC 68-1: 55/175/56

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	0.5	0.9	K/W	-
Device on PCB, minimal footprint	R_{thJA}	-	-	62	K/W	-
Device on PCB, 6 cm² cooling area[3]	R_{thJA}	-	-	40	K/W	-
Soldering temperature, wave and reflow soldering are allowed	T_{sold}	-	-	260	°C	Reflow MSL1

[1] See figure 3 for more detailed information
[2] See figure 13 for more detailed information
[3] Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

4 Electrical characteristics

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	2.1	2.8	3.3	V	V_{DS}=V_{GS}, I_D=95 µA
Zero gate voltage drain current	I_{DSS}	- -	0.5 10	1 100	µA	V_{DS}=60 V, V_{GS}=0 V, T_j=25 °C V_{DS}=60 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	- -	2.1 2.7	2.5 3.8	mΩ	V_{GS}=10 V, I_D=90 A V_{GS}=6 V, I_D=22.5 A
Gate resistance[1)]	R_G	-	1.7	2.6	Ω	-
Transconductance	g_{fs}	80	160	-	S	|V_{DS}|>2|I_D|$R_{DS(on)max}$, I_D=90 A

Table 5 Dynamic characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	5200	6500	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Output capacitance	C_{oss}	-	1200	1500	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Reverse transfer capacitance	C_{rss}	-	48	96	pF	V_{GS}=0 V, V_{DS}=30 V, f=1 MHz
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=90 A, $R_{G,ext}$,ext=1.6 Ω
Rise time	t_r	-	20	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=90 A, $R_{G,ext}$,ext=1.6 Ω
Turn-off delay time	$t_{d(off)}$	-	34	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=90 A, $R_{G,ext}$,ext=1.6 Ω
Fall time	t_f	-	12	-	ns	V_{DD}=30 V, V_{GS}=10 V, I_D=90 A, $R_{G,ext}$,ext=1.6 Ω

[1)] Defined by design. Not subject to production test

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	24	-	nC	V_{DD}=30 V, I_D=90 A, V_{GS}=0 to 10 V
Gate charge at threshold	$Q_{g(th)}$	-	14	-	nC	V_{DD}=30 V, I_D=90 A, V_{GS}=0 to 10 V
Gate to drain charge[2)]	Q_{gd}	-	13	17	nC	V_{DD}=30 V, I_D=90 A, V_{GS}=0 to 10 V
Switching charge	Q_{sw}	-	23	-	nC	V_{DD}=30 V, I_D=90 A, V_{GS}=0 to 10 V
Gate charge total	Q_g	-	71	83	nC	V_{DD}=30 V, I_D=90 A, V_{GS}=0 to 10 V
Gate plateau voltage	$V_{plateau}$	-	4.7	-	V	V_{DD}=30 V, I_D=90 A, V_{GS}=0 to 10 V
Gate charge total, sync. FET	$Q_{g(sync)}$	-	62	-	nC	V_{DS}=0.1 V, V_{GS}=0 to 10 V
Output charge[2)]	Q_{oss}	-	81	102	nC	V_{DD}=30 V, V_{GS}=0 V

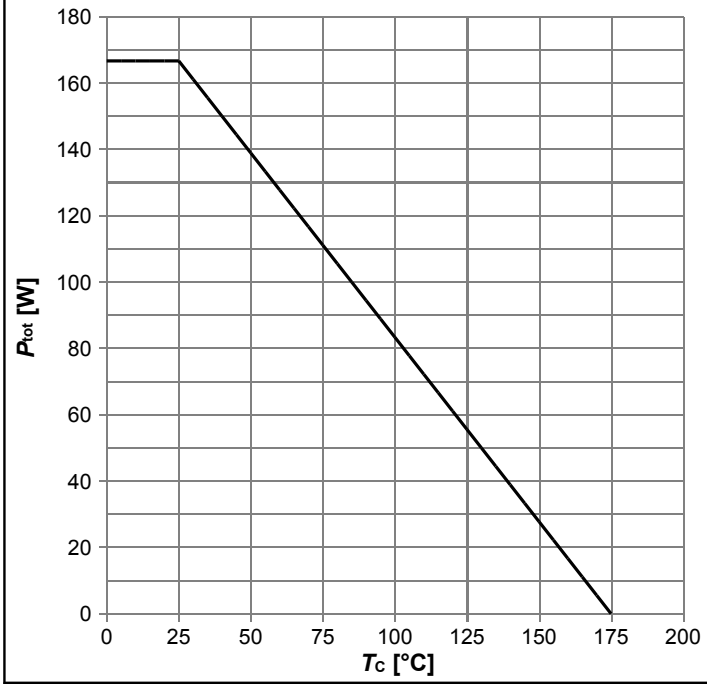
Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	90	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$	-	-	360	A	T_C=25 °C
Diode forward voltage	V_{SD}	-	1.0	1.2	V	V_{GS}=0 V, I_F=90 A, T_j=25 °C
Reverse recovery time[2)]	t_{rr}	-	83	133	ns	V_R=30 V, I_F=I_S, di_F/dt=100 A/µs
Reverse recovery charge	Q_{rr}	-	105	-	nC	V_R=30 V, I_F=I_S, di_F/dt=100 A/µs

[1)] See ″Gate charge waveforms″ for parameter definition
[2)] Defined by design. Not subject to production test

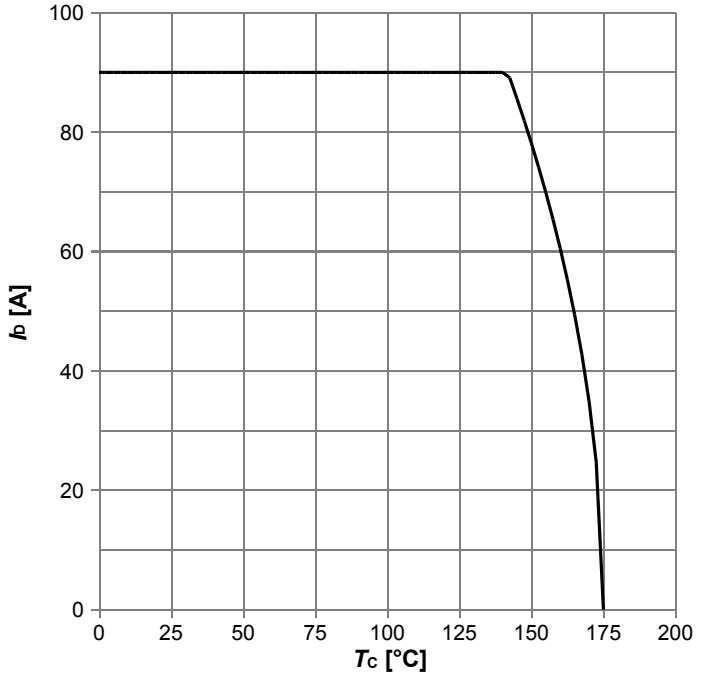
5 Electrical characteristics diagrams

Diagram 1: Power dissipation



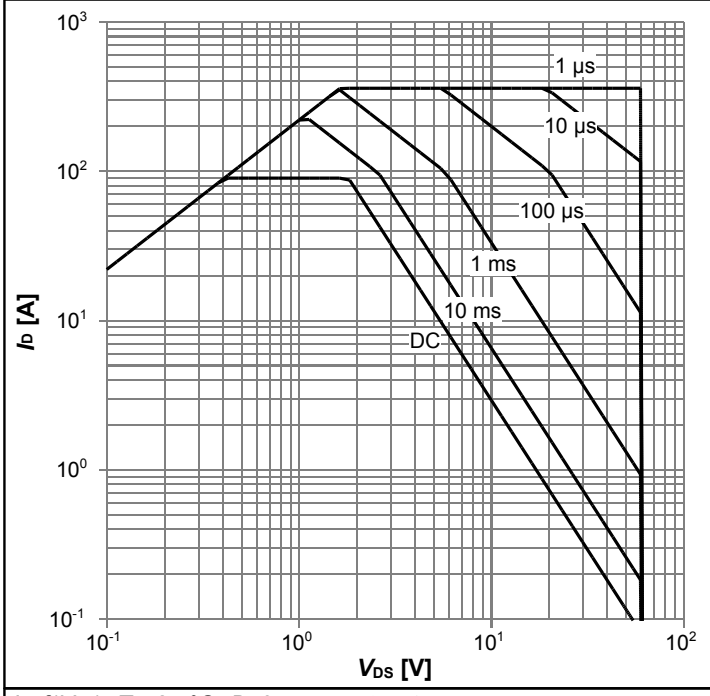
$P_{tot}=f(T_C)$

Diagram 2: Drain current



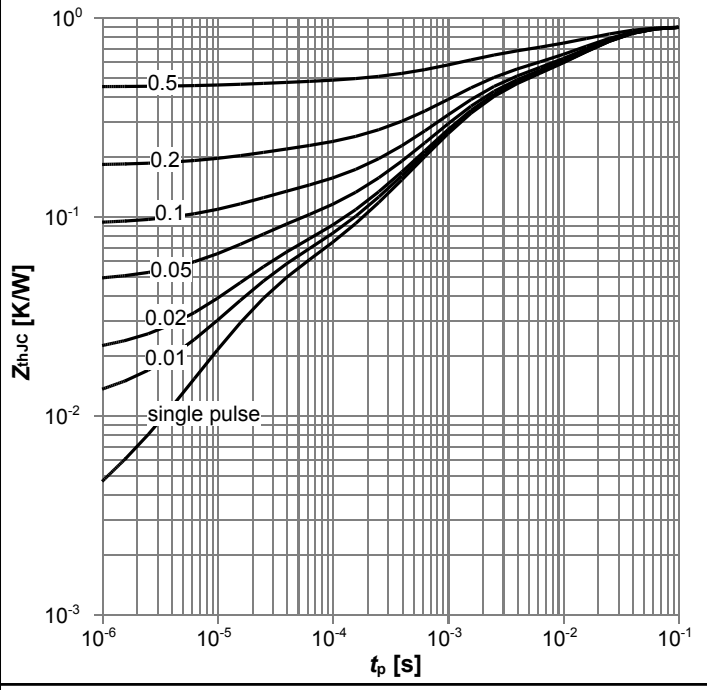
$I_D=f(T_C)$; $V_{GS}\geq 10$ V

Diagram 3: Safe operating area



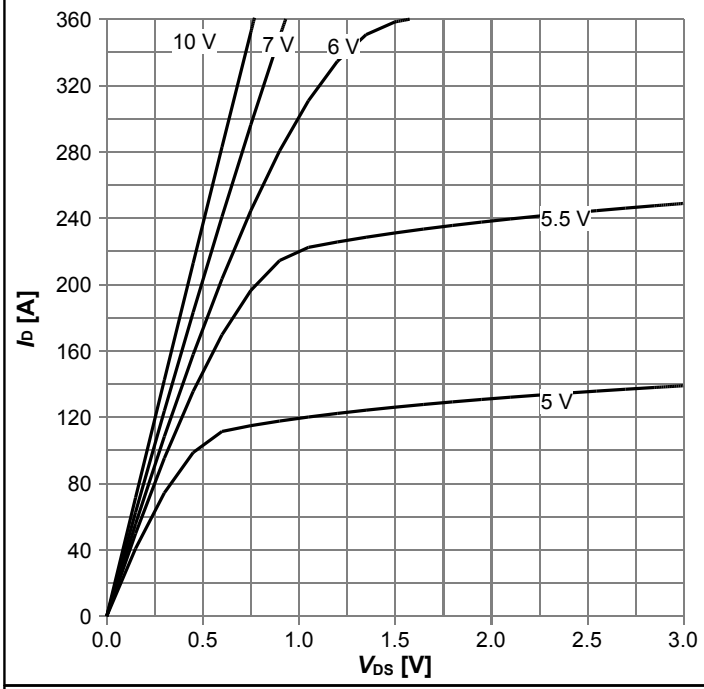
$I_D=f(V_{DS})$; $T_C=25$ °C; $D=0$; parameter: t_p

Diagram 4: Max. transient thermal impedance



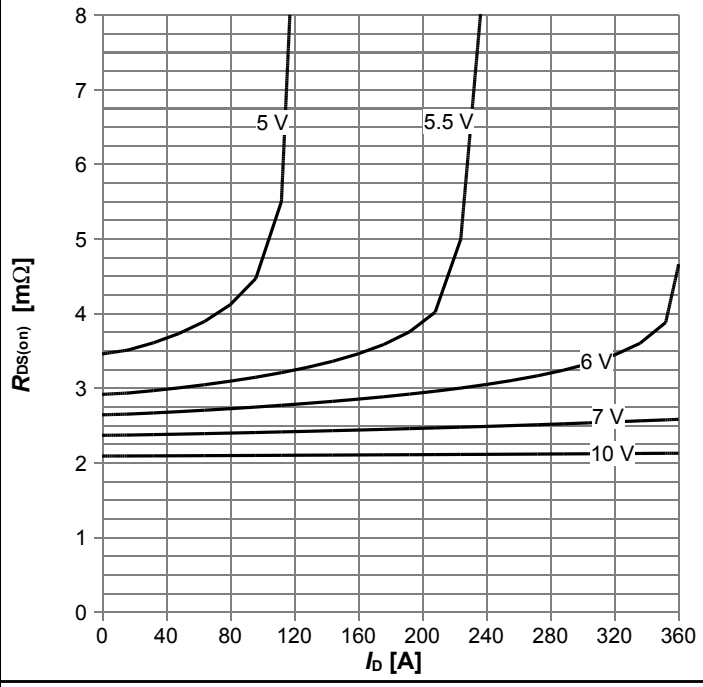
$Z_{thJC}=f(t_p)$; parameter: $D=t_p/T$

Diagram 5: Typ. output characteristics



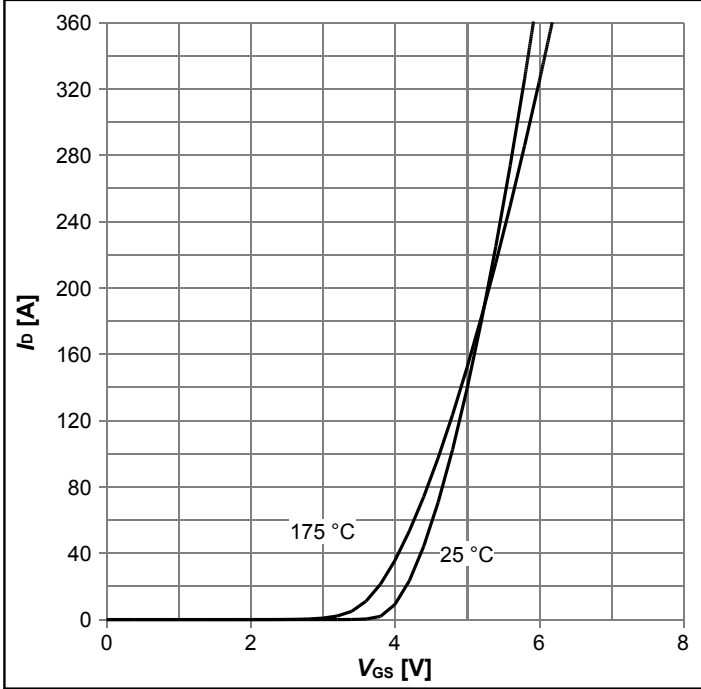
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



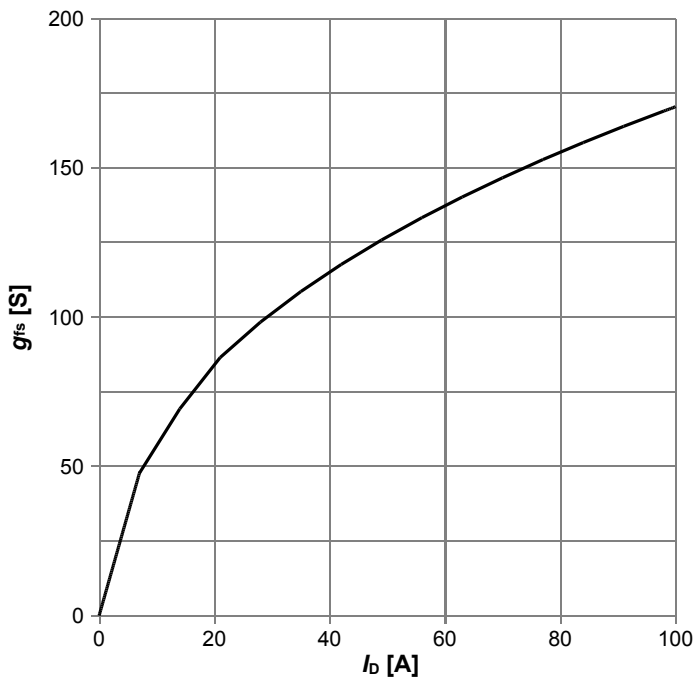
$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



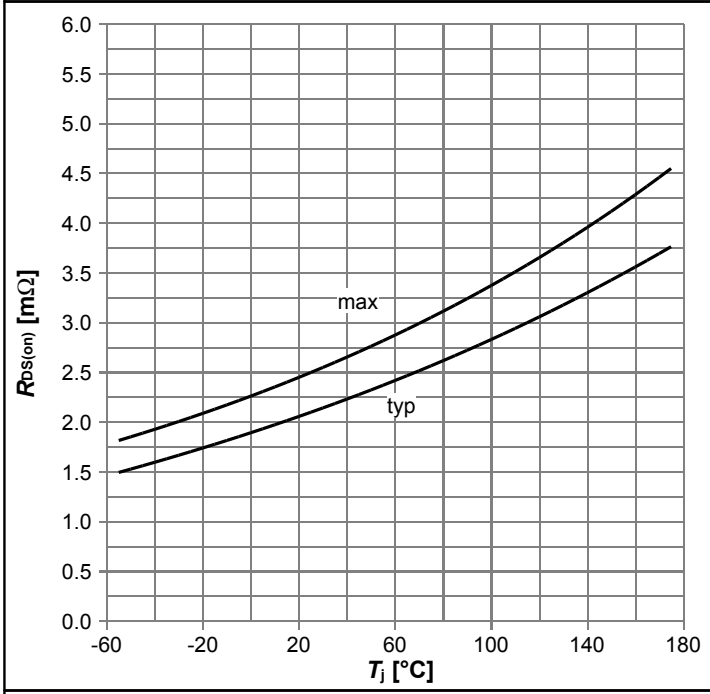
I_D=f(V_{GS}); |V_{DS}|>2|I_D|$R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. forward transconductance



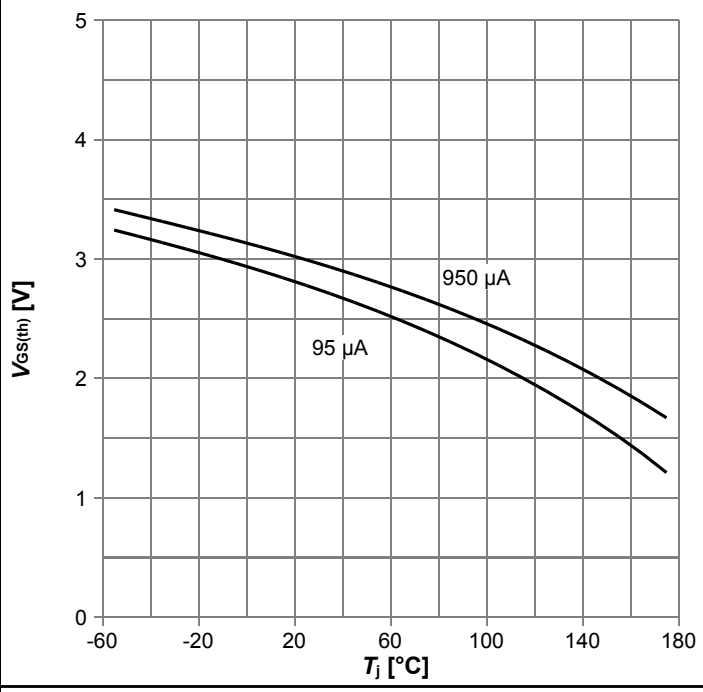
g_{fs}=f(I_D); T_j=25 °C

Diagram 9: Drain-source on-state resistance



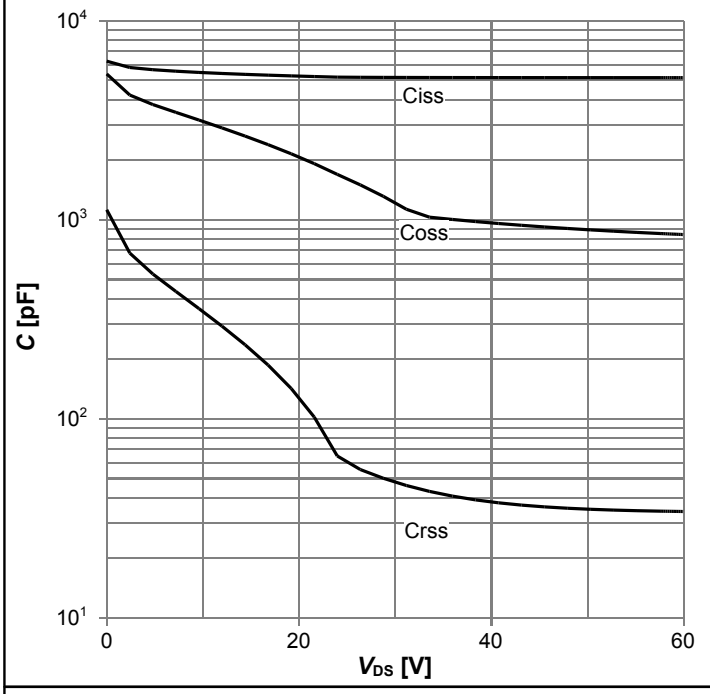
$R_{DS(on)}$=f(T_j); I_D=90 A; V_{GS}=10 V

Diagram 10: Typ. gate threshold voltage



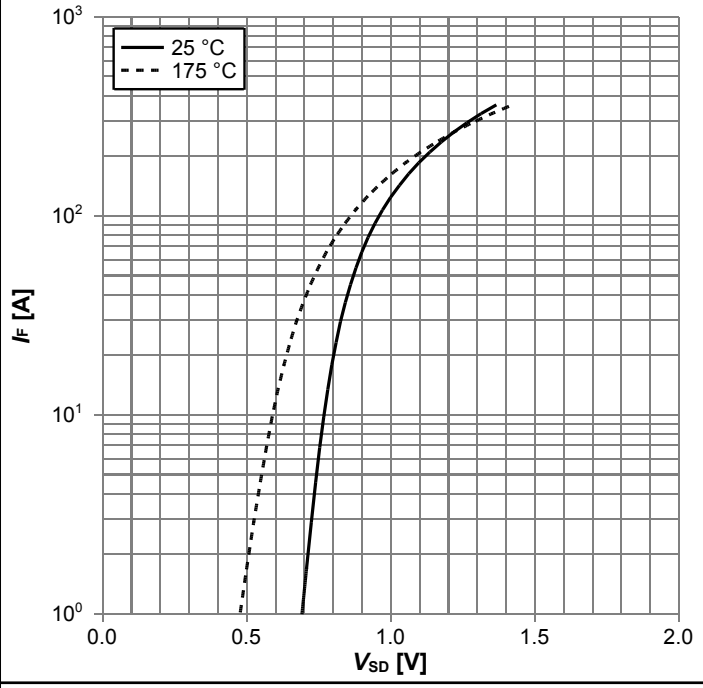
$V_{GS(th)}$=f(T_j); V_{GS}=V_{DS}

Diagram 11: Typ. capacitances



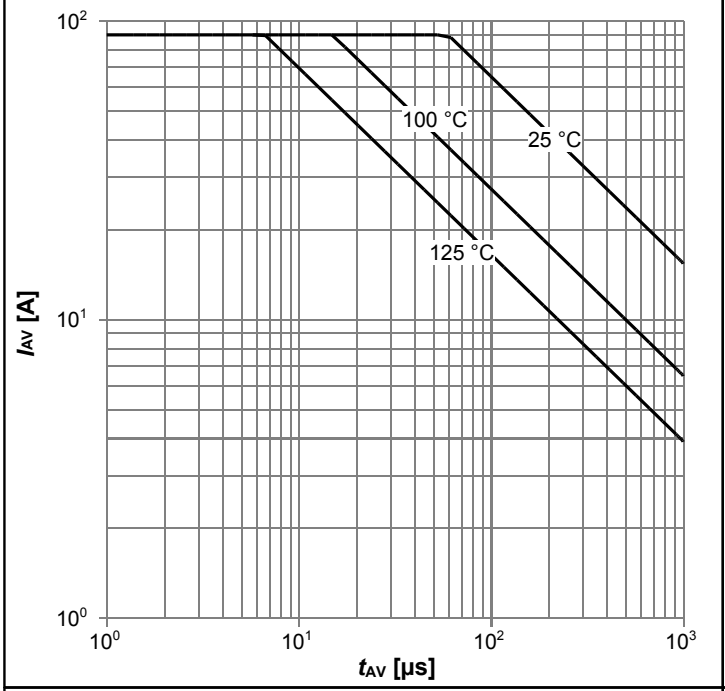
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz

Diagram 12: Forward characteristics of reverse diode



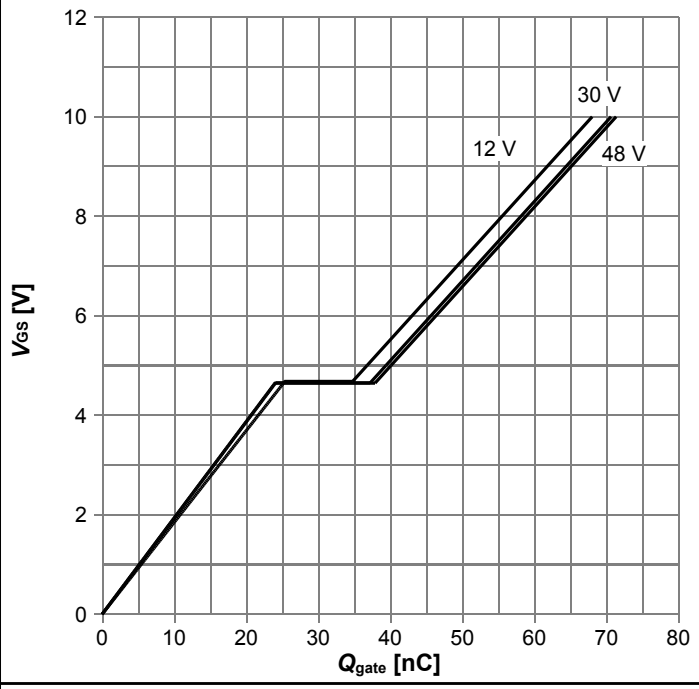
I_F=f(V_{SD}); parameter: T_j

Diagram 13: Avalanche characteristics



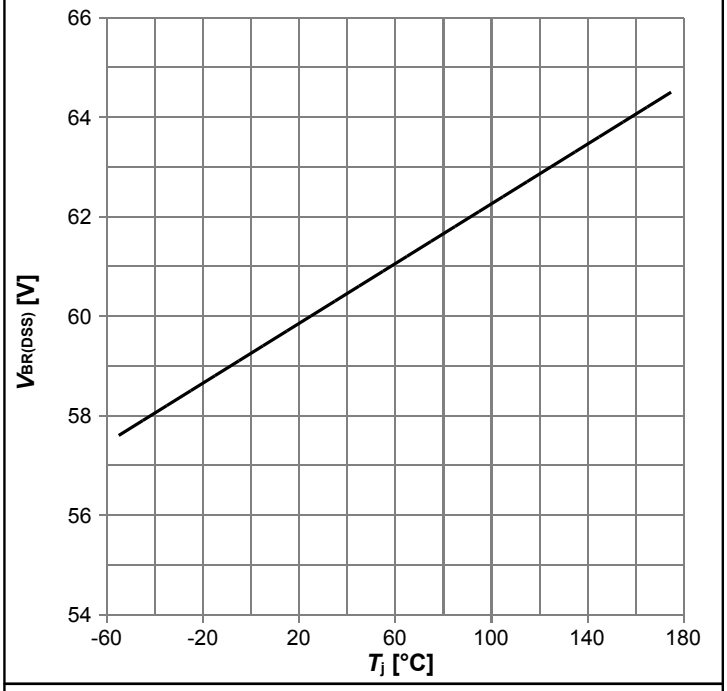
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$

Diagram 14: Typ. gate charge



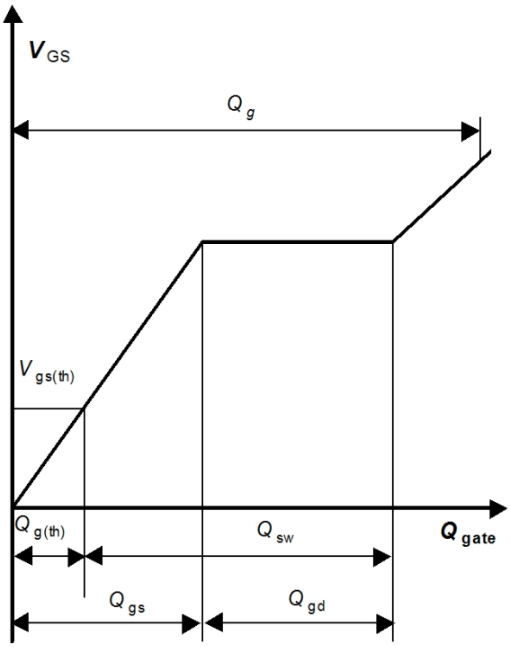
V_{GS}=f(Q_{gate}); I_D=90A pulsed; parameter: V_{DD}

Diagram 15: Drain-source breakdown voltage

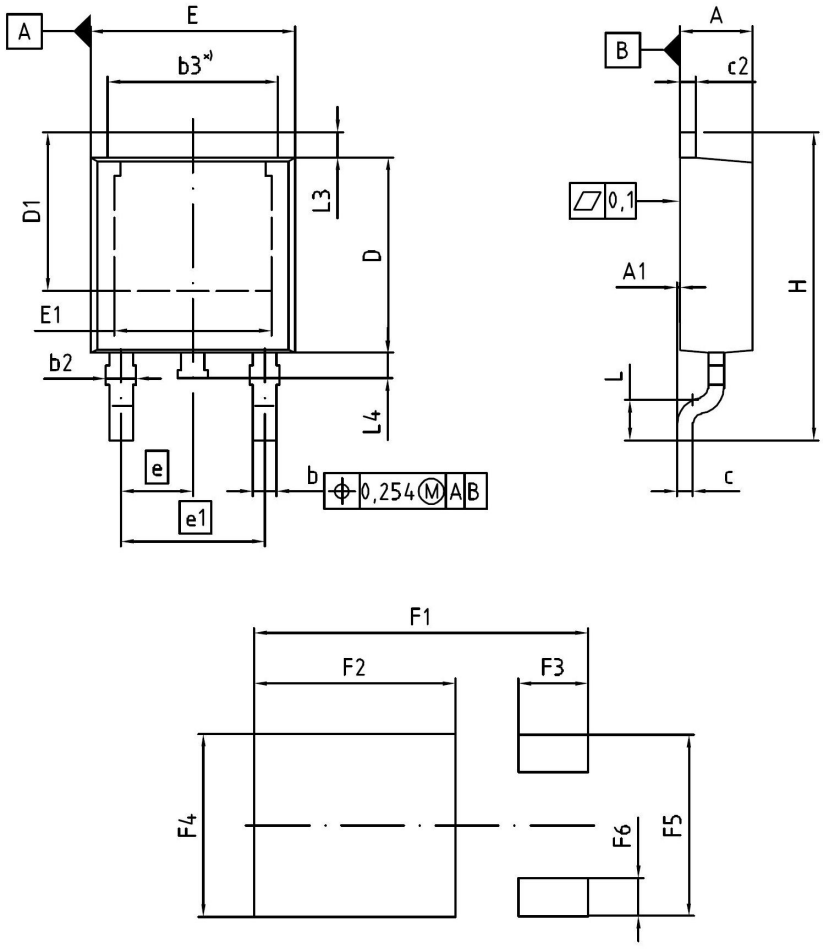


$V_{BR(DSS)}$=f(T_j); I_D=1 mA

Gate charge waveforms



6 Package Outlines



*) mold flash not included

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.16	2.41	0.085	0.095
A1	0.00	0.15	0.000	0.006
b	0.64	0.89	0.025	0.035
b2	0.65	1.15	0.026	0.045
b3	5.00	5.50	0.197	0.217
c	0.46	0.60	0.018	0.024
c2	0.46	0.98	0.018	0.039
D	5.97	6.22	0.235	0.245
D1	5.02	5.84	0.198	0.230
E	6.40	6.73	0.252	0.265
E1	4.70	5.21	0.185	0.205
e	2.29 (BSC)		0.090 (BSC)	
e1	4.57		0.180	
N	3		3	
H	9.40	10.48	0.370	0.413
L	1.18	1.70	0.046	0.067
L3	0.90	1.25	0.035	0.049
L4	0.51	1.00	0.020	0.039
F1	10.60		0.417	
F2	6.40		0.252	
F3	2.20		0.087	
F4	5.80		0.228	
F5	5.76		0.227	
F6	1.20		0.047	

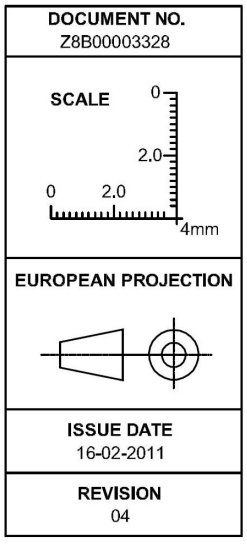


Figure 1 Outline PG-TO252-3, dimensions in mm/inches

Revision History

IPD025N06N

Revision: 2014-07-23, Rev. 2.5

Previous Revision		
Revision	Date	Subjects (major changes since last revision)
2.5	2014-07-23	Rev.2.5

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