

### FEATURES

- Provides 3 output voltages (5.1 V, 15.3 V, -10.2 V) from one 3 V input supply
- Power efficiency optimized for use with TFT in mobile phones
- On-board socket for evaluation of multiple ICs
- Shutdown line
- Options to use external LDO

### PACKAGE CONTENTS

- ADM8832 evaluation board
- ADP8832 evaluation board data sheet
- ADM8832 data sheet

### GENERAL DESCRIPTION

The ADM8832 evaluation board allows the [ADM8832](#) TFT color panel charge pump regulator to be quickly and easily evaluated.

The evaluation board allows all of the input and output functions to be exercised without the need for external components.

Full details about the part are available in the ADM8832 data sheet, which should be consulted when using the EVAL-ADM8832.

### FUNCTIONAL BLOCK DIAGRAM

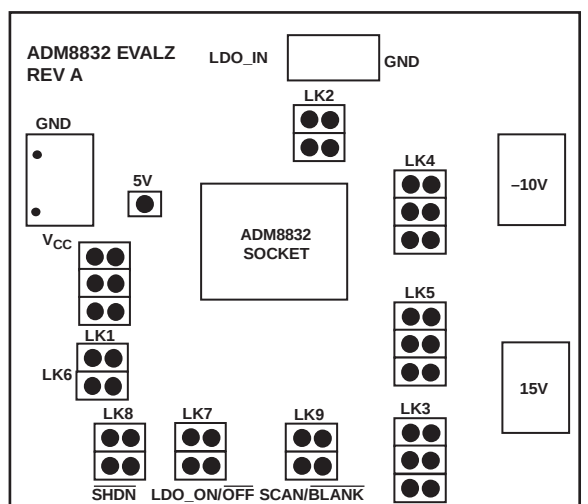


Figure 1.

### Rev. 0

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REVISION HISTORY

6/08—Revision 0: Initial Version

## EVALUATION BOARD HARDWARE

The ADM8832 evaluation board contains the following main components, which can be identified from the block diagram and the schematic shown in Figure 1 and Figure 2, respectively:

- 20-lead LFCSP socket to hold the ADM8832 IC
- 9 jumper points to facilitate the connection of external LDOs, clock sources, and external loads
- 1 SMB connector for reliable logic signal connection
- 9 test points for signal connection and measurement
- A large patchwork area to facilitate the addition of extra components to the ADM8832 evaluation board

## EVALUATION BOARD CONNECTORS AND JUMPERS

The function of the various connectors and jumpers on the evaluation board is explained in Table 1, Table 2, and Table 3.

**Table 1. Evaluation Board Power Connectors**

| Connector | Function                                           |
|-----------|----------------------------------------------------|
| J1        | Supply to ADM8832 (3 V nominal)                    |
| J2        | External Source (can be regulated by on-board LDO) |

**Table 2. SMB Connection**

| Jumper | Pin   | Function                                 | Logic Level (High = 3 V, Low = 0 V) |
|--------|-------|------------------------------------------|-------------------------------------|
| SK1    | CLKIN | External clock used during blanking mode | External                            |

**Table 3. Jumpers (Links)**

| Jumper | Description                                                                                                                            | Default Status |
|--------|----------------------------------------------------------------------------------------------------------------------------------------|----------------|
| LK1    | Connects to optional external 5 V loads (R1, R2, and R3).                                                                              |                |
| LK1A   | Connects +5VOUT (Pin 4) to 620 $\Omega$ resistor (R1) to GND. (This generates a maximum scanning mode load current of 8 mA.)           | Removed        |
| LK1B   | Connects +5VOUT (Pin 4) to 1 k $\Omega$ resistor (R2) to GND. (This generates a load current of 5 mA.)                                 | Removed        |
| LK1C   | Connects +5VOUT (Pin 4) to 24.9 k $\Omega$ resistor (R3) to GND. (This generates a maximum blanking mode load current of 200 $\mu$ A.) | Removed        |
| LK2A   | Connects VOUT (Pin 2) to LDO_IN (Pin 3).                                                                                               | Inserted       |
| LK2B   | Connects external source (J2) to LDO_IN (Pin 3).                                                                                       | Removed        |
| LK3A   | Connects CLKIN (Pin 9) to VCC.                                                                                                         | Removed        |
| LK3B   | Connects CLKIN (Pin 9) to GND.                                                                                                         | Removed        |
| LK3C   | Connects CLKIN (Pin 9) to SK1.                                                                                                         | Inserted       |
| LK4A   | Connects –10VOUT (Pin 17) to 100 k $\Omega$ resistor (R6) to GND. (This generates a max load current of 100 $\mu$ A.)                  | Inserted       |
| LK4B   | Connects –10VOUT (Pin 17) to 1 M $\Omega$ resistor (R7) to GND. (This generates a min load current of 10 $\mu$ A.)                     | Inserted       |
| LK4C   | Connects –10VOUT (Pin 17) to patchwork area.                                                                                           | Inserted       |
| LK5A   | Connects +15VOUT (Pin 10) to 150 k $\Omega$ resistor (R4) to GND. (This generates a maximum load current of 100 $\mu$ A.)              | Inserted       |
| LK5B   | Connects +15VOUT (Pin 10) to 1.5 M $\Omega$ resistor (R5) to GND. (This generates a minimum load current of 10 $\mu$ A.)               | Inserted       |
| LK5C   | Connects +15VOUT (Pin 10) to patchwork area.                                                                                           | Inserted       |
| LK6A   | Connects ADM8832 regulated +5VOUT (Pin 4) to +5VIN (Pin 5). (Input to the +15 V and –10 V charge pump stage.)                          | Inserted       |
| LK6B   | Connects externally regulated 5 V output to +5VIN (Pin 5). (Input to the +15 V and –10 V charge pump stage.)                           | Removed        |
| LK7A   | Connects V <sub>CC</sub> to LDO_ON/OFF (Pin 6).                                                                                        | Inserted       |
| LK7B   | Connects LDO_ON/OFF (Pin 6) to GND.                                                                                                    | Removed        |
| LK8A   | Connects V <sub>CC</sub> to $\overline{\text{SHDN}}$ (Pin 7).                                                                          | Inserted       |
| LK8B   | Connects $\overline{\text{SHDN}}$ (Pin 7) to GND.                                                                                      | Removed        |
| LK9A   | Connects V <sub>CC</sub> to SCAN/BLANK (Pin 8).                                                                                        | Inserted       |
| LK9B   | Connects SCAN/BLANK (Pin 8) to GND.                                                                                                    | Removed        |

## SETTING UP THE ADM8832 EVALUATION BOARD

### Scanning Mode

To set up the ADM8832 evaluation board in scanning mode, use the following steps:

1. Connect the scanning mode load resistors.
2. +5VOUT—Connect R1 (insert LK1A, remove LK1C/LK1D)
3. +15VOUT—Connect R4 (insert LK5A )
4. –10VOUT—Connect R6 (insert LK4A )  
Note that all other load resistors should be disconnected by removing their links (see Table 3).
5. Connect VOUT to the ADM8832 LDO (insert LK2A, remove LK2B).
6. Use 3.3 V logic levels for logic inputs.
7. Connect the following jumpers:  
SHDN—Insert LK8A, remove LK8B  
LDO\_ON/OFF—Insert LK7A, remove LK7B  
SCAN/BLANK—Insert LK9A, remove LK9B
8. CLKIN—Connect the SMB cable to SK1.  
Note that an external clock is not required to be applied to CLKIN (Pin 9) in this mode.
9. Apply a 3 V supply to J1.

### Blanking Mode

To set up the ADM8832 evaluation board in blanking mode, use the following steps:

1. Connect the blanking mode load resistors.
2. +5VOUT—Connect R3 (insert LK1C, remove LK3A/LK3B)
3. +15VOUT—Connect R5 (insert LK5B)
4. –10VOUT—Connect R7 (insert LK4B)  
Note that all other load resistors should be disconnected by removing their links (see Table 3).
5. Connect VOUT to the ADM8832 LDO (insert LK2A, remove LK2B).
6. Use 3.3 V logic levels for logic inputs.
7. Connect the following jumpers:  
SHDN—Insert LK8A, remove LK8B  
LDO\_ON/OFF—Insert LK7A, remove LK7B  
SCAN/BLANK—Insert LK9B, remove LK9A (The signal must be low for blanking mode.)
8. CLKIN—Connect the SMB cable to SK1.  
Note that an external clock must be applied to CLKIN (Pin 9) in this mode. The frequency of this clock is nominally 1 kHz (refer to the ADM8832 data sheet for more details).
9. Apply a 3 V supply to J1.



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# EVAL-ADM8832

## ORDERING INFORMATION

### BILL OF MATERIALS

Table 4.

| Qty | Reference Designator | Description                             | Manufacturer | Part Number      |
|-----|----------------------|-----------------------------------------|--------------|------------------|
| 1   | U1                   | 20-lead LFCSP socket (ADM8832 inside)   | Loranger     | 03714-201-6217   |
| 2   | J1, J2               | Power connector, 5 mm pitch             | Weidmuller   | 1716120000       |
| 1   | SK1                  | SMB connector                           | Emerson      | SMB 131-3701-266 |
| 2   | T1 to T2,            | Test point                              | Vero         | 20-313137        |
| 7   | T4 to T10            | Test point                              | Vero         | 20-313137        |
| 6   | C2 to C4, C8 to C9   | Capacitor, 1 $\mu$ F, 50 V, 1206, X7R   | TDK          | C3216X7R1H105M   |
| 5   | C1, C5 to C7         | Capacitor, 2.2 $\mu$ F, 25 V, 1206, X7R | TDK          | C3216X5R1E225K   |
| 1   | R1                   | Resistor, 620 $\Omega$ , 0805 1%        | Yageo        | RC0805FR-07620RL |
| 1   | R2                   | Resistor, 1 k $\Omega$ , 0805 1%        | Yageo        | RC0805FR-071KL   |
| 1   | R3                   | Resistor, 24.9 k $\Omega$ , 0805 1%     | Yageo        | RC0805FR-0725KL  |
| 1   | R4                   | Resistor, 150 k $\Omega$ , 0805 1%      | Yageo        | RC0805FR-07150L  |
| 1   | R5                   | Resistor, 1.5 M $\Omega$ , 0805 1%      | Yageo        | RC0805FR-071M5L  |
| 1   | R6                   | Resistor, 100 k $\Omega$ , 0805 1%      | Yageo        | RC0805FR-07100KL |
| 1   | R7                   | Resistor, 1 M $\Omega$ , 0805 1%        | Yageo        | RC0805FR-071ML   |

### ORDERING GUIDE

| Model                      | Description      |
|----------------------------|------------------|
| ADM8832-EVALZ <sup>1</sup> | Evaluation Board |

<sup>1</sup> Z = RoHS Compliant Part.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## **NOTES**

## NOTES