ZL70101 Medical Implantable RF Transceiver

Features

- 402–405 MHz (10 MICS channels) and 433–434 MHz (2 ISM channels)
- High Data Rate (800/400/200 kbit/s raw data rate)
- High Performance MAC with Automatic Error Handling and Flow Control, Typically < 1.5×10^{-10} BER
- Very Few External Components (3 pieces + antenna matching)
- Extremely Low Power Consumption (5 mA, continuous TX/RX, 1 mA low power mode)
- Ultra Low Power Wakeup Circuit (250 nA)
- Standards compatible (MICS[1], FCC, IEC)

Applications

- Implantable Devices, e.g., Pacemakers, ICDs, Neurostimulators, Implantable Insulin Pumps, Bladder Control Devices, Implantable Physiological Monitors
- Body Area Network, Short Range Device Applications Using the 433 MHz ISM Band

Description

The ZL70101 is a high performance half duplex RF communications link for medical implantable applications.

The system is very flexible and supports several low power wakeup options. Extremely low power is achievable using the 2.45 GHz ISM Band Wakeup-receiver option. The high level of integration includes a Media Access Controller, providing complete control of the device along with coding and decoding of RF messages. A standard SPI interface provides for easy access by the application.

Ordering Information

ZL70101LDG1A	48 Pin QFN[2], for Base Stations Only (trays, bake, and drypack)
ZL70101UBJ	Die, Implantable Grade (trays and drypack)
ZL70101LDG1	48 Pin QFN[2], for Evaluation Only (not available in volume)

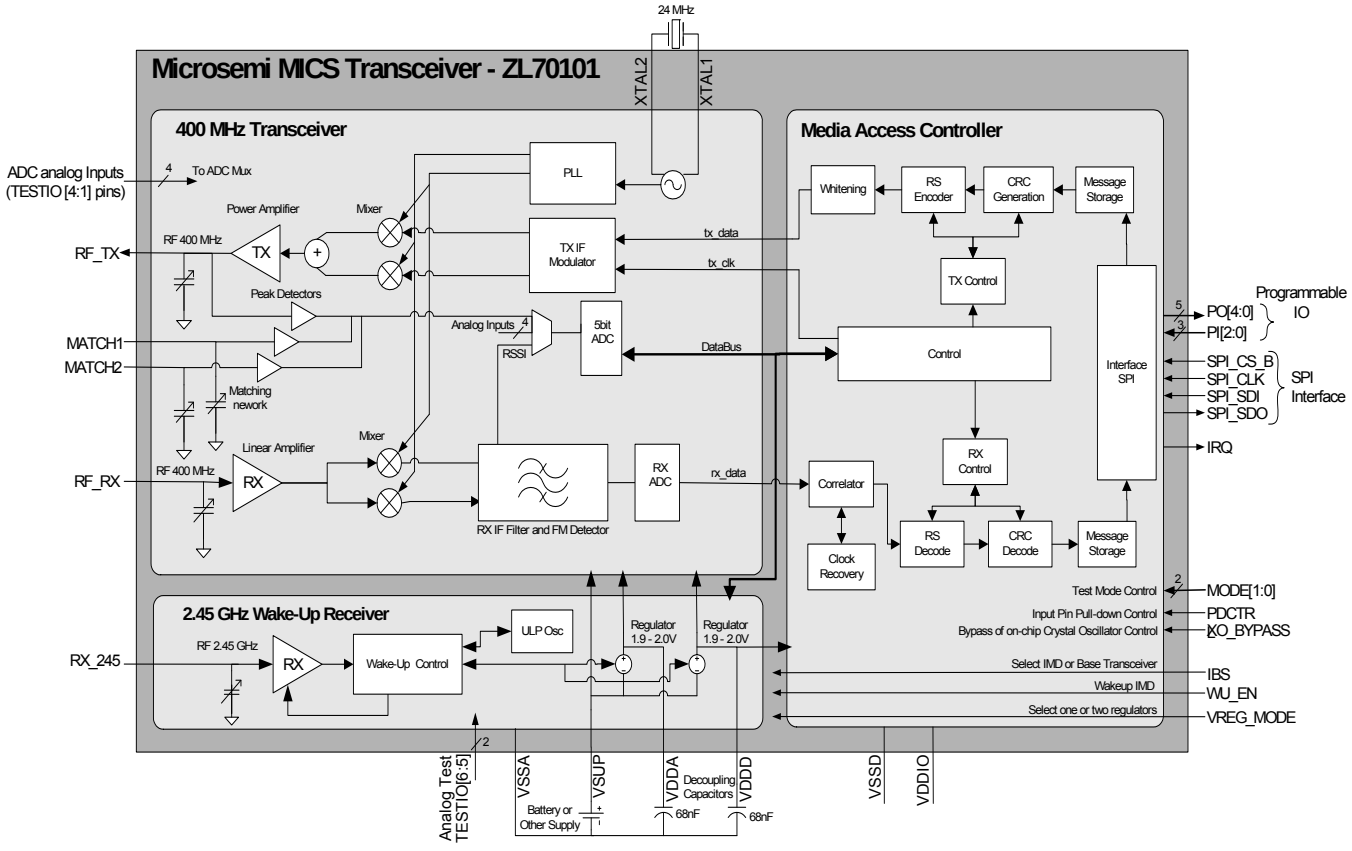

Figure 1 • **ZL70101 Block Diagram**

1 MICS is a subset of MedRadio,
2 Pb free matte tin. Not for implantable use.

QFN Package Diagram

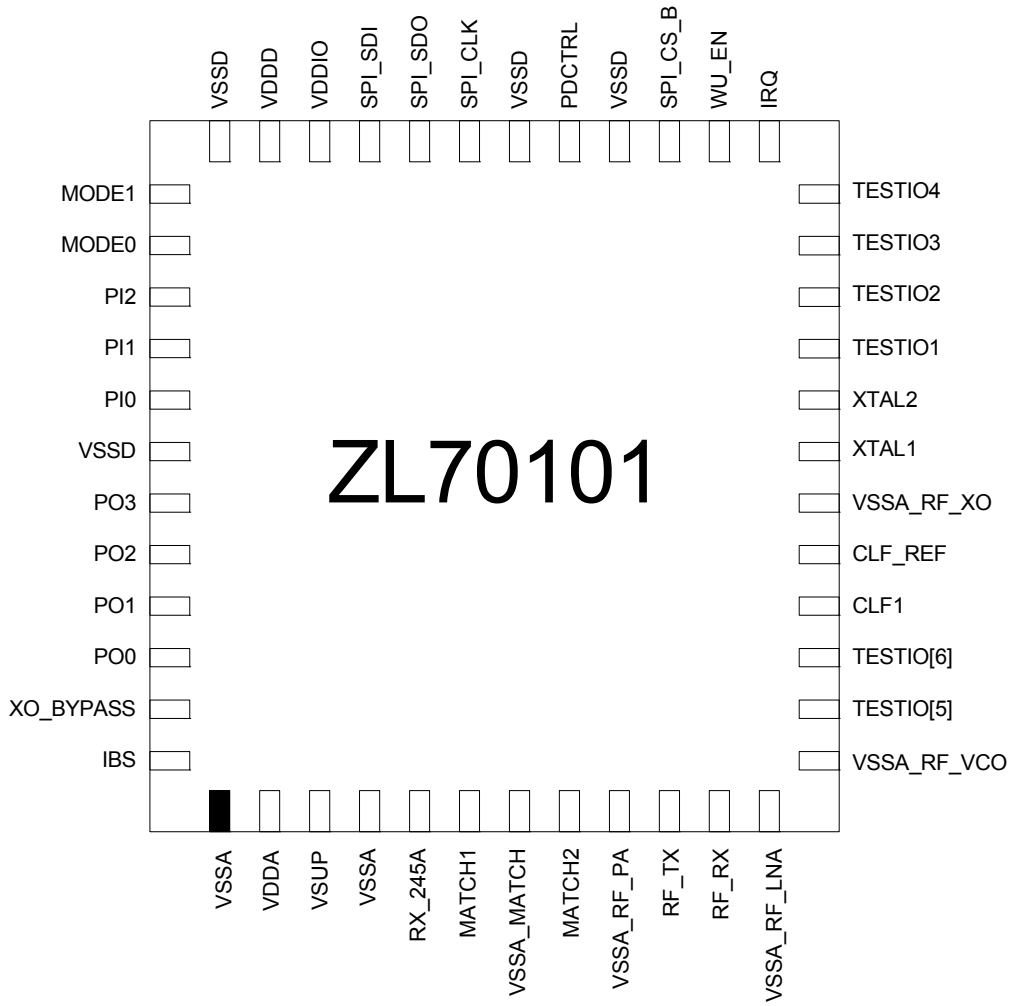

Figure 2 • **ZL70101 QFN Package Diagram, Top View**

Pin Descriptions

Bare Die Pad#	Package Pin #	Name	Description	I/O	ESD Level (V_{HBM})	Output Max Load
1	GND Post + 1	VSSA / VSSD	Analog / Digital Ground	power	1 K	–
2	2	VDDA2 [1]	Analog On chip Regulated Power (1.9–2 V)	power	1 K	–
3	3	VSUP	Unregulated supply (2.1–3.5 V) for PA, wake up and voltage regulator input	power	1 K	–
	GND Post + 4	VSSA / VSSD	Analog / Digital Ground	power	1 K	–
4	5	RX_245A	Receive 2.45 GHz wake message	analog input	1 K	–
5	GND Post	VSSA_WAKE_LNA	RF Ground for Wake-Up LNA	power	1 K	–
6	6	MATCH1	Tuning Capacitor 1	analog I/O	1 K	–
7	7	VSSA_MATCH	RF ground for MATCH1 and MATCH2 capacitors	power	1 K	–
8	8	MATCH2	Tuning Capacitor 2	analog I/O	1 K	–
9	GND Post	VSSA_GEN1	General Analog Ground	power	1 K	–
10	10	RF_TX	Transmit 400 MHz output to matching network	analog output	1 K	–
11	GND Post + 9	VSSA_RF_PA	RF Ground for Power Amplifier (PA)	power	1 K	–
12	11	RF_RX	Receive 400 MHz RF input from matching network	analog input	1 K	–
13	GND Post + 12	VSSA_RF_LNA	RF Ground for LNA	power	1 K	–
14	GND Post	VSSA_GEN2	General Analog Ground	power	1 K	–
15	GND Post	NC	Spare pad not used	analog input	1 K	–
16	GND Post	VSSD	Digital Ground	power	1 K	–
17	GND Post	VSSD	Digital Ground	power	1 K	–
18	GND Post + 13	VSSA_RF_VCO	RF Ground for RF VCO	power	1 K	–

Notes:

1. *The two VDDA pads are hardwired together on chip so only one of these pads is required to be bonded. For bare die on a hybrid, it is recommended to bond only pad 1 (especially if pads 52–70 are unbonded and PDCTRL (pad 40) = 1).*
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3. *The SPI_SDO is tristated in sleep mode to ensure that other devices may use the SPI bus*
4. *The MODE pins are described in the "Selection of Modes (mode pin function)" section on page 1-4. The programmable input and output pads are described in the "Application Interface" section on page 3-1.*
5. *These output pads are defined low in sleep mode. (Some may be interrupts and it is preferred that they are defined rather than floating).*
6. *The maximum output frequency for PO0–PO4 is 5MHz for the full range of VDDIO (1.5V to VSUP). The PO3 and PO4 pads may be programmed to output the crystal frequency which is 24 MHz. This is only possible with VDDIO > 3V and the duty cycle variation is then 0.3–0.7.*
7. *The user must ensure that all inputs are defined and not floating at all times (even when the system is asleep), otherwise unnecessary power consumption will occur.*

Pin Descriptions (continued)

Bare Die Pad#	Package Pin #	Name	Description	I/O	ESD Level (V_{HBM})	Output Max Load
19	14	TESTIO[5]	Analog test bus pin 5, used for connection to internal nodes selected by test register	analog I/O	1 K	–
20	15	TESTIO[6]	Analog test bus pin 6, used for connection to internal nodes selected by test register	analog I/O	1 K	–
21	16	CLF1	Optional Loop Filter Capacitor 1	analog I/O	1 K	–
22	NC	CLF2	Optional Loop Filter Capacitor 2	analog I/O	1 K	–
23	17	CLF_REF	Optional Loop Filter Reference	analog I/O	1 K	–
24	GND Post	VSSA_GEN3	General Analog Ground	power	1 K	–
25	GND Post	VSSA_GEN4	General Analog Ground	power	1 K	–
26	GND Post + 18	VSSA_RF_XO	RF Ground for Crystal Oscillator (XO)	power	1 K	–
27	19	XTAL1	Crystal Oscillator in	analog input	1 K	–
28	20	XTAL2	Crystal Oscillator out	analog output	1 K	–
29	21	TESTIO[1]	Analog test bus pin 1, used for connection to internal nodes selected by test register	analog I/O	1 K	–
30	22	TESTIO[2]	Analog test bus pin 2, used for connection to internal nodes selected by test register	analog I/O	1 K	–
31	23	TESTIO[3]	Analog test bus pin 3, used for connection to internal nodes selected by test register	analog I/O	1 K	–
32	24	TESTIO[4]	Analog test bus pin 4, used for connection to internal nodes selected by test register	analog I/O	1 K	–
33	GND Post	VSSD	Digital Ground	power	1 K	–

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Pin Descriptions (continued)

Bare Die Pad#	Package Pin #	Name	Description	I/O	ESD Level (V_{HBM})	Output Max Load
34	GND Post	VSSD	Digital Ground	power	1 K	–
35	25	IRQ	Interrupt request	digital output	1 K	10 pF/ 5 MHz
36	GND Post	VSSD8	Digital Ground	power	1 K	–
37	26	WU_EN	Wake-Up enable signal used for strobing the wake-up LNA.	digital input	1 K	–
38	27	SPI_CS_B	SPI Chip Select (active low)	digital input	1 K	–
39	GND Post + 28	VSSD3	Digital Ground	power	1 K	–
40	29	PDCTRL [2]	Pull-down control (for inputs on top side of chip (see note 2). If PDCTRL = 1 then these inputs are pulled low and do not need to be bonded out)	digital Input	1 K	–
41	GND Post + 30	VSSD2	Digital Ground	power	1 K	–
42	31	SPI_CLK	SPI Serial Clock	digital input	1 K	–
43	32	SPI_SDO	SPI Serial Data Out	digital output	1 K	10 pF/ 5 MHz [3]
44	GND Post	VSSD7	Digital Ground	power	1 K	–
45	NC	PO4	Programmable output 4 (See MAC for description on programmable I/O)	digital output [4]	1 K	10 pF/ 30 MHz [5,6]
46	33	SPI_SDI	SPI serial Data In	digital input	1 K	–
47	34	VDDIO	Digital I/O supply (acceptable range: 1.5–VSUP)	power	1 K	–
48	GND Post	VSSD1	Digital Ground	power	1 K	–
49	GND Post	VREG_MODE	1 or 2 regulator selection pin (1 regulator = 1, 2 regulators = 0)	digital input	1 K	–

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Pin Descriptions (continued)

Bare Die Pad#	Package Pin #	Name	Description	I/O	ESD Level (V_{HBM})	Output Max Load
50	35	VDDD	Digital On chip Regulated Power (1.9–2 V) (This regulator can be disabled with pin VREG_MODE)	power	1 K	–
51	GND Post + 36	VSSD	Digital Ground	power	1 K	–
52	GND Post	VSSD	Digital Ground	power	1 K	–
53	37	MODE1	Mode selection pin (used with MODE0 to configure certain test and other states)	digital input [2,4]	1 K	–
54	38	MODE0	Mode selection pin (used with MODE1 to configure certain test and other states)	digital input [2,4]	1 K	–
55	GND Post	VSSD6	Digital Ground	power	1 K	–
56	39	PI2	Programmable input 2 (See MAC for description on programmable I/O)	digital input [2,4]	1 K	–
57	40	PI1	Programmable input 1 (See MAC for description on programmable I/O)	digital input [2,4]	1 K	–
58	41	PI0	Programmable input 0 (See MAC for description on programmable I/O)	digital input [2,4]	1 K	–
59	GND Post + 42	VSSD4	Digital Ground	power	1 K	–
60	43	PO3	Programmable output 3 (See MAC for description on programmable I/O)	digital output [4]	1 K	10 pF/ 30 MHz [5,6]
61	44	PO2	Programmable output 2 (See MAC for description on programmable I/O)	digital output [4]	1 K	10 pF/ 5 MHz [5,6]
62	GND Post	VSSD10	Digital Ground	power	1 K	–
63	45	PO1	Programmable output 1 (See MAC for description on programmable I/O)	digital output [4]	1 K	10 pF/ 5 MHz [5,6]
64	46	PO0	Programmable output 0 (See MAC for description on programmable I/O)	digital output	1 K	10 pF/ 5 MHz [5,6]

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Pin Descriptions (continued)

Bare Die Pad#	Package Pin #	Name	Description	I/O	ESD Level (V_{HBM})	Output Max Load
65	GND Post	VSSD5	Digital Ground	power	1 K	–
66	47	XO_BYPASS	Bypass on-chip crystal oscillator circuit and use external oscillator connected to XTAL1	digital input [2]	1 K	–
67	48	IBS	Implant - Base Selection (Implant = 0, Base station = 1)	digital input [2]	1 K	–
68	GND Post	VSSD9	Digital Ground	power	1 K	–
69	NC	VDDA1 [1]	Analog On chip Regulated Power (1.9–2 V)	power	1 K	–
70	GND Post	VSSD	Digital Ground	power	1 K	–

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Table of Contents

List of Figures

List of Tables

1 – ZL70101 Functional Description

General

The ZL70101 is an ultra low power, high bandwidth RF link for medical implantable applications. It operates in the MICS (Medical Implantable Communication Service) at 402–405 MHz. It uses a Reed-Solomon coding scheme together with CRC error detection to achieve an extremely reliable link. For standard data-blocks defined in "400 MHz Packet Definition" section on page 1-12 a maximum BER (Bit Error Rate) of less than 1.5×10^{-10} is provided assuming a raw radio channel quality of 10^{-3} BER. An even higher quality of 2×10^{-14} BER is available using housekeeping messages as described in "Housekeeping Messages" section on page 3-3.

Basic Operation and Modes

The ZL70101 transceiver is intended for operation in both an implant and base station. These systems have different requirements especially with regard to power consumption. Therefore, the ZL70101 transceiver has defined two fundamental startup modes of operation:

- Implantable Medical Device (IMD) Mode
- Base Mode

When configured as an IMD, the transceiver is usually asleep and in a very low current state. The IMD may be woken up to initiate communications by either receipt of a specially coded 2.45 GHz wakeup message or directly by the IMD processor via the WU_EN pin. These two methods of starting a communication session with an IMD are summarized below.

Startup Method Using 2.45 GHz Sent from Base

Figure 1-1 below indicates the steps in setting up communication between a Base and an IMD woken up by using the ultra-low power 2.45 GHz wakeup method. Details of this wakeup method are available in the design manual.

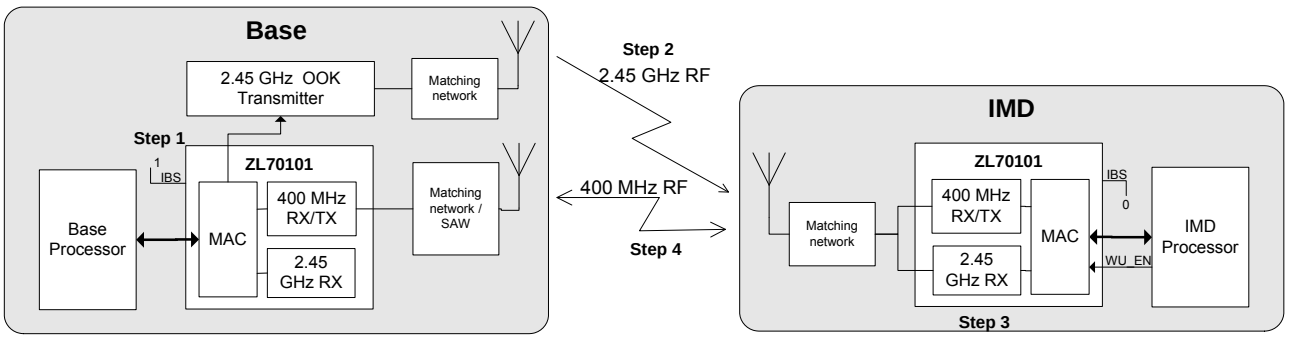


Figure 1-1 • **Startup Method Using 2.45 GHz**

Steps:

1. STARTUP BASE: Set pin IBS=1 and power up Base. MAC starts and waits in idle state. Base application performs clear channel assessment as described in ZL70101 design manual. Base application sets up important link parameters including registers for modulation mode, channel to use, IMD transceiver ID, company ID as described in "2.45 GHz Wakeup Receiver" section on page 1-8 as well as in the design manual.
2. SEND 2.45 GHz WAKEUP MESSAGE: The Base application initiates wakeup by writing to a communication control register in the Base ZL70101. This will simultaneously provide the On-Off Keyed (OOK) pattern for the 2.45 GHz transmitter and start the 400 MHz receiver to receive wakeup responses from the IMD.
3. IMD 2.45 GHz RECEIVES MESSAGE: The IMD 2.45 GHz receiver is usually in sleep mode. The receiver may be periodically powered up to look for the 2.45 GHz wakeup message. The interval between power up strobes

is user defined. The user may select one or both of the following two strobe mechanisms. (a) Program a low power oscillator available in the ZL70101 which will generate the strobe. (b) Supply the strobe using the WU_EN pin.

4. IMD SENDS 400 MHz WAKEUP RESPONSES: The IMD will begin transmitting 400 MHz wakeup responses to the Base and the Base will receive these responses. The interval between response packets is randomized to minimize collisions between multiple IMDs and the Base. The Base may then begin a full MICS communication session with the desired IMD by writing to a communication control register in the Base ZL70101.

Startup Method Using IMD Pin Control

Figure 1-2 below indicates the steps in setting up communication between a Base and an IMD woken up by using the pin control in the IMD. This method would be used for the following wakeup schemes:

- IMD woken up to sniff 400 MHz link. The ZL70101 supports such a mode of operation although the 2.45 GHz wakeup system described in the previous section has a much lower power consumption.
- IMD woken to send an emergency message in which case no clear channel assessment by the Base is required.
- IMD woken up by a low frequency inductive link (as typically used in pacemakers/ICDs) or some alternative mechanism.

In all these cases, the IMD transceiver is started by asserting WU_EN high for greater than 1.5 ms as described in the following step description.

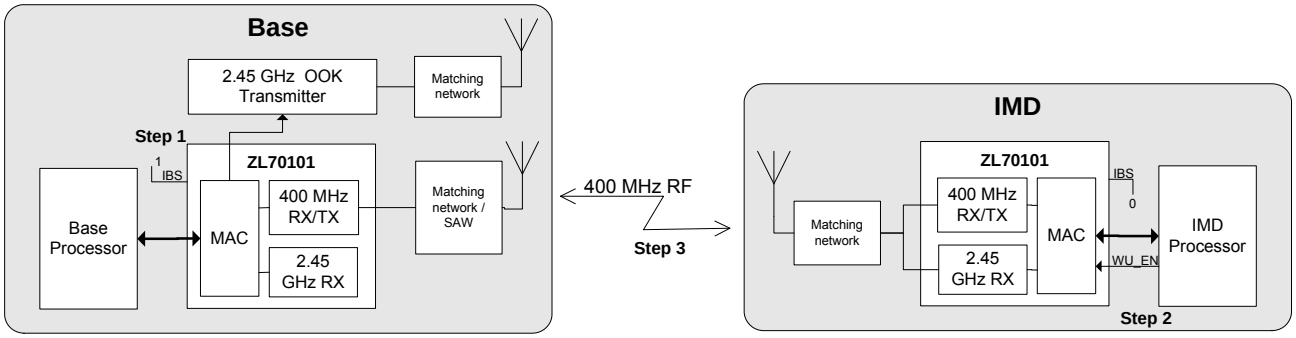


Figure 1-2 • **Startup Method Using IMD Pin Control**

Steps:

1. STARTUP BASE: Set pin IBS=1 and power up Base. MAC starts and waits in the idle state. Base application is set to monitor a predefined channel (for emergency command case) or a channel determined by a previously performed clear channel assessment as described in the ZL70101 design manual.
2. IMD PROCESSOR STARTS IMD TRANSCEIVER: IMD application sets the WU_EN pin high for greater than 1.5 ms and then low again. The IMD transceiver will wakeup and wait in the idle state. An important flag in the IMD transceiver called the *Idle* flag is set to 1 (Idle). The Idle flag defines the operation of the transceiver after the MAC has woken up. The flag has two states (1 = Idle, 0 = Send_Response).

IMD SENDS 400 MHz WAKEUP NOTIFICATION: The IMD application should then setup the transceiver to use the desired modulation mode and channel. The IMD application should then change the *Idle* flag to 0, (Send_Response) by writing to the appropriate control register in the IMD ZL70101. The IMD will begin transmitting 400 MHz wakeup responses to the Base and the Base will receive these responses. The Base may then begin a full MICS communication session with the desired IMD by writing to a communication control register in the Base ZL70101.Details of the programming steps necessary for these steps and other operations is provided in the ZL70101 design manual.

Configuration Options and Power States

Table 1-1 summarizes the required control signals to configure a device as an IMD or Base.

Table 1-1 • **Methods of Starting as Base or IMD**

Startup Methods			Required Control Signals			
Mode	**Method**	**Startup action**	**IBS Pin**	**WU_EN Pin**	**WU_EN Internal Strobe Osc**	**2.45 GHz Wake Received**
BASE	Pin control – IBS	Starts MAC and waits in Idle state	1	X	X	X
IMD	Pin control – Extended WU_EN	Starts MAC and waits in Idle state	0	1 (for > 1.5 ms pulse)	X	X
IMD	WU_EN pin strobe and receive 2.45 GHz	Starts MAC and sends wakeup responses	0	1 (for < 0.4 ms)	X	1
IMD	WU internal strobe oscillator and receive 2.45 GHz	Starts MAC and sends wakeup responses	0	0 or 1 (for < 0.4 ms)	1	1
IMD	Asleep and periodically sniffing wakeup	No MAC startup – No wakeup received	0	sleep (0) or sniffing (1 for < 0.4 ms)	sleep (0) or sniffing (1 for < 0.4 ms)	0

In addition, for both the IMD and Base modes there exist configuration options (or *operational modes*) that are setup using registers and pins (for some wafer test options). Four broad categories of operational modes exist as shown below. Each of these configurations applies to both the IMD and Base modes. The reset value of registers is such that the normal operation mode is the default mode of operation for the device. These modes are described in detail in the design manual.

Table 1-2 • **Summary of Operational Modes**

Operational Mode	Description
Normal (Default)	All ZL70101 transceivers are initially powered up in the normal operation mode. The normal operation mode is fully described in the design manual where a complete behavioral flow-chart is provided along with a description of the link operation.
Bypass and Loopback Operation	Includes the following modes • Full MAC bypass • Selected TX/RX datapath block bypass • RF Bypass mode • MAC loopback mode The application of these modes is described in "Programmable I/O and Bypass Modes" section on page 3-4.
Calibration	Trimming and tuning of certain on-chip circuitry is necessary before the ZL70101 transceiver is ready for use. Most calibrations are performed automatically and without user intervention when the transceiver starts up. A select few should be performed in the production environment. From calibration mode, the ZL70101 transceiver automatically returns to normal operation mode after the calibration is performed.
Test	Not used by the user. For chip production testing.

Furthermore, the device has various power states (or *power modes*). Whilst starting up and performing operations in each of the configurations, the device will step through different power modes that define which blocks are operational

at any one time. Power states are necessary for optimal control and power saving. Table 1-3 below summarizes the power states.

The communication protocol features a "power-save timer" which allows the transceiver to enter the wake-mode state for a user defined time (0–27 sec) following the transmission of a packet. This is a very useful power saving feature in applications where the IMD does not immediately have data to send and the effective required data rate is lower than the high data rate provided by the ZL70101.

Table 1-3 • **Summary of Power States**

Power Mode	Maximum Current	Description
Sleep Mode, external strobe	100 nA	The device is in low power mode in between strobe pulses on WU_EN pin, internal strobe oscillator is disabled. See Figure 1-5 on page 1-9.
Sleep Mode, internal strobe	500 nA	The device is in low power mode in between strobe signals generated by internal strobe oscillator. See Figure 1-5 on page 1-9.
Listen Mode	715 µA	Listens (sniffs) for 2.45 GHz wakeup signal. In this mode the wakeup LNA and detector circuit are enabled by the WU_EN pin or the internal wakeup strobe oscillator (if enabled). See Figure 1-5 on page 1-9.
Wake Mode	0.9 mA	The device has been woken up and has started the voltage regulators, crystal oscillator and MAC. SPI interface is now operational.
TX Mode	5.0 mA	The device is transmitting on 400 MHz.
RX Mode	5.0 mA	The device is receiving on 400 MHz.

Selection of Modes (register programming)

In general, the configuration of the ZL70101 transceiver into various modes and states requires programming of registers. Programming of registers may be performed using two different interfaces that are collectively referred to as the "Application Interface":

1. Serial Interface
   This is a standard slave Serial Peripheral Interface (SPI) complemented by a programmable IRQ and programmable I/O pins.
2. RF Interface – Housekeeping (HK) Messages
   The ZL70101 transceiver may access registers in a remote ZL70101 transceiver by using housekeeping messages. These are messages sent in the header of the packet. Housekeeping messages allow communication of high priority data and programming of remote device registers.

Details of these interfaces are contained in the "Application Interface" section on page 3-1 of this document. Unless specified otherwise, internal registers are controllable from either of these 2 interfacing methods.

Note that the ZL70101 transceiver, when asleep, resets all registers except for some VSUP supplied registers within the wakeup circuitry that contain important trimming and tuning data and control information for the wakeup. The registers that are backed-up by VSUP are denoted by CRC = Yes in the ZL70101 memory map.

Selection of Modes (mode pin function)

There are particular chip configurations that should be directly configurable using I/O pins as opposed to register programming. These configurations include the implant / base station mode and digital test modes. The two mode pins (MODE0 and MODE1) are used for these select situations that are not suitable for register programming. The function of these pins is described in the design manual.

400 MHz Transceiver Subsystem

The transceiver uses a low-intermediate frequency super-heterodyne architecture with image reject mixers. The low-IF minimizes filter and modulator power consumption without the flicker noise issues associated with zero-IF architectures. An FSK modulation scheme reduces amplifier linearity requirements thereby reducing power consumption. In addition, FSK offers spectral efficiency by producing a high data rate given the MICS band spectrum mask requirements. Image rejection improves the adjacent channel rejection of the system.

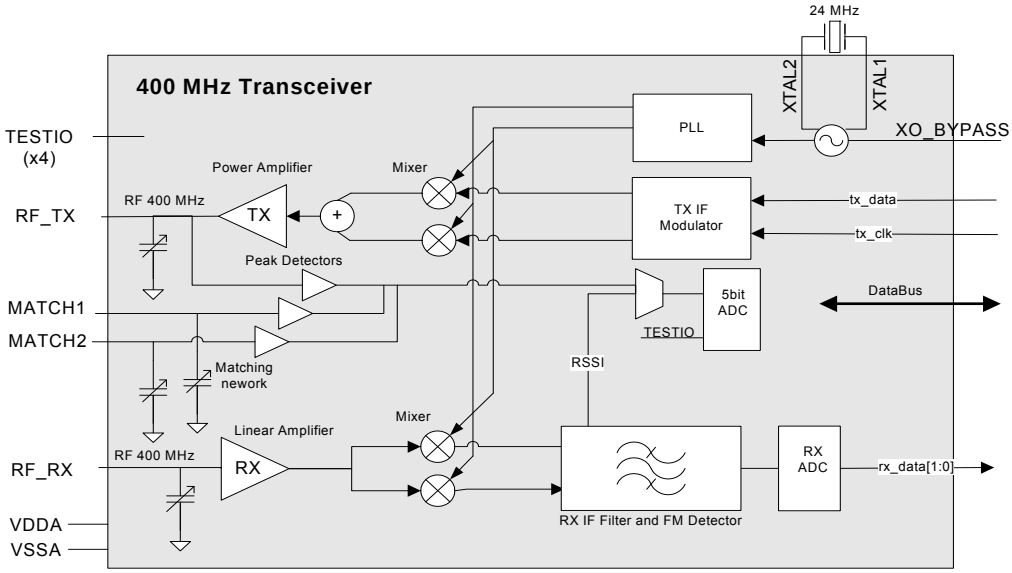


Figure 1-3 • **400 MHz Transceiver Subsystem**

For minimum overall power consumption, defined in terms of Joules/bit, it is recommended that IMD transceivers should use the highest possible data rate that satisfies the application receiver sensitivity requirements. Systems that require low data rates (even in the low kHz range) should operate at the highest data rate possible and exploit duty-cycling of the power states to reduce the average current consumption. Sending data in short bursts not only offers the benefits of conserving power, the time window allowed for interference is reduced by a short transmission time, and, in systems with high battery impedance, the decoupling requirements are more forgiving.

The ZL70101 allows the user to select from a wide range of data rates (200/400/800 kbps) with varying receiver sensitivity. To facilitate this flexibility, the system uses either 2FSK or 4FSK modulation with 200 or 400 kSymbols/s and varying frequency deviations. Table 1-4 below summarizes the allowable modulation modes, respective data rates and corresponding receiver sensitivity. Note also, that the user may choose even lower rates by bypassing the MAC as described later in "MAC Bypass Mode" section on page 3-5 and in the design manual.

Table 1-4 • **Options for Modulation Modes, Data Rate and Receiver Sensitivity**
Please see the Design Manual for further information.

Modulation Mode	Maximum Raw Radio Data Rate (kbps)	Maximum Effective Data Rate (kbps)	Typical Receiver Sensitivity R_S=500, R_L=4500 and R_{eff} = 1620 Ohms	
4FSK	800	528	−84 dBm	80 μV_{rms}
2FSK high rate	400	267	−94 dBm	25 μV_{rms}
2FSK high sensitivity	200	134	−99 dBm	14 μV_{rms}

Transmitter Section

The ZL70101 transmitter consists of an IF modulator, I and Q mixer and power amplifier.

The IF modulator converts a one (2FSK) or two bit (4FSK) asynchronous digital input data stream to a 450 kHz FSK modulated I and Q signal. The data stream may come from the MAC in normal operation mode or may be applied to the programmable input pins in the MAC bypass mode. The IF center frequency of 450 kHz is automatically calibrated using a frequency locked loop (FLL) each time the transceiver is woken up.

An up-converting mixer transforms the IF to RF. Note that the local oscillator frequency is the same for both transmit and receive mode, facilitating a minimum deadtime between receiving and transmitting packets. Both low and high side injection is used to always keep the image in the MICS band to relax the demands on phase and amplitude matching of the I and Q signals. When the RF is in the lower half of the MICS band, the LO frequency is higher than the transmitted radio frequency. When the RF is in the upper half of the MICS band, the LO frequency is lower than the transmitted radio frequency.

The output power of the TX power amplifier is register programmable from approximately −1 dBm to −18 dBm (into a 500 Ohm load, dependent on supply voltage). An antenna matching capacitor bank is provided to fine tune the matching network for maximum delivered output power for a given power setting. The antenna tuning is an automatic calibration which uses a peak-detector coupled to an ADC along with a state-machine for calibration control.

Receiver Section

The ZL70101 400 MHz receiver side amplifies the MICS band signal and down-converts from the carrier frequency to the intermediate frequency (IF) using an IQ image reject mixer. The LNA gain is programmable from 9 to 35 dB in approximately 3 dB steps. Higher gain settings are recommended for IMD transceivers whilst the lower gain settings may be applicable to Base transceivers that choose to use an external LNA. Programmability of LNA and mixer bias currents provides further flexibility in optimizing for desired linearity (IIP3), power consumption and noise figure.

An image rejecting I/Q poly-phase IF filter is used to suppress interference at the image frequency and adjacent channels and limit the noise bandwidth. The poly-phase filter is followed by limiters and an Received Signal Strength Indicator (RSSI) block. The RSSI measurement is converted by a 5 bit ADC and may be read by the SPI interface. For performing the MICS clear-channel assessment, the user has the option of porting out the IF signal via the TESTIO pins. The RSSI measurement may then use off-chip components, available in the Base, to perform a measurement with higher resolution than the on-chip RSSI.

The RSSI block on ZL70101 can be trimmed to obtain an optimum absolute accuracy. This is done once in production by applying a known external signal on RX and calibrating the RSSI offset with the trim bits.

An FM detector converts frequency deviation to voltage levels. The resulting baseband signal is subsequently low pass filtered to remove the 4th harmonic of the IF and then digitized by a 2-bit quantizer. The resulting data stream is provided to the MAC for correlation and clock recovery. Each packet begins with a (1 to 4) byte training and 5 byte correlation sequence. The value of the training and correlation word is programmable as well as the number of training bytes. A DC removal circuit prior to the quantizer adjusts the DC level during the training phase. The purpose of this adjustment is to remove DC offset due to reference frequency differences between the Base and IMD transceivers. After the 40 bit correlation word is matched the DC level is fixed for the remainder of the packet.

An matching capacitor bank is provided on RX to fine tune the matching network. This function is intended to be used when RX and TX are separated in the matching network. This tuning is done once in production with an external signal and using the on-chip RSSI.

Two additional capacitor banks (on MATCH1 and MATCH2) are provided to be used for the tuning matching network. See the Design Manual for further details.

Frequency Synthesizer

The Frequency Synthesizer is a PLL structure with a RF Voltage Controlled Oscillator (VCO) running at four times the LO frequency. The I/Q Local Oscillator (LO) signals are derived from the VCO signal and distributed to the receive and transmit Front-End. The VCO is divided down and locked to the reference frequency which is supplied by the crystal oscillator running at 24 MHz with an external crystal. The synthesizer uses both high and low side injection to ensure that the image frequency is always within the MICS band The channel number is programmable from 1–10 for the 402–405 MHz MICS band and 11–12 for 433.65 and 434.25 MHz ISM band.

Crystal Oscillator

The 24 MHz crystal oscillator (XO) is responsible for generating the system clock used by both the 400 MHz transceiver and the MAC. A 24 MHz crystal was selected as a compromise between small implant crystal size (decreases slowly with increasing frequency) and oscillator power requirements (<200 µA budgeted). Moreover, this frequency simplifies on-chip clocking since 24/80=300 kHz is exactly the channel spacing and 24/60=400kHz is the symbol rate. The required characteristics of the crystal are discussed in detail in the design manual. Microsemi has worked closely with leading IMD crystal manufacturers to ensure the availability of an implant grade 24 MHz crystal.

The required XO tolerance is determined by the transmitter and receiver frequency alignment requirements. Analysis of the ZL70101 indicates that the total frequency misalignment should be limited to ±75 ppm. The ZL70101 XO has the facility for trimming a ±60 ppm oscillator to within ±10 ppm.

The oscillator may be bypassed by asserting the pin XO_BYPASS. This will enable an external oscillator connected to XTAL1 to provide the 24 MHz frequency. Base stations may then choose to use a very accurate external temperature controlled crystal oscillator (TCXO) to provide engineering margin in the frequency budget and reduce on-chip frequency trimming requirements. When XO_BYPASS is asserted the XO Core is powered down and the signal from XTAL1 is provided directly to internal circuitry.

The 24 MHz clock and a variety of subfrequencies are available on the buffered programmable output pins PO3 and PO4 by register programming. This may be used by implant or base systems that require a clock.

General Purpose ADC

A 5 bit general purpose successive approximation ADC with a conversion time of 2 µsec is provided for the following purposes:

1. Measurement of the peak voltage at the 400 MHz PA output: This measurement is used for tuning the antenna matching network.
2. Measurement of the peak voltage at the MATCH1 capacitor bank. This is used for tuning the antenna matching network.
3. Measurement of the peak voltage at the MATCH2 capacitor bank. This is used for tuning the antenna matching network.
4. Measurement of the internal 400 MHz RSSI signal. The application may find the RSSI measurement useful for automatic gain control or other system optimization methods that require a measurement of received signal strength.
5. Supply voltage input: This is a useful system diagnostic measurement. The voltage on VSUP is divided by a resistive divider and measured using the ADC. The resistor divider is disconnected from the battery voltage when the ADC measurement is not selected or the ADC is disabled. Other ADC inputs do not have a resistor divider.
6. Measurement of inputs from analog TESTIO bus: One of four TESTIO pins, TESTIO[4:1], may be selected for input into the ADC. This provides a useful general purpose ADC function for the application. The ADC may be used to measure application specific physiological signals, or system diagnostic signals.

A programmable multiplexer on the input of the ADC selects between the different measurements.

2.45 GHz Wakeup Receiver

The 2.45 GHz receiver is used for a low power wakeup system. The block diagram is shown below followed by a description of the basic operation.

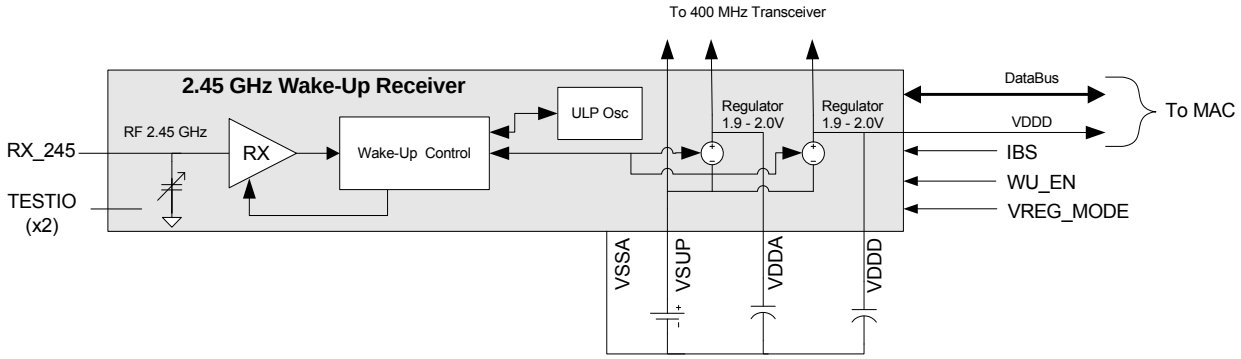


Figure 1-4 • **2.45 GHz Wakeup Receiver Subsystem**

Basic Operation

Most implant applications will use the MICS RF link infrequently due to the overriding need to conserve battery power. In very low power applications, the ZL70101 will spend most of the time asleep in a very low current state. Except for the sending of an emergency command, systems that use the MICS band must first wait for the Base to initiate communications following a clear channel assessment procedure in which the Base determines which channel to use.

Therefore, periodically, the IMD transceiver should listen for a Base that wants to begin communication. This "sniffing" operation should be frequent enough to provide reasonable startup latency, consume a very low current since it will occur regularly, and be immune to noise sources that invoke an erroneous startup.

For a very low power receiver an OOK modulation scheme is recommended since it removes the need for a local oscillator and synthesizer in the receiver. Further simplification, and hence power saving, is gained by using a frequency band for the startup process which is of reasonable power. The 2.45 GHz WLAN band satisfies such a requirement and at 100 mW EIRP (country dependent, can also be 10 mW) is 36 dB higher in power than the MICS band.

The wakeup system uses a novel ultra low power RF receiver, operating in the 2.45 GHz WLAN band, to read OOK transmitted data. The main function is to detect and decode a specific data packet that is transmitted from a Base station and then switch on the supply to the rest of the chip (the MAC block and the RF block, referred to collectively as the *core* in this document).

To reduce the average current consumption of the wakeup subsystem, the wakeup system is strobed by either:

1. An application generated strobe pulse applied to the WU_EN pin to enable the wake up circuitry.
2. An internally generated strobe pulse created using a low power (400 nA) internal 25 kHz oscillator.

In the example calculation supplied in Figure 1-5 on page 1-9, 250 nA (external strobe) or 650 nA (internal strobe) is achieved including 100 nA for leakage current. The actual current will depend significantly on the timing of the strobe. The power supply to both the digital and analog parts in the wakeup is the VSUP voltage (2.1 V–3.5 V).

The external strobe (*wu_en*) and internal oscillator strobe are OR'ed such that either one (or both) may generate a wakeup strobe any time the device is asleep.

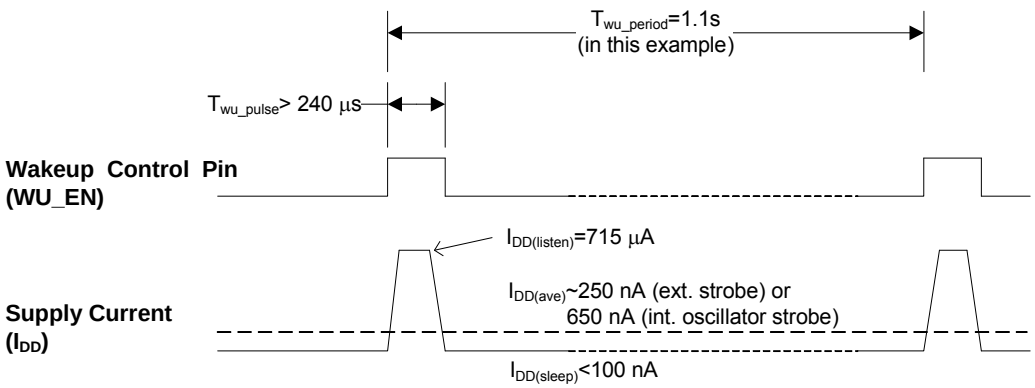


Figure 1-5 • **Strobing of Wakeup System**

The data packet that is sent from the Base to the IMD transceiver is Manchester encoded and OOK modulated. The transmitted data packet is encoded with clock and data information. A simple decoder block is then used to extract the clock information and sample the data using the recovered clock.

If Manchester encoded data is detected during the strobe pulse time, the strobe signal will be maintained internally and the system will search for the start of the pattern indicated by a unique non Manchester encoded pattern of 11110000. After the start is found a complete packet of data is analysed. If at any time during the packet reception the data becomes corrupted, the wakeup controller will terminate reception and power down. Furthermore, if the data stream is lost during reception (and consequently the clock), a watchdog circuit will terminate reception and power down the wakeup receiver.

On successful detection and decoding of a valid packet of data, the wakeup receiver will be turned off and on-chip 2 V voltage regulators will start. Two voltage regulators are used (one for the analog core supply and one for the digital core supply) to separate the digital and analog supplies. The two supplies are available on two pads, VDDA and VDDD. They need two separate external capacitors (both 68 nF), one for VDDA and one for VDDD. It is recommended to use both these regulators.

For low data rate applications in need of low current consumption and low component count there is an option to use only one regulator which leads to a slightly reduced BER. One way to improve BER with one regulator setup is to use external filtering (more external components) on VDDA/VDDD. The digital input pad VREG_MODE defines if both these two regulators are used or if only the analog regulator is used by setting it to 0 (two regulators) or 1 (1 regulator).

After the regulators are fully on, the crystal oscillator will start followed by the MAC. The time allowed for the crystal oscillator to start is programmable which allows the user to achieve faster startup times if crystal specifications permit. On successful core power up (i.e when the 2 V regulators and XO starts up OK and the MAC is running) the MAC will reply to the wakeup subsystem that it is ready and perform a CRC check of the wakeup memory, copy registers to the MAC and perform calibrations. A communication session then occurs at 400 MHz. When this is finished the MAC under user register control will signal to the wakeup system to go back to sleep and power down the core.

As mentioned in "Basic Operation and Modes" section on page 1-1, there are various methods for waking up the transceiver. The wakeup controller, by monitoring pins IBS and WU_EN, controls the selection of the various wakeup methods. Note that if the IBS pin is high, meaning a Base transceiver is selected, then the wakeup controller will maintain the regulated supply turned on throughout operation.

When the battery is connected for the first time, a POR block (wake_por) will reset all digital registers and flip flops in the wakeup subsystem.

2.45 GHz Wakeup Data Packet Definition

The data packet content is shown in Figure 1-6 below. The information is used by the IMD to setup the 400 MHz transceiver for communication on the appropriate channel and modulation mode.

The raw data is Manchester encoded (a 0 is encoded as 01, a 1 is encoded as 10) since such a coding scheme can convey clock information, thus permitting the wakeup receiver to operate without a high frequency clock and therefore save power. The OOK modulation pattern is provided on pin PO0 by appropriately programming the output and writing a 1 to bit 0 of *reg_mac_initcom*. This OOK modulation pattern may be used by the external base station 2.45 GHz transmitter. The contents of the wakeup pattern are set by programming various registers in the base station ZL70101 transceiver. The total wakeup packet length is 2.688 ms. Further details of the wakeup packet are described in the design manual.

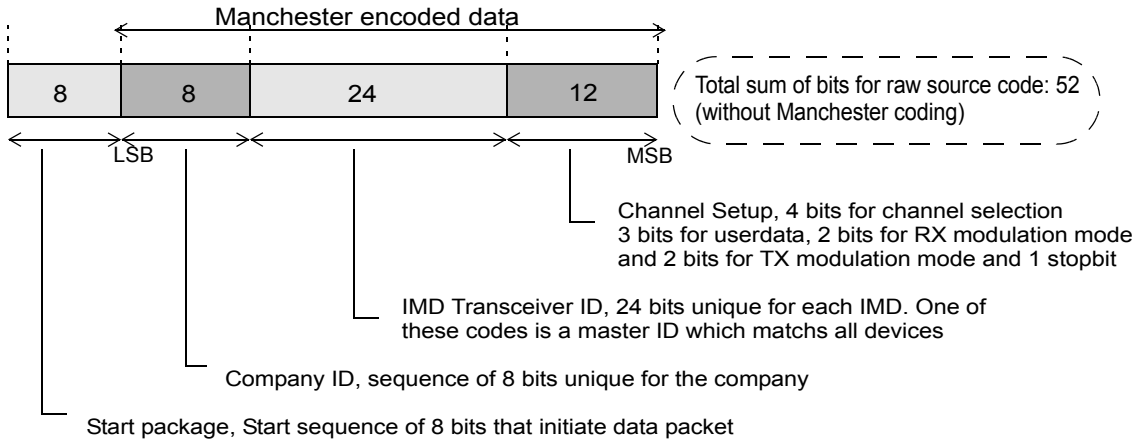


Figure 1-6 • **The Data Packet Definition**

Typically, the Base will first use a company ID (assigned by Microsemi) with a general IMD transceiver ID. This will wakeup all of the devices associated with the company ID within 2.4 GHz RF range. The IMD transceiver wakeup responses will contain their IMD transceiver ID. The base station user will then select a specific device for a communications session.

The 12 bits after the IMD transceiver ID consists of channel setup information required to establish a 400 MHz communications session. This information is sent to the MAC if a correct company ID and IMD transceiver ID is detected.

The channel setup information is Manchester encoded as per the rest of the data packet and therefore no additional error checking is considered necessary. The probability that these last 12 bits are incorrectly detected following a correct company ID and IMD transceiver ID correct is very low. Furthermore, any error will simply manifest as a delayed wakeup (it will need to be repeated). In addition, the user may use the user-defined bits for parity or other error checking of the channel setup information.

Media Access Controller (MAC)

The MAC is a digital subsystem that controls the data communication and application interface. The block diagram is shown below followed by a description of the basic operation.

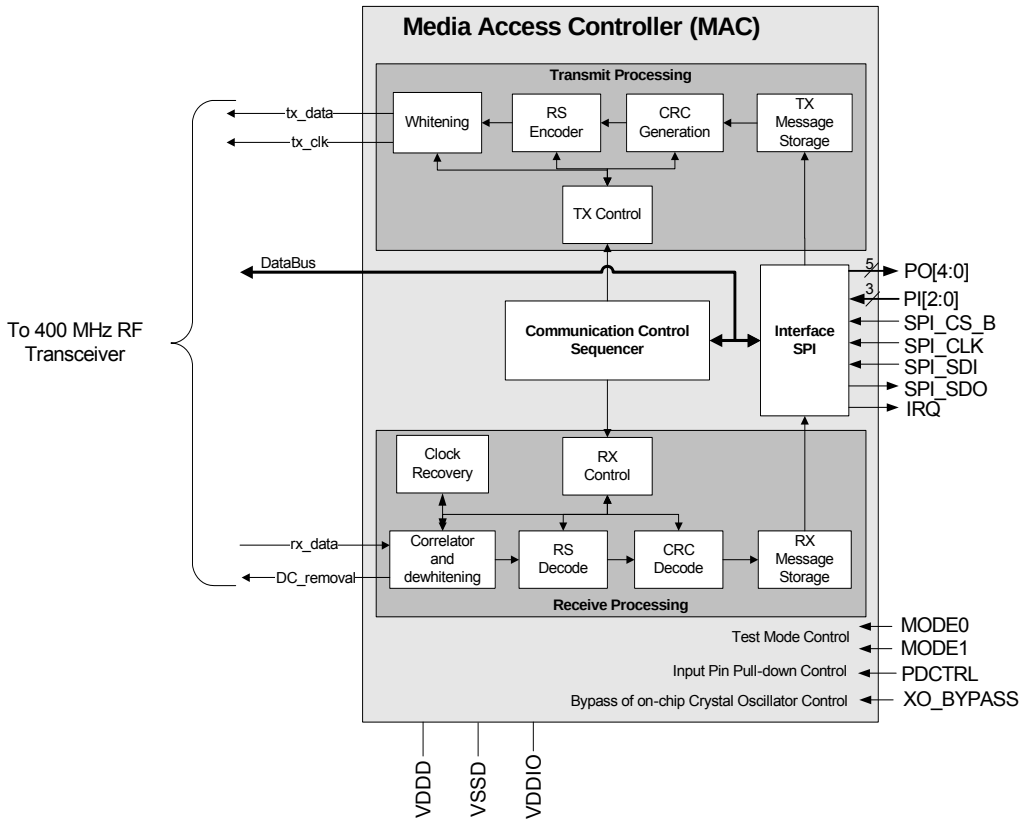


Figure 1-7 • **Media Access Controller Subsystem**

Basic Operation

The MAC consists of 4 main subsystems including:

1. Transmitter processing
2. Receiver processing
3. Communication control sequencer
4. Application Interface

The transmit processing is fed by a 64×113 bit storage buffer capable of storing 2 maximally sized packets. The buffer is simply a memory mapped address that is written through the SPI interface. The TX control will construct a data packet when more than 1 block of data exists in the transmit buffer. The definition of a data packet is contained in "400 MHz Packet Definition" section on page 1-12. A cyclic redundancy code (CRC) is appended to the data and the result is passed through a Reed-Solomon (RS) block that provides extensive forward error correction. The final stage of transmission processing is to perform whitening using a pseudo-noise (PN) method. Whitening ensures that the data has sufficient transitions for accurate operation of the clock recovery.

The receiver processing fills up a 64×113 bit storage buffer capable of storing 2 maximally sized packets. Again, the buffer is simply a memory mapped address that is read through the SPI interface. The receiver performs clock recovery by oversampling the received data and identifies the correlation word signifying the start of a packet. Upon receipt of a packet, a Reed-Solomon decoder performs forward error correction on the header and each of the blocks that constitute a packet. The RS is capable of correcting up to 15 consecutive bit errors within a block. After error

correction, a CRC decoder determines blocks which contain uncorrectable errors and forwards the information on which blocks require retransmission to the transmit controller and main sequencer.

The communication control sequencer implements and controls the overall ZL70101 communication protocol. The features offered by the protocol include:

- Correction and detection of errors (FEC and CRC)
- Automatic retransmission of data blocks in error (ACK/NACK)
- Automatic flow control to prevent buffer overflow
- Automatic setup of modulation modes and reply to wakeup responses
- Facility to flush old data (e.g., useful when sending real-time ECG data in poor link conditions)
- Capable of sending MICS emergency command
- Minimization of collisions from multiple implants during wakeup responses
- Ability to send high priority housekeeping messages
- Handling of link watchdog to ensure link is shutdown after 5 seconds without successful communication
- Provision of link quality diagnostics
- Backup of important registers to wakeup block and CRC checking of memory
- Control of automatic calibrations

The rich feature set of the ZL70101 communication protocol relieves the user application of many link maintenance activities. The communication link is simply viewed as a receive and transmit buffer accessible via the SPI interface. Buffer conditions that require user attention are flagged by interrupts allowing the user to optimally maintain data flow. The user may also choose to poll buffer status registers as an alternative to handling interrupts.

The application interface is discussed in more detail in "Application Interface" section on page 3-1.

400 MHz Packet Definition

The packet definition is chosen to enable a high effective data rate. The packet header should be kept as small as possible and the payload should be as large as possible. The same packet definition is used in both the uplink and downlink. The basis for the packet definition and the link protocol is fully described in the design manual.

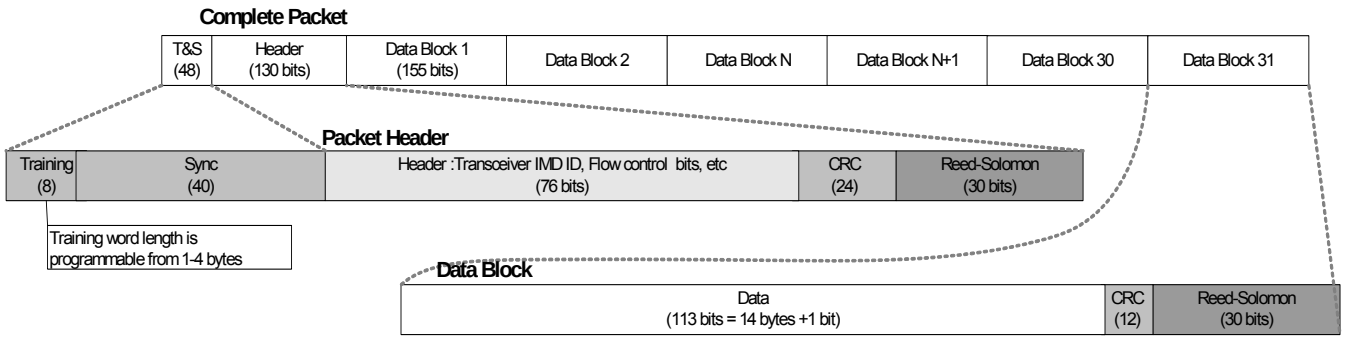


Figure 1-8 • **Packet Definition (first in time on the left side)**

The receiver contains a DC removal circuit that is adjusted at the beginning of each received packet. Therefore, the packet starts with an 8-bit training sequence defined by the register *reg_mac_trainword*. The number of times this 8-bit sequence is sent is programmable (1–4 times, default 2, using *reg_mac_trainnum*) and its optimal value will depend on the magnitude of the DC offset that must be removed. The receiver will use this training sequence to make a coarse adjustment of the DC level of the baseband signal. The two main sources of DC offsets are frequency differences between the transmitter and the receiver and imperfections in the detector. The training sequence is followed by a 40 bit synchronization word defined by the registers *reg_mac_sync[5:1]*. The number of bits that must match in the synchronization word is specified by the register *reg_mac_syncmatch.* The default value of this register is 36 (24 Hex) which allows a maximum of 4 errors in the synchronization word. The sliding correlator in the receiver will check against a known pattern. The synchronization word has been chosen so that its auto correlation is high only for zero lag.

The packet header contains flow control information that handles the automatic retransmissions of blocks in error, prevention of receiver buffer overflow, packet acknowledgement, HK related bits and other protocol details. These are fully described in the design manual. The header also contains the IMD transceiver ID, a unique 24 bit code that identifies the implant. The entire header is protected by a RS code and 24 bit CRC.

The header has a stronger CRC protection than the data since it is important that there are no undetected header errors. That would cause erroneous link operation with the system operation dependent on the header bits in error.

Each data block consists of 113 bits of effective data (14 bytes + 1 bit). The 1 additional bit may be used by the application in a transport layer for indicating the start of the users packet. The data block is protected by a 12-bit CRC. The resulting bits are protected by 30 bits of RS error correcting code.

The maximum number of blocks in a data packet is programmable (1–31) via the register *reg_txbuff_maxpacksize.* The system will send less than the maximum number of blocks if data is available in the TX buffer. In other words, data is sent as soon as it is available provided at least one block exists in the TX buffer. The register *reg_txbuff_maxpacksize* only sets a limit on the *maximum* blocks in a packet.

The number of bytes in a TX or RX block that needs to be transferred from the SPI interface is programmable (*reg_rxbuff_bsize, reg_txbuff_bsize)* as described in the "Serial Peripheral Interface" section on page 3-1. There will always be 113 bits sent in a data block but some of these bits will be padded zeroes if the number of bytes in a block is set to less than the maximum value of 15. When using all 113 bits (14 bytes + 1 bit, block size set to 15) then the LSB of the first byte sent by the SPI interface is used for the additional 1 bit. This single bit is not used when the block size is less than 15.

2 – System Reliability Features

System Integrity – Watchdogs

Several watchdogs have been provided to ensure that the implant transceiver is never locked in an unwanted power consuming state.

Some fundamental system requirements impact the specification of watchdogs

1. The implant transceiver shall never be locked in an unwanted power consuming state to which the application is unaware.
2. The application shall always be capable of resetting a device that has a failure in the application interface or transceiver.
3. The application shall control where possible the disconnection of links.
4. The system (application and transceiver) shall abort the link if no header is received in a period of 5 seconds.

The system timing varies at different stages of the ZL70101 transceiver operation which leads to three different watchdogs as described below. A watchdog of some type is always operating in the ZL70101.

Table 2-1 • **Summary of Watchdogs**

Watchdog	Purpose
Wakeup Watchdog. (IMD only)	Ensures wakeup block is shutdown if a loss of the 2.45 GHz data and clock is detected.
Transceiver Initialization Watchdog. (Base and IMD)	Ensures the system is put to sleep (IMD) or restarted (Base) in the event of a 24 MHz crystal failure or some other condition in which the MAC fails to start.
Main Watchdog (Base and IMD)	Ensures the link is shutdown after 5 seconds if no header is received. The MICS standard requires that the link is not occupied for greater than 5 seconds if no communication occurs. This watchdog also ensures that a device in Idle mode has serial interface communication with the application. The application is notified by an interrupt that occurs 0.6 seconds before the link will be shutdown and the IMD put to sleep. The application may override the shutdown by resetting the watchdog. During initial software development it is very convenient to disable the watchdog. Methods of disabling the watchdog are discussed in the design manual.

Memory Integrity – CRC Check of Registers

The MAC or application can perform a CRC check of selected registers in the wakeup block. The MAC does this action automatically at startup and the user may also perform the CRC check anytime the MAC is powered. The CRC check includes all registers labelled in the memory map for CRC checking.

The CRC operation is controlled by the register *reg_wakeup_crcctrl*. The user may initiate a check of the CRC using a control bit and status bits indicate if the CRC check passed or failed. The user can also calculate a new CRC word using a control bit and a status bit indicates that the calculation is complete. The application should control the copying of registers to the wakeup stack using the "copy registers" control bit in *reg_mac_ctrl*. It is recommended that such copying should only occur following a successful communication session since the register settings have been verified as operational. See the memory map for more details and requirements regarding the operation of the CRC control register.

Communication Link Integrity

The following features of the ZL70101 contribute to a high communication link integrity.

- The RS forward error correction and CRC provides for excellent final BER performance. For example, data blocks with 12 bit CRC protection, obtain a final effective BER of 1.5×10^{-10} given a raw radio BER of 10^{-3} and even better performance is available with housekeeping messages.
- Individual acknowledgement and retransmission of data blocks is automatically handled.
- The variable receiver sensitivity obtained by different modulation modes is useful for poor link conditions.
- Link quality diagnostics are available including:
  - number of corrected blocks.
  - number of blocks with errors detected.
- A link quality interrupt is generated when either of the block error or retransmission indicators exceed programmable thresholds.

Details of these features may be found in the ZL70101 design manual.

3 – Application Interface

This section describes the application interface including available methods for programming registers (SPI or Housekeeping messages), interrupts, programmable I/O and bypass modes.

Serial Peripheral Interface

Registers and the TX/RX buffers are programmed via a standard SPI slave interface. The design manual contains the full register map and programming details for the device.

The interface supports "mode 0 slave" operation where data is valid on the first rising edge of SPI_CLK, the idle state of SPI_CLK is low as shown in the basic timing diagrams below. The default maximum SPI_CLK rate is 2.4 MHz. A register (*reg_interface_mode)* may be programmed to increase this operating speed to 4.4 MHz.

A typical connection between the application and the ZL70101 Transceiver SPI interface is shown below. The application initiates the data transfer by driving the SPI_CS_B pin low. Data from the application is presented to SPI_SDI whilst data to the application is presented to SPI_SDO. Both input and output are clocked using the input SPI_CLK.

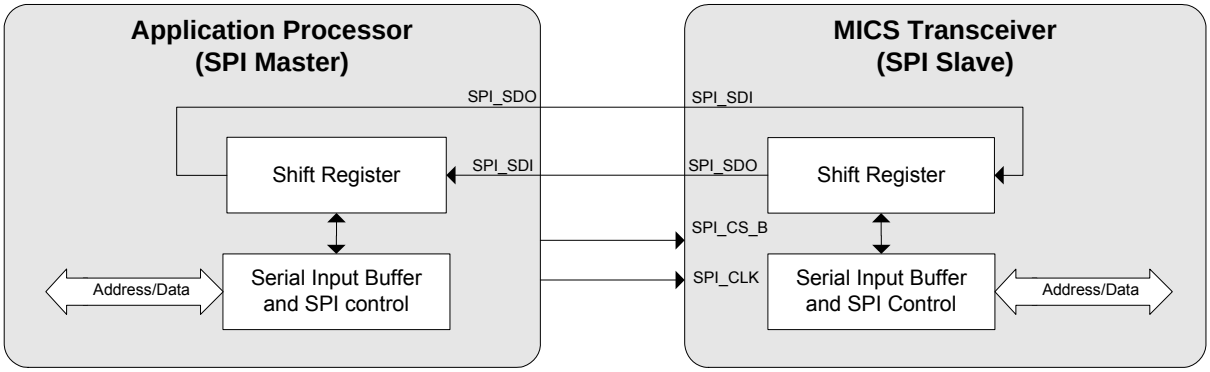


Figure 3-1 • **SPI Interface**

For writing to a register SPI_CS_B is driven low giving access to the internal parallel bus on the ZL70101 transceiver. The application sends out address bits so data can be sampled on the rising edges of SPI_CLK. The write bit (A7 = 0) and 7 address bits are shifted into the ZL70101 transceiver on the SPI_SDI pin. The 8 address bits including the write bit are loaded into an address register. The address byte is followed by the data byte.

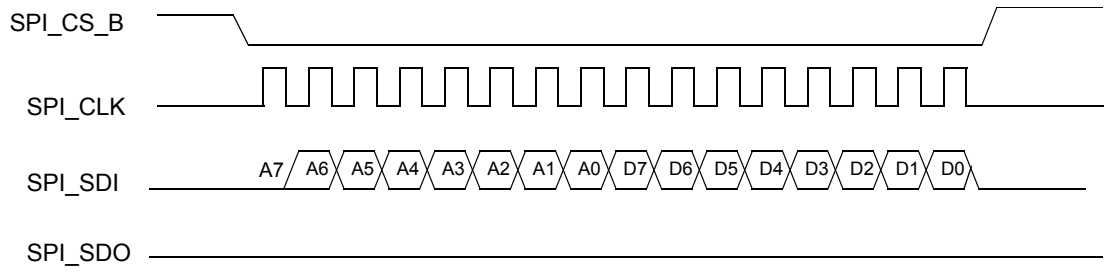


Figure 3-2 • **Timing for SPI Write of One Byte**

SPI_CS_B is driven low giving access to the internal parallel bus on the ZL70101 transceiver. Address or data changes can occur on the falling edge of SPI_CLK. Address and data bits, provided on the SPI_SDI pin, are sampled by the ZL70101 transceiver on the positive edge of SPI_CLK. The first bit (A7 = 1) indicates a read command. Read

data is clocked out on the SPI_SDO pin on the falling edge of SPI_CLK. The application will sample read data on the positive edge of SPI_CLK.

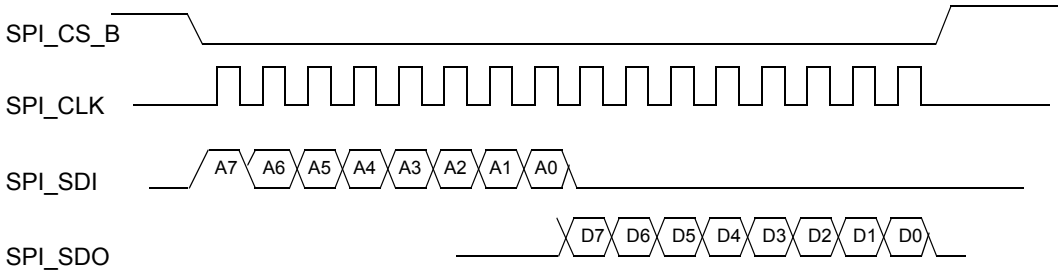


Figure 3-3 • **Timing for SPI Read of One Byte**

Buffer Operation and Automatic Internal Address Increment

Automatic internal address increment is a process where the first address of a block of data is followed by the complete data block. The SPI-interface supports automatic internal address increment for accessing of the TX and RX buffers (*reg_txrxbuff*) only. A single address is used to access the buffer addresses and the internal address (or pointer) within the buffer is then automatically incremented for each byte of data that follows. The interface efficiency is improved since there is no need to send the buffer address with each byte of data. The first byte after assertion of SPI_CS_B is used to identify the address byte. A read operation to *reg_txrxbuff* accesses the TX buffer whilst a write operation will access the RX buffer.

The number of bytes in a TX or RX data block that needs to be transferred from the SPI interface for a block to be constructed into a TX packet or read from the RX buffer is programmable (*reg_rxbuff_bsize, reg_txbuff_bsize).* The value may range from 2 to 15. For small amounts of data this simplifies the SPI interface operation since only the number of desired bytes need be read or written for the internal block counters (*reg_rxbuff_used, reg_txbuff_used*) to change.

Address Checking

Address checking will detect errors in the address. This feature is included for very high reliability applications that may operate in electrically noisy environments.

Every address byte will be sent twice where the first byte sent is the true value and the second byte is the bit wise complement. The receiver will check if the two bytes are bit-wise complements. The general sequence for address checking is shown below. Address checking is enabled and disabled by a bit in the register *reg_interface_mode.* The default is disabled.

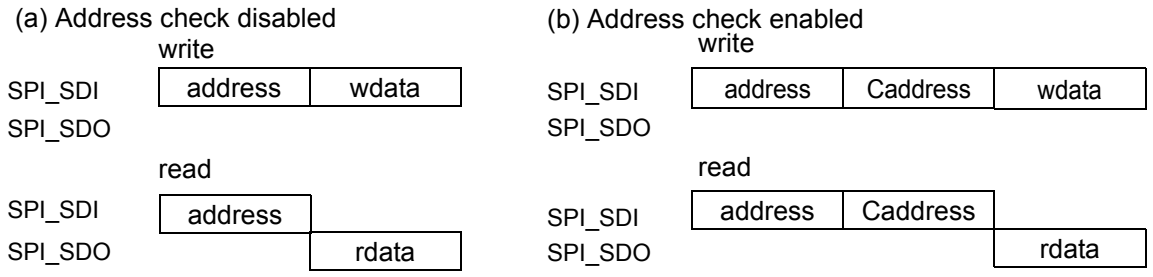


Figure 3-4 • **Read and Write of One Byte Showing Address Checking (each box represents 1 byte of data)**

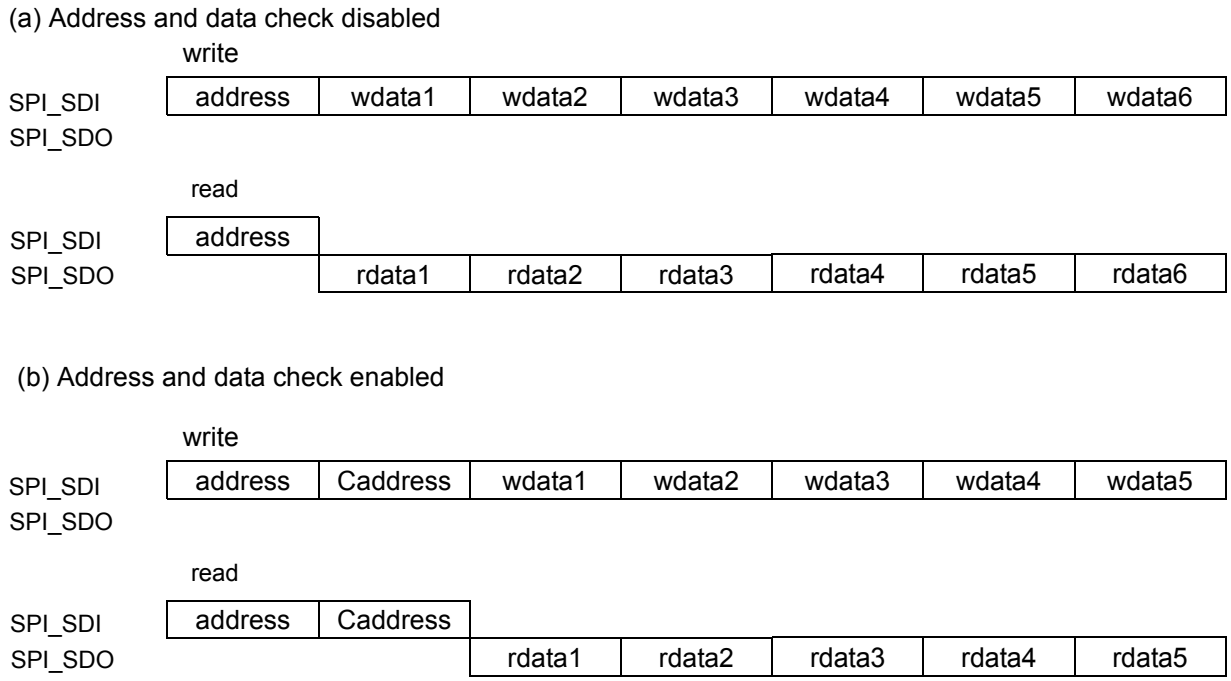


Figure 3-5 • **Timing for Read and Write Using Automatic Address Increment (TX/RX buffers only)**

Multiple Devices on the SPI-Bus

Support for multiple devices on the SPI-bus is considered mandatory for most microprocessor systems. Many applications may require more memory for program or data than will be resident in a typical processor. In addition, implant systems are frequently I/O limited and demand sharing of the databus.

The ZL70101 transceiver supports multiple devices on the "SPI-bus" databus. The ZL70101 transceiver acts as a slave with the signal SPI_CS_B selecting the chip. The SPI_SDO output, on a slave (e.g., ZL70101 transceiver), shall be tristated when the chip is not accessed (SPI_CS_B into chip is high).

Housekeeping Messages

A HK message is a method of communicating directly with status and control registers in a remote transceiver in a similar manner to the local SPI interface. The data and address in the remote transceiver is sent in the radio packet header instead of via the SPI interface. There is one bit within the packet header (the HK bit) indicating that the header is a HK message. A HK message is sent as a header only packet with the packet HK bit asserted. HK messages may be sent at any time by writing to the HK control registers.

HK messages have higher priority than packets containing data so it is possible to send high priority messages using HK. Eight bit data can be sent to special registers (*reg_hk_userdata, reg_hk_userstatus*) in the receiving ZL70101 transceiver, and an IRQ will alert the receiving application that there is new HK data.

HK messages may be used to read and write to remote registers, transfer small amounts of data (1 byte at a time) or perform an action in the remote device that is initiated by a register write. Housekeeping messages are useful for down-loading software, remotely performing calibrations such as a base station in production requesting calibrations in an implant, operation of an implant transceiver without the need for an implant processor and transfering high priority small amounts of data with excellent CRC error detection. An effective BER of 2×10^{-14} BER (assuming a raw radio BER of 10^{-3}) is available using housekeeping messages due to the 24 bit CRC protection offered by the header packet.

HK messages feature a security mechanism that prevents unauthorized devices from remotely programming a transceiver. This feature is discussed in detail in the design manual.

Interrupts

The ZL70101 has been designed to ease user software development. The application may choose to develop software using an interrupt service routine or may simply use polling of various status registers within the device. Important status changes in the ZL70101 transceiver are signified by the assertion of an IRQ (Interrupt request).

Interrupts are provided for the following purposes

- Buffer control (e.g., rx buffer not empty, tx buffer full)
- Housekeeping message control
- Radio and link status and quality indicators (e.g., radio ready, link established)
- Radio operation error conditions (e.g., backup memory CRC error)

A maximum of 3 register reads are required to determine the interrupt source. The interrupt controller provides interrupt raw source status, interrupt status after masking and an enable register. The enable register is used to determine if an active interrupt source should generate an interrupt request to the processor. The enable register has a dual mechanism for setting and clearing the enable bits. This allows enable bits to be set or cleared independently, with no knowledge of the other bits in the enable register. Such an approach simplifies interrupt software design. The control and clearing of interrupts is fully described in the design manual.

Programmable I/O and Bypass Modes

Programmable input/output pins are very useful for many applications. They provide polled outputs, direct access to status conditions within the ZL70101 transceiver, user defined interrupt pins, user defined general purpose outputs and clock signals, access to bypass mode outputs and access to specific base station outputs.

Programmable Output Sources

Five output pins are available that may be programmable to directly display useful outputs. The programmable output sources including support for general purpose outputs, clock outputs, base station outputs, interrupts and bypass outputs (MAC bypass mode and RF bypass mode). The MAC and RF bypass modes are set by asserting appropriate bits in the register – *reg_interface_mode*. The MAC Bypass bit has priority if both are asserted.

One select register is used for each pin to select the signals assigned to each POx. PO0–PO3 are defined using the registers called *reg_pox*, (where x = 0, 1, 2, 3 is the pin number) and PO4 is defined with the register reg_mac_clkrecctrl giving a total of 5 registers. Several other registers controlling multiplexing of signals to these outputs and the available signals and register programming requirements are detailed in the design manual.

Support for General Purpose Outputs: The general purpose outputs (control register bit = 0,default) provide pin-constrained applications with some additional digital outputs. These outputs are set by writing the desired output value to the appropriate bit in *reg_gpo*. These general purpose outputs may also be used by size-constrained implant applications in which removal of the implant application processor is desirable. In this case, the general purpose outputs provide rudimentary digital control for the implant. It should be noted that these outputs shall be set low when the transceiver is asleep.

Support for additional IRQ/status Outputs: Most of the raw IRQ interrupt sources are available on pins PO0, PO1 and PO3. These support polled I/O processor communication or applications preferring multiple interrupts. The interrupts associated with PO0 and PO1 are mainly normal link and radio status conditions. The interrupts associated with are PO2 are mainly warning and error conditions.

Support for Selectable Clock Output: The pin PO3 may be used as a programmable clock. The values selected are extracted from a ripple counter operating from the 24 MHz system clock.

Support for MAC and RF Bypass modes: These modes require digital I/O and are described in later sections.

Support for Base station Controls: The programmable outputs provide several signals useful for supporting the base station operation. These signals are defined in Table 3-1 below:

Table 3-1 • **Summary of Base Station Control Signals**

Base Station Control Signal	Description
TX245	OOK digital modulation wakeup pattern produced by MAC powerup block.
TX_MODE	TX_MODE is high when both the TX_IF and TX_RF blocks are enabled. The transmitter will not begin transmitting until 15 µs after the TX_MODE signal is asserted. The blocks are turned off < 1 µs after TX_MODE goes low. For convenience, some systems may prefer an active low variant of this signal, therefore,TX_MODE_B = $\overline{\text{TX\_MODE}}$
RX_MODE	RX_MODE is high when both the RX_IF and RX_RF blocks are enabled. The receiver blocks will not be fully functional until 15 µs after the RX_MODE signal is asserted. The blocks are turned off < 1 µs after RX_MODE goes low. For convenience, some systems may prefer an active low variant of this signal, therefore, RX_MODE_B = $\overline{\text{RX\_MODE}}$

Support for IMD: One of the programmable outputs (PO4) is placed on the right side of the chip to make it available also when the upper side of the chip is not bonded (typical on implants) to save area. This output can be programmed to provide the same signal as defined to any of the other 4 programmable outputs (PO0–PO3). PO4 can also provide TX_MODE, TX_MODE_B, RX_MODE or RX_MODE_B.

Programmable Input Sources

The programmable input (PI0, PI1, PI2) pins may be used as general purpose inputs available as a register in the memory map. They are also used for bypass modes and test purposes.

MAC Bypass Mode

Some users may choose to bypass the MAC and develop their own message control, forward error correction and CRC error detection. The MAC bypass mode is a complete bypass of the MAC TX and RX datapaths, except for the clock recovery and correlation circuit. The mode is also useful for system testing such as receiver sensitivity tests. The application may choose to bypass the correlation circuit and use a user defined correlation method.

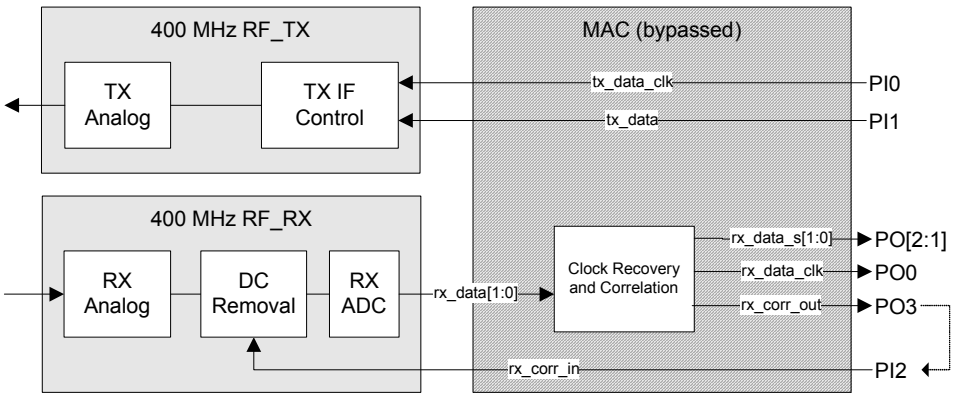


Figure 3-6 • **MAC Bypass Mode**

RF Bypass Mode

The RF bypass mode is a complete bypass of the RF block that is useful for evaluation and testing. In such an RF bypass mode, external hardware and/or software could be used to model the RF channel and precisely emulate errors without the need for an RF link. Data and clock control signals normally intended for the TX modulator are routed to programmable outputs and similarly data normally from the RX ADC are derived from programmable inputs. Burst errors and poor link conditions may be easily modeled and the systems response to such conditions may be evaluated.

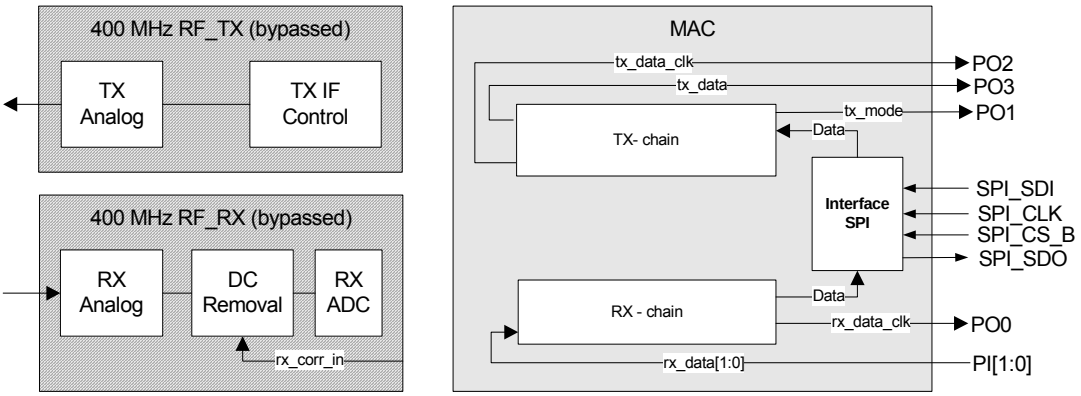


Figure 3-7 • **RF Bypass Mode**

Error Correction and Detection Bypass

The Reed-Solomon FEC encoder, CRC encoder and whitening blocks may be individually bypassed in the transmit chain. Similarly, in the receiver chain, the RS decoder, CRC decoder and dewhitening may be individually bypassed. These selective bypasses are useful for test and evaluation and are controlled by the *reg_mac_bypass* register.

4 – Calibrations

Calibrations are needed for optimal transceiver performance. The majority of calibrations require no external equipment and may be performed very quickly (< 10 ms) by a single register write to the calibration initiation bit in *reg_mac_ctrl*. The only exceptions that require external equipment are the XO tuning, which requires a precise RF reference frequency, the output power trimming, which requires an external power meter, the RSSI trimming, which requires an external signal and the RX antenna tuning which also requires an external signal.

Some calibrations need only be performed once in the factory whilst other calibrations should be performed before each communication session.

The following parameters can be calibrated:

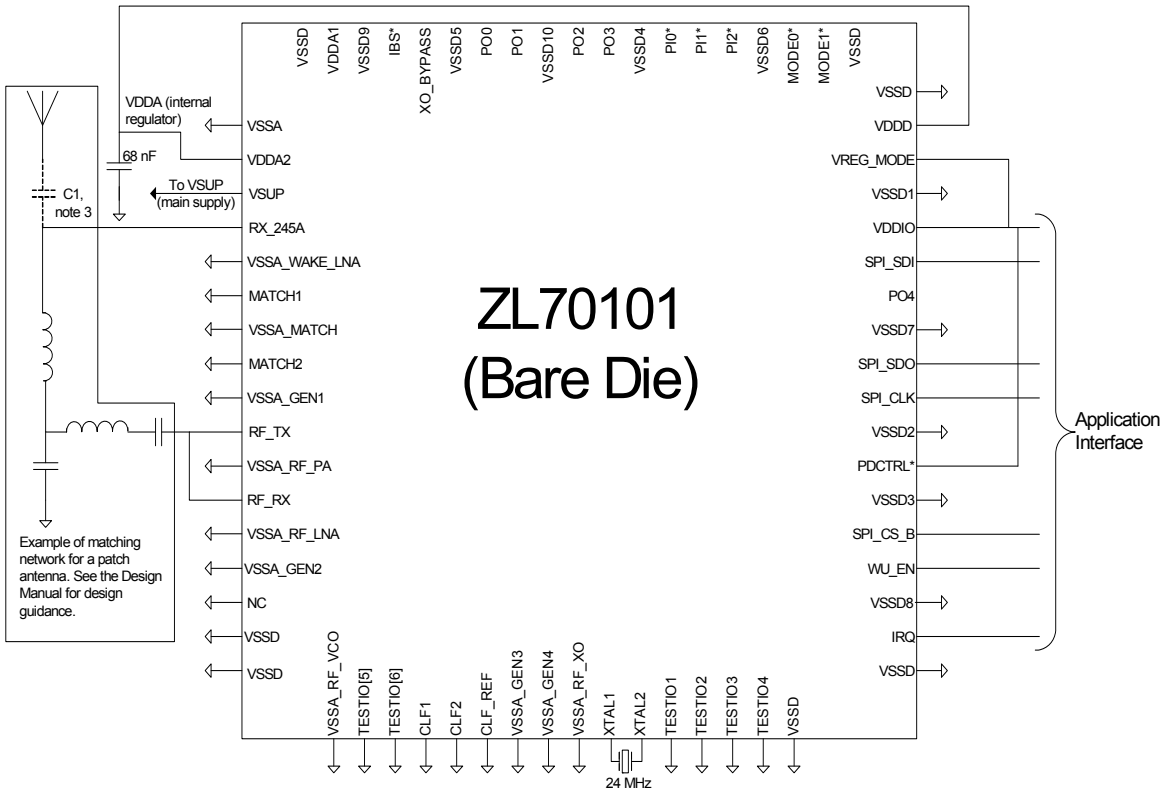
- Wake-up strobe oscillator tuning
- TX IF oscillator tuning
- RSSI offset trimming
- FM detector and RX IF tuning
- RX ADC trimming
- 400 MHz TX antenna tuning
- 400 MHz RX antenna tuning
- 2 additional antenna tuning capacitors (MATCH1 and MATCH2)
- XO tuning
- Output power trimming
- 2.45 GHz detector zero trimming
- 2.45 GHz antenna tuning (This automated calibration does not work correctly and gives always maximum code. This calibration must be done manually once in production.)

All calibrations are optional and the application has full control over initiations. Calibrations are performed by writing and reading registers in the ZL70101 transceiver using the SPI or HK messages. At device powerup or wakeup, calibrations defined by the register *reg_mac_calselect1,* are performed automatically by the MAC. After this the user may perform calibrations at any time by selecting the calibrations to perform (*reg_mac_calselect1*) and then initiating the calibrations by writing to the calibration initiation bit in *reg_mac_ctrl*.

Generally after the battery is first attached to an implant, the implant housing is sealed and implant software is downloaded. A base station in the implant manufacturer's facility may then wakeup the implant and use HK commands to download software and perform all the factory and operational calibrations. Note that a reduced range is expected for a precalibrated device as defined in the design manual. The design manual also discusses methods for downloading software in a new or implanted device.

5 – Example Configurations

The ZL70101 Transceiver device is configurable as an implant transceiver or as a base station transceiver. Typical configurations are shown in the following diagrams. Two different configurations for implants are shown, the first is optimized for few external components and the second is optimized for highest performance.

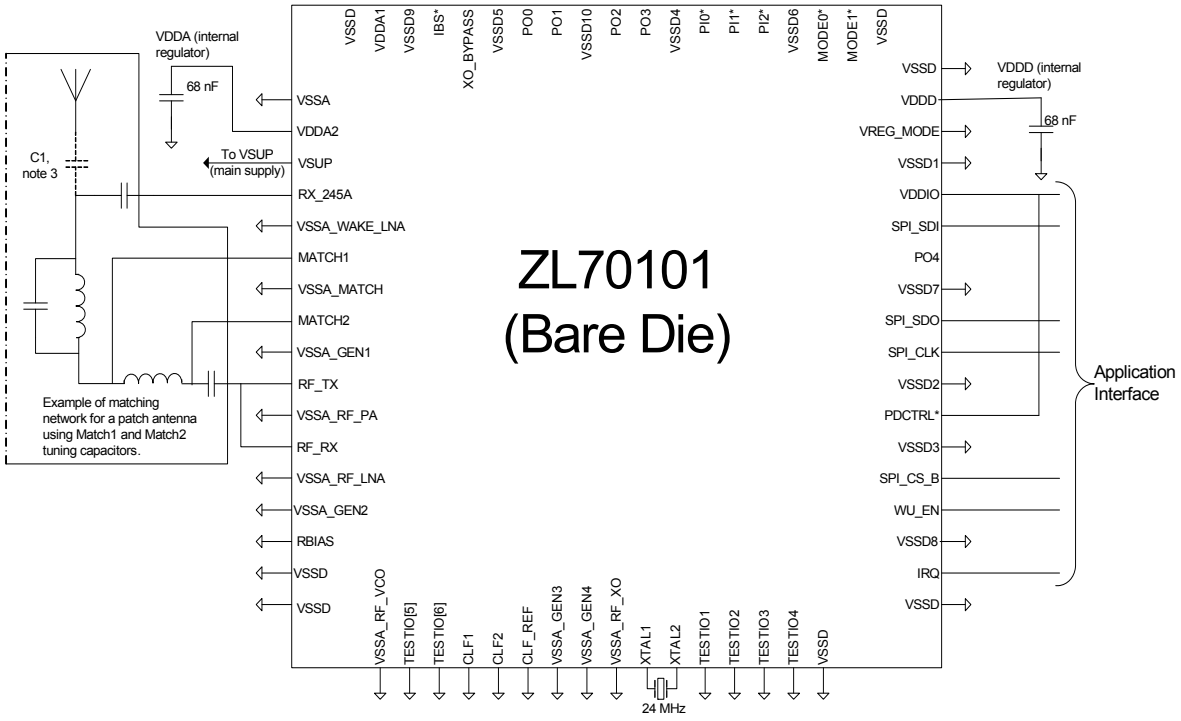


Note 1: *Inputs connected via internal pull-down to ground. Upper side pins do not need to be bonded out

Note 2: Two supply voltages are required, VSUP (the main supply, 2.1-3.5V) and VDDIO (the digital IO voltage which may be 1.5V to VSUP). VDDA is an on-chip derived regulated supply created by a voltage regulator connected to the VDDA 1 and VDDA2 pads. VDDA requires a 68nF decoupling capacitor and a connection between VDDD and VDDA 2. VREG_MODE is bonded to VDDIO in this example (only the VDDA voltage regulator enabled).

Note 3: C1 is an optional DC blocking capacitor.

Figure 5-1 • **ZL70101 Transceiver Configured for an Implant – Minimum External Components**



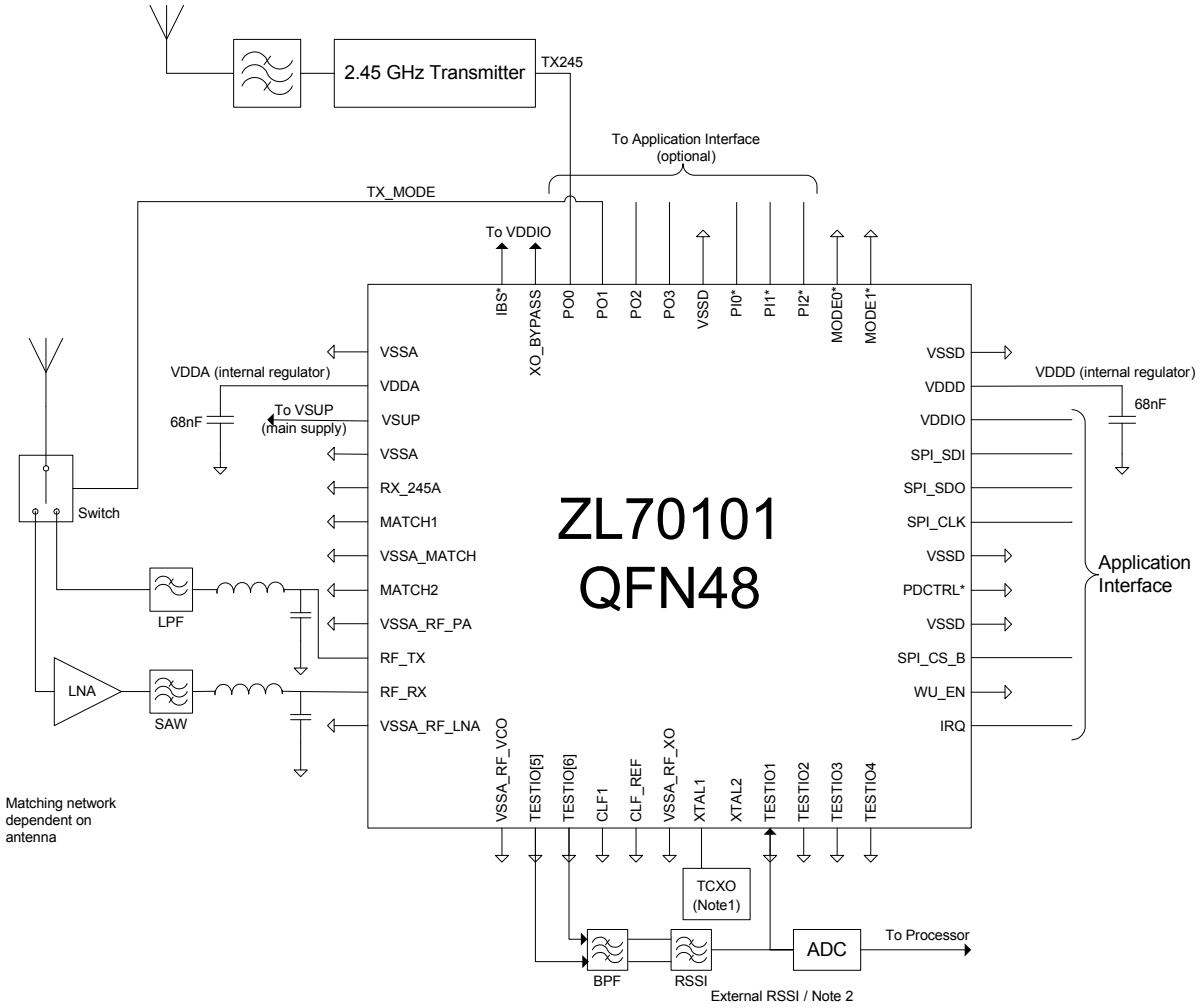
Note 1: *Inputs connected via internal pull-down to ground. Upper side pins do not need to be bonded out

Note 2: Two supply voltages are required VSUP (the main supply,2.1-3.5V) and VDDIO (the digital IO voltage which may be 1.5V to VSUP) VDDA and VDDD are both on-chip derived regulated supplies. VDDA and VDDD require two separate 68 nF decoupling capacitors. VREG_MODE is bonded to GND in this example (both analog and digital voltage regulators enabled).

Note 3: C1 is an optional DC blocking capacitor.

Note 4: The matching network is using the on-chip tuning capacitor arrays to GND (VSSA_MATCH) available on the Match1 and Match2 pads.

Figure 5-2 • **ZL70101 Transceiver Configured for an Implant – Optimal Performance**



Note 1: For Basestation, a TCXO is recommended (in which case XO_BYPASS is tied high)

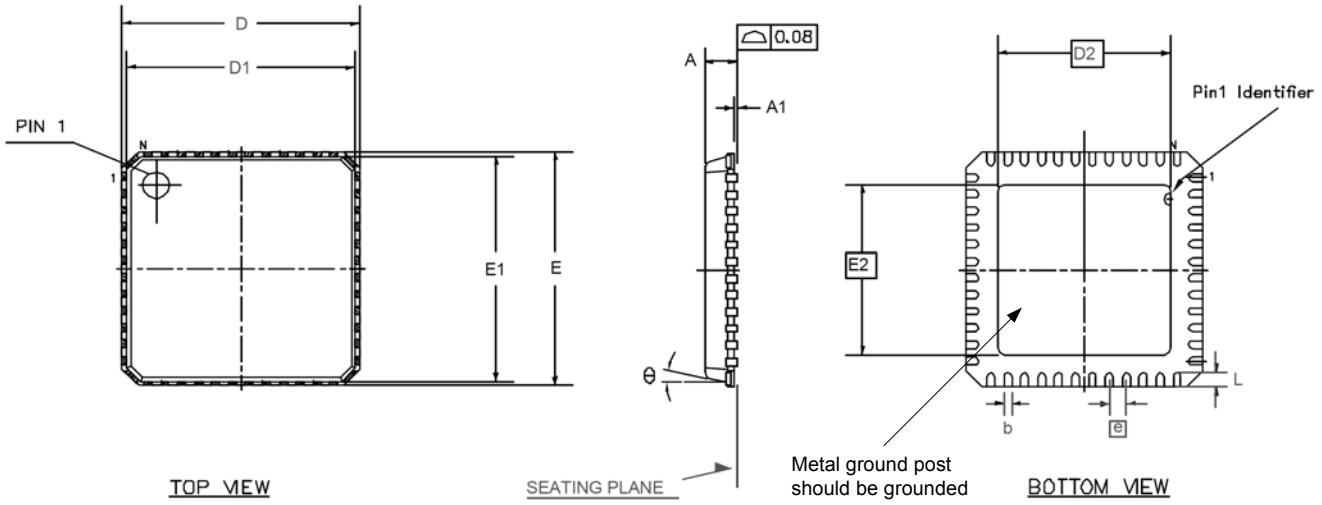
Note 2: External RSSI Detector System is recommended. Connection to be done either to MICS chip after RSSI or direct to application

Note 3: Two supply voltages are required VSUP (the main supply,2.1-3.5V) and VDDIO (the digital IO voltage which may be 1.5V to VSUP) VDDA and VDDD are both on-chip derived regulated supplies. VDDA and VDDD require two separate 68 nF decoupling capacitors. VREG_MODE is bonded to GND inside the QFN package in this example (both analog and digital voltage regulators enabled).

Figure 5-3 • **ZL70101 Transceiver Configured for a Base Station**

6 – Mechanical Characteristics

48 Pin QFN Package



SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	0.800	0.850	0.900
A1	0.005	0.025	0.045
b	0.180	0.230	0.300
D	6.900	7.000	7.100
D1	6.650	6.750	6.850
D2	5.10 BSC		
E	6.900	7.000	7.100
E1	6.650	6.750	6.850
E2	5.10 BSC		
N	48		
Nd	12		
Ne	12		
e	0.50 BSC		
L	0.300	0.400	0.500
θ	10°	11°	12°

Conforms to JEDEC MO-220

NOTES:
1. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
2. N IS THE NUMBER OF TERMINALS.
   Nd & Ne ARE THE NUMBER OF TERMINALS IN X & Y DIRECTION RESPECTIVELY.
3. ALL DIMENSIONS ARE IN MILLIMETERS.
4. LEAD COUNT IS 48
5. PACKAGE WARPAGE MAX 0.08mm.
6. NOT TO SCALE.

Figure 6-1 • **48 Pin QFN Dimensions**

Die

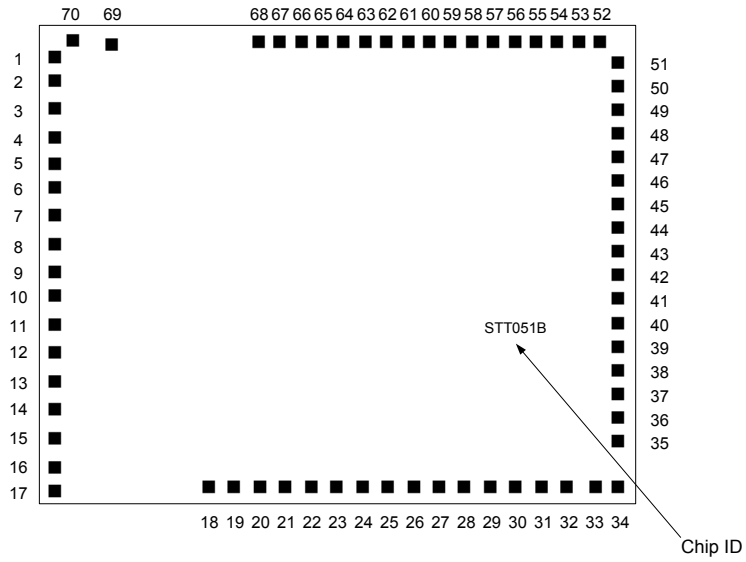


Figure 6-2 • **ZL70101 Die**

Table 6-1 • **Pad Coordinates Positions [µm], Chip Center as Reference**

Pad	Coordinate [x,y]	Pad	Coordinate [x,y]	Pad	Coordinate [x,y]	Pad	Coordinate [x,y]
1	−1971, 1323	18	−890, −1406	35	1986, −1116	52	1862, 1421
2	−1971, 1173	19	−710, −1406	36	1986, −966	53	1712, 1421
3	−1971, 993	20	−530, −1406	37	1986, −816	54	1562, 1421
4	−1971, 813	21	−350, −1406	38	1986, −666	55	1412, 1421
5	−1971, 644	22	−170, −1406	39	1986, −516	56	1262, 1421
6	−1971, 494	23	10, −1406	40	1986, −366	57	1112, 1421
7	−1971, 314	24	190, −1406	41	1986, −216	58	962, 1421
8	−1971, 134	25	370, −1406	42	1986, −66	59	812, 1421
9	−1971, −46	26	550, −1406	43	1986, 84	60	662, 1421
10	−1971, −197	27	730, −1406	44	1986, 234	61	512, 1421
11	−1971, −377	28	910, −1406	45	1986, 384	62	362, 1421
12	−1971, −557	29	1090, −1406	46	1986, 534	63	212, 1421
13	−1971, −737	30	1270, −1406	47	1986, 684	64	62, 1421
14	−1971, −917	31	1450, −1406	48	1986, 834	65	−88, 1421
15	−1971, −1105	32	1630, −1406	49	1986, 984	66	−238, 1421
16	−1971, −1283	33	1832, −1406	50	1986, 1134	67	−388, 1421
17	−1971, −1433	34	1986, −1406	51	1986, 1284	68	−538, 1421
						69	−1570, 1398
						70	−1845, 1427

Table 6-2 • **Die Specification**

	Parameter		Unit	Notes
1	Die area (x, y)	4275 × 3145	um	Maximum size
2	Die thickness	250 ± 25	um	
3	Pad size	80 × 80	um	
4	Pad metal	Al/Cu		
5	Backside potential	GND		

7 – Electrical Characteristics

Table 7-1 • **Absolute Maximum Ratings**
Voltages are with respect to ground (VSS) unless otherwise stated.

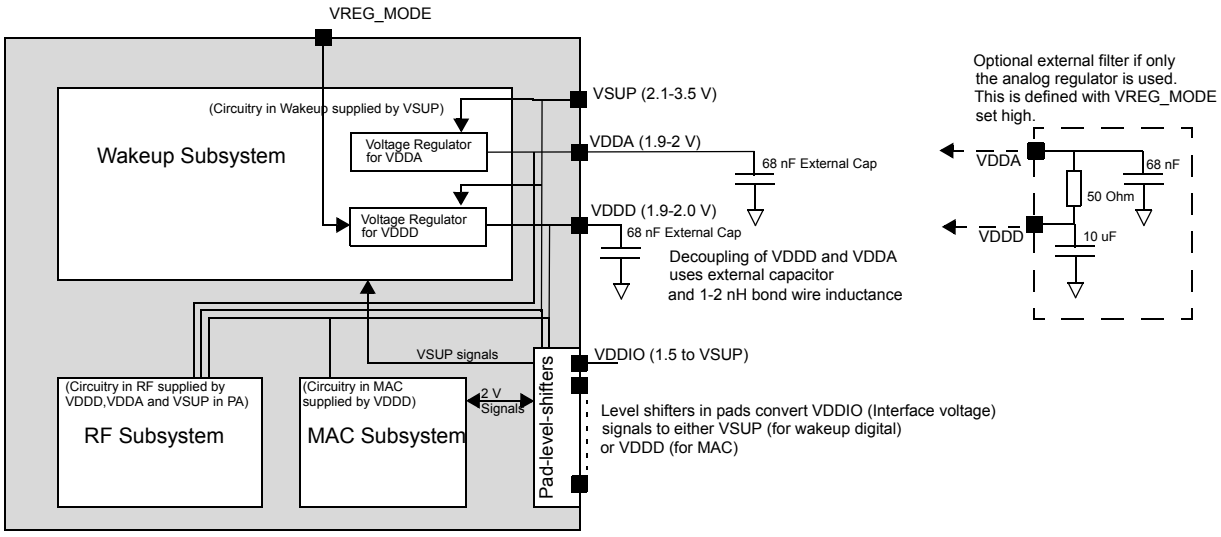
	Parameter	Symbol	Min.	Max.	Unit	Notes
1	Supply voltage	VSUP	0	3.6	V	
2	Input voltage (Digital I/O)	VDDIO	0	VSUP	V_{peak} rel. to VSS	
3	Unpowered Storage temperature	T_{stg}	−40	+125	°C	

Table 7-2 • **Recommended Operating Conditions**
(See Note 1)

	Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
4	Supply voltage	VSUP	2.1		3.5	V	
5	Input voltage (Digital I/O)	VDDIO	1.5		VSUP	V	Note 2
6	Operating temperature	T_{op}	0		55	°C	
7	Extended Operating temperature	T_{op_ext}	−20		60	°C	Limited requirements [3]

Notes:

1. *This table lists the external conditions under which the chip shall operate according to the specifications detailed within this document.*
2. *Note that VDDIO must never be higher than VSUP even during system startup.*
3. *The requirements specified in this extended temperature range are limited to digital functionality and to the following parameters with increased current limits: #27 I_{sleep_ext} (max 200nA), #28 I_{sleep_int} (max 600nA), #29 I_{listen} (max 1mA)*



Notes:

1. *VREG_MODE is used to define if the two regulators shall be used or if only the analog regulator shall be used. This is done by externally setting VREG_MODE low (= two regulators) or high (= one regulator). If both regulators are used then two external 68nF decoupling capacitors are needed, one for VDDA and one for VDDD. If only one regulator is used then the two decoupling capacitors should be replaced with an external filter to suppress digital noise into the analog supply. Another option is to use one regulator and VDDA and VDDD shorted together and using only one 68nF storage capacitor. This can result in a slightly increased BER. It is recommended to use two regulators by setting VREG_MODE low for best performance. VREG_MODE is bonded to GND (two regulators) in the QFN packaged devices.*
2. *In addition, both the two internal voltage regulators may be turned off via register programming in which case VDDA and VDDD must be supplied externally.*

Figure 7-1 • **Chip Power Supply Summary**

The digital interface electrical specifications are summarized below. The interface voltage is determined by the VDDIO pin voltage. This allows for users to interface to a wide range of system voltages. The XTAL1 input when XO_BYPASS is set high is an exception. This input requires a logic level compatible with the internal VDDD supply. The maximum output load and frequency of operation for each I/O are shown in the pin-list descriptions.

Table 7-3 • **Digital Interface Electrical Characteristics**
The parameters tested in production with different limits, different conditions or not tested are indicated with *, ** or *.**

	Parameter	Symbol	Min.	Typ.	Max.	Unit	Notes
8	Digital Interface Voltage	VDDIO	1.5		VSUP	V	
9	Digital I/O input low *	VIL	0		300	mV	Note 1
10	Digital I/O input high *	VIH	VDDIO–300		VDDIO	mV	Note 2
11	XTAL1 input low *	VIL_{XTAL1}	0		300	mV	Note 1,3
12	XTAL1 input high *	VIH_{XTAL1}	VDDD–300		VDDD	V	Note 2,3
13	Digital I/O output low	VOL	0		150	mV	I_{load}=1mA
14	Digital I/O output high	VOH	VDDIO–150		VDDIO	mV	I_{load}=−1mA
15	Digital I/O input leakage (WU_EN, SPI_CS_B, SPI_CLK, SPI_SDO, SPI_SDI, PDCTRL, MODE0, MODE1, PI0, PI1, PI2, XTAL1, XO_BYPASS)	I_{leak}	−10		10	nA	V_{out}=0V and 3.5V

* *These parameters are tested in production but with a different limit to that specified in the data sheet. This is due to limitations in the capabilities of the automated test equipment. The production tests that are carried out, coupled with correlation to tests carried out in the lab environment mean that the parameters are guaranteed.*

** *These parameters are guaranteed by production tests, however these may be carried out in a different manner to that defined in the data sheet.*

*** *These parameters are for design aid only: not guaranteed and not subject to production testing.*

Notes:

1. *VIL is the required input voltage to ensure internal signal switching from high to low.*
2. *VIH is the required input voltage to ensure internal signal switching from low to high.*
3. *A digital input to XTAL1 is only applicable when the XO is bypassed by setting XO_BYPASS high.*

Table 7-4 • **Performance Characteristics**
VSUP = 2.1V–3.5V and T = 0°C–55°C unless otherwise stated. The parameters tested in production with different limits, different conditions or not tested are indicated with *, **,* or ****. See also Notes 1 to 10 on page 7-9.**

	Parameter	Symbol	Min.	Typ. ****	Max.	Unit	Notes
General RF Parameters							
16	Radio frequency (MICS)	F_{RF_MICS}	402.0		405.0	MHz	MICS Band
17	Radio frequency (ISM)	F_{RF_ISM}	433.5		434.4	MHz	ISM Band
18	Channel Width	CW			300	kHz	10 channels MICS 2 Channels ISM
19	Raw Data Rate (4FSK)	D_{4FSK_raw}		800		kbps	4FSK
20	Error Corrected Data Rate (4FSK)	D_{4FSK_ec}		528		kbps	4FSK with BER 10^{-9}
21	Raw Data Rate (2FSK High Rate)	D_{2FSKhr_raw}		400		kbps	2FSK
22	Error Corrected Data Rate (2FSK High Rate)	D_{2FSKhr_ec}		267		kbps	2FSK with BER 10^{-9}
23	Raw Data Rate (2FSK High Sensitivity)	D_{2FSKhs_raw}		200		kbps	2FSK
24	Error Corrected Data Rate (2FSK High Sensitivity)	D_{2FSKhs_ec}		134		kbps	2FSK with BER 10^{-9}
25	Bit Error Rate of RF channel for data blocks	BERdata		1.5×10^{-10}		Errors/ bit	Including Error correction assuming raw channel quality BER 10^{-3}
26	Bit Error Rate of RF channel for housekeeping messages	BERhk		2×10^{-14}		Errors/ bit	Including Error correction assuming raw channel quality BER 10^{-3}

* *These parameters are tested in production but with a different limit to that specified in the data sheet. This is due to limitations in the capabilities of the automated test equipment. The production tests that are carried out, coupled with correlation to tests carried out in the lab environment mean that the parameters are guaranteed.*

** *These parameters are guaranteed by production tests, however these may be carried out in a different manner to that defined in the data sheet.*

*** *These parameters are for design aid only: not guaranteed and not subject to production testing.*

**** *Typical figures are at 37°C, VSUP=3.0V and for design aid only: not guaranteed and not subject to production testing.*

Table 7-4 • **Performance Characteristics (continued)**
VSUP = 2.1V–3.5V and T = 0°C–55°C unless otherwise stated. The parameters tested in production with different limits, different conditions or not tested are indicated with *, **,* or ****. See also Notes 1 to 10 on page 7-9.**

	Parameter	Symbol	Min.	Typ. ****	Max.	Unit	Notes
Current Consumption							
27	Current, Sleep Mode (External strobe), Die	$I_{sleep\_ext\_die}$		10	100	nA	WU_EN low, between ext. strobe pulses
	Current, Sleep Mode (External strobe), QFN	$I_{sleep\_ext\_qfn}$		10	500	nA	WU_EN low, between ext. strobe pulses
28	Current, Sleep Mode (Internal strobe), Die	$I_{sleep\_int\_die}$			500	nA	WU_EN low, between int. strobe pulses
	Current, Sleep Mode (Internal strobe), QFN	$I_{sleep\_int\_qfn}$			900	nA	WU_EN low, between int. strobe pulses
29	Current, Listen Mode	I_{listen}			715	uA	Bias code=10
30	Current, Sleep/Listen Mode (External strobe), Die	$I_{dd\_wu\_ext\_die}$			250	nA	Wake up strobe period=1.1s. Bias code=10. See Figure 1-5 on page 1-9
	Current, Sleep/Listen Mode (External strobe), QFN	$I_{dd\_wu\_ext\_qfn}$			650	nA	Wake up strobe period=1.1s. Bias code=10. See Figure 1-5 on page 1-9
31	Current, Sleep/Listen Mode (Internal strobe), Die	$I_{dd\_wu\_int\_die}$			650	nA	Wake up strobe period=1.1s. Bias code=10. See Figure 1-5 on page 1-9
	Current, Sleep/Listen Mode (Internal strobe), QFN	$I_{dd\_wu\_int\_qfn}$			1050	nA	Wake up strobe period=1.1s. Bias code=10. See Figure 1-5 on page 1-9

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Table 7-4 • **Performance Characteristics (continued)**
VSUP = 2.1V–3.5V and T = 0°C–55°C unless otherwise stated. The parameters tested in production with different limits, different conditions or not tested are indicated with *, **,* or ****. See also Notes 1 to 10 on page 7-9.**

	Parameter	Symbol	Min.	Typ. ****	Max.	Unit	Notes
32	Current, Wake Mode	I_{wake}			0.9	mA	Crystal oscillator and voltage regulator on. Digital voltage regulator min load off.
33	Current, TX Mode	I_{tx}			5.0	mA	PA power set to code 63 (max) into 500 Ω
34	Current, RX Mode	I_{rx}			5.0	mA	At maximum LNA gain
	Synthesizer						
35	Composite transmit phase noise @ Δf = 250 kHz	Φ_{synth_250k}		−110		dBc/ Hz	At mixer
36	Reference spurs	Ψ_{synth_clrs}			−45	dBc	At ± n×300 kHz
37	PLL Lock time	T_{synth_lock}		2		ms	To within 2 kHz
400 MHz Transmitter							
38	Tx load Impedance	R_{tx_load}		500		Ω	Real Part (typically 15+j85)
39	Frequency Separation (4FSK, 800 kbps)	MOD_{F4}	33	36	39	kHz	
40	Frequency Separation (2FSK, 400 kbps)	MOD_{F2_400}	77	80	83	kHz	
41	Frequency Separation (2FSK, 200 kbps)	MOD_{F2_200}	96	100	104	kHz	
42	Transmit Power	P_{TX}		−4.5		dBm	Programmable in 3 dB steps. Power code = 63 (max). Note 1
43	Unwanted emissions outside the 402–405 MHz band	$E_{outband}$		−42	−33	dBc	Compliant with FCC CFR47.95 free space.
44	Unwanted emissions within the 402–405 MHz band	E_{inband}		−22	−20	dBc	Compliant with FCC CFR47.95

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	Parameter	Symbol	Min.	Typ. ****	Max.	Unit	Notes
400 MHz Receiver							
45	RF amplifier and mixer gain *	G_{RX}	9	32	35	dB	Programmable In steps of 3 dB except from 15–23 dB
46	1 dB compression point referred to input *	ICP1	2.5	3		mV	at 32 dB gain, Note 2
47	Third-order input intercept point	IIP3		8		mV	at 32 dB gain,
48	RX Sensitivity (4FSK) *	P_{rx_4FSK}	120	80		μV_{rms}	$R_{(effective\ source)}$ = 1620Ω, Note 3
49	RX Sensitivity (2FSK-high rate) *	P_{rx_2FSKhr}	35	25		μV_{rms}	$R_{(effective\ source)}$ = 1620Ω, Note 3
50	RX Sensitivity (2FSK-high sensitivity) **	P_{rx_2FSKhs}	20	14		μV_{rms}	$R_{(effecitve\ source)}$ = 1620Ω, Note 3
2.45 GHz Receiver							
51	RX_245 sensitivity, Die *	P_{rx_245}		300		μV_{rms}	Operating temp range is 25°C to 55°C. Note 4
52	RX_245 rise time on pulse *	T_{wu_rise}			300	ns	To 90%
53	RX_245 fall time on pulse *	T_{wu_fall}			500	ns	To 10%
Crystal Oscillator							
54	Oscillator frequency	F_{xo_osc}		24		MHz	
55	Post-Trim Tolerance (Frequency Trim step) **	ΔF_{xo_post}			±10	ppm	Based on a pre-trim tolerance = ±60 ppm. See also Note 5
General Purpose ADC							
56	ADC conversion time	T_{con}		2.08		µs	$T_{con} = 8/24 \times N_{ADCr}$
57	ADC resolution	N_{ADCr}		5		bits	
58	Differential Nonlinearity	DNL_{ADC}			0.5	LSB	
59	Integral Nonlinearity	INL_{ADC}	−1		1	%FS	
60	Gain error	G_{ADCerr}	−2.5		2.5	%FS	at Full-scale

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	Parameter	Symbol	Min.	Typ. ****	Max.	Unit	Notes
61	Offset error	V_{ADCerr}	−1		1	LSB	
62	Input voltage range	V_{ADC}	0		1.25	V	
Internal RSSI							
63	Input voltage giving 00000_2 **	$V_{rx\_rssi\_min}$			5	μV_{RMS}	At LNA input, RSSI trimmed Note 6
64	Input voltage giving 11111_2 **	$V_{rx\_rssi\_max}$	4			mV_{RMS}	At LNA input, RSSI trimmed Note 7
65	Relative Step size	ΔV_{rx_rssi}	1	2	3	dB	
Matching Network							
66	Tuning Capacitor Range (400 MHz TX) **	$C_{tune400tx}$	2		7	pF	Bare die, 0.1pF step, Q-values in Figure 7-2 on page 7-10
67	Tuning Capacitor Range (400 MHz RX) **	$C_{tune400rx}$	2		7	pF	Bare die, 0.1pF step, Q-values in Figure 7-2 on page 7-10
68	Tuning Capacitor Range MATCH1 **	C_{tune_match1}	5		60	pF	Bare die, 0.4pF step, Q-values in Figure 7-3 on page 7-10
69	Tuning Capacitor Range MATCH2 **	C_{tune_match2}	5		60	pF	Bare die, 0.4pF step, Q-values in Figure 7-3 on page 7-10
70	Tuning Capacitor Range (2.45 GHz) **	$C_{tune245}$	0.3		2	pF	Bare die, 0.1pF step
71	Shunt Resistive Load presented to 400 MHz transmitter ***	R_{L400tx}	144	500		Ω	Note 8
72	Shunt Reactive Load presented to 400 MHz transmitter ***	X_{L400tx}	+j57	+j88	+j199	Ω	Note 9
73	Resistive Input Impedance 400 MHz receiver ***	R_{L400rx}	5000	20000		Ω	Note 10

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Table 7-4 • Performance Characteristics (continued)
VSUP = 2.1V–3.5V and T = 0°C–55°C unless otherwise stated. The parameters tested in production with different limits, different conditions or not tested are indicated with *, **,* or ****. See also Notes 1 to 10 on page 7-9.**

	Parameter	Symbol	Min.	Typ. ****	Max.	Unit	Notes
74	Reactive Input Impedance 400 MHz receiver ***	X_{L400rx}		−j500		Ω	Note 10
75	Resistive Input Impedance 2.45 GHz receiver ***	R_{L245rx}	2000			Ω	
76	Parallel Reactive Input Impedance 2.45 GHz receiver ***	X_{L245rx}	−j82			Ω	

Notes:

1. *Power output measured in a 50 Ohm load, using a device mounted in a Gryphics socket, part no. 101078-0020 in Microsemi Test Fixture 1645-17 which incorporates a matching network with a transfer efficiency of 44%.*
2. *The 1 dB compression point corresponds to −49 dBm into 500 Ohms.*
3. *The sensitivity is specified in μV_{rms} since the device input impedance is not 50 Ohms. The effective source impedance Reff = 1620 Ohms is used for dBm calculations. This value is derived from a source impedance Rs = 500 Ohms and a chip load impedance RI = 4500 Ohms. Please see the ZL70101 design manual for further details.*
4. *The sensitivity is specified in μV_{rms} since the device input impedance is not 50 Ohms. Design center value for a die mounted on a suitable substrate. Packaged devices will offer a worse sensitivity: This sensitivity is very dependant of substrate material and layout. Test omitted for device ZL70101LDG1A.*
5. *The pretrim tolerance is composed of 40 ppm for XTAL (initial, aging, temp), 10 ppm for series resistance variation and 10 ppm for other XO nonidealities. Based on the crystal type: Statek CX9SM. The total required XO tolerance is determined by the transmitter and receiver frequency alignment requirements. Analysis of the ZL70101 indicates that the total frequency misalignment should be limited to ±75 ppm.*
6. *The lower end of the RSSI range is set by the receiver noise. For the base unit this corresponds to roughly −174 (noise floor) + 58 (bandwidth) + 14 (NF) = −102 dBm (or 5 µV(rms) into 500 Ohms).*
7. *The upper limit of the RSSI range of interest is determined by the maximum input signal that can be handled and the required SNR. Limiting in the RF front-end occurs for input signals stronger than −45 dBm (or 4 mV(rms) into 500 Ohms). If the level is higher than that, the system is blocked.This means that the desired range of the RSSI is around 57dB.*
8. *The load requirement on the 400 MHz transmitter (R_{L400tx} and X_{L400tx}) largely determines the matching network design. The resistive load to the transmitter is determined by the required RF output power Po. This is derived from the required radiated power, less the antenna gain and matching circuit losses; expected typical values are provided. For the case of maximum available power, 3.9 dBm at 3.6 V battery (See PA specification in RF chapter), we can consider the maximum voltage swing of the PA and maximum available current (1.7 Vpp and 4.1 mA current(rms)) to derive a minimum load of 144 Ohms. An R_{L400tx} value of 500 Ohms will correspond to −3 dBm output power or 1.4 Vpp and 1 mA current(rms).*
9. *The reactive load is set to provide resonance. It should be the conjugate of the tuning capacitor reactance. That is, $X_{L400tx} = j/(\omega C_{tune400})$. The range of tuning may be restricted by parasitic capacitance and inductance in a packaged device.*
10. *The receiver input impedance is important for maximizing SNR. The optimum receiver source impedance for maximizing SNR is 500 Ohms or greater.*

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Typical Q of RX and TX tuning capacitors

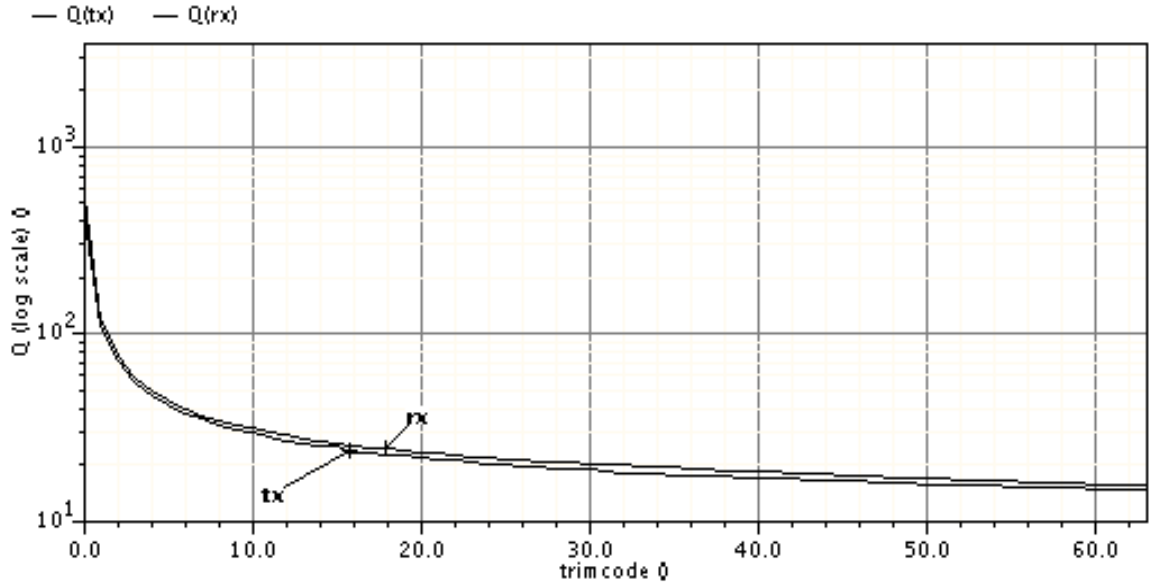

Figure 7-2 • **Q-values for TX and RX Tuning Capacitors**
Resistance in bondwires not taken into account; Log scale on Y-axis.

Typical Q of MATCH1 and MATCH2 tuning capacitors

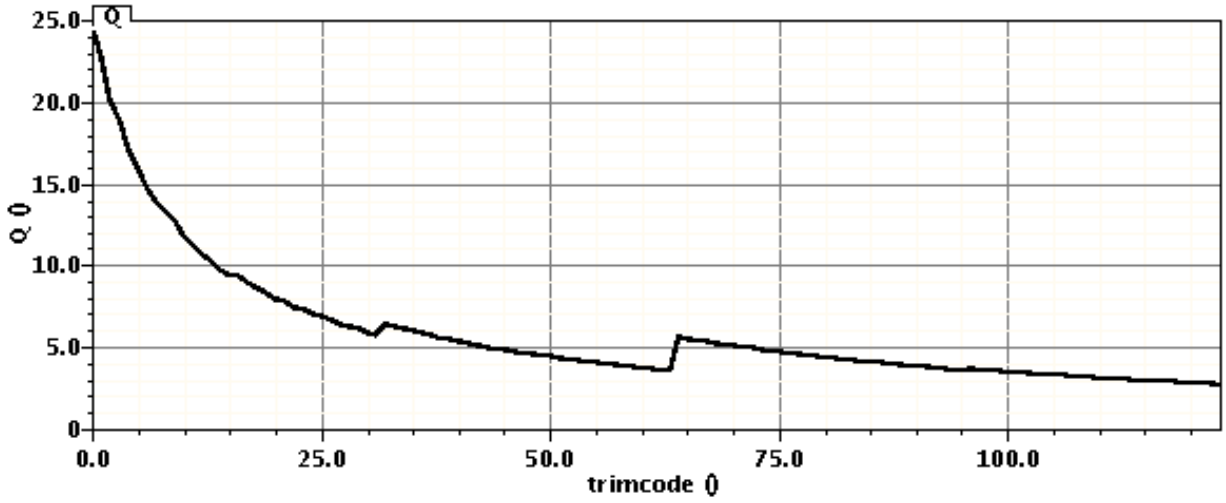

Figure 7-3 • **Q-values for MATCH1 and MATCH2 Tuning Capacitors**
Resistance in bondwires not taken into account.

8 – Quality

The ZL70101 can be delivered either as bare-dies (ZL70101UBJ) or in a QFN package (ZL70101LDG1A); please see the "Ordering Information" on page I for further details.

The bare-dies are intended for implantable applications. The QFN package is intended for base station applications and for nonimplantable applications. It is not approved for use in implantable products.

For all versions of the product, manufacturing processes are carried out in ISO9001 approved facilities and all products are fully tested and qualified to ensure conformance to this data sheet.

For the implantable products, the following additional stages are implemented among others:

- Enhanced Change Notification
  - A comprehensive system of change notification and approval is invoked. No major changes to the product will be made without notification to and/or approval from the customer.
- Wafer Lot Acceptance Testing
  - Each wafer lot is individually assessed to ensure that it is capable of meeting the stringent quality requirements for implantable applications using established quality acceptance requirements and test methods based upon MIL-STD-883 and MIL-PRF-38535.
- Die Acceptance Testing
  - Every die is individually tested at 37°C.
  - Every die is visually inspected.
- Enhanced Record Retention
  - Quality records are retained for the expected duration of production and use of end products.

9 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the datasheet.

Revision	Changes	Page
Revision 8 (May 2012)	Name change from Zarlink to Microsemi. Included changing document format and chapter structure. Spelling and grammar were also corrected throughout the document.	All

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Safety Critical, Life Support, and High-Reliability Applications Policy

The products described in an advance status document may not have completed the Microsemi qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the Microsemi CMPG Products Group Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the CMPG Products Group's products is available from Microsemi upon request. Microsemi also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local sales office for additional reliability information.

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