



***Z86E72/73***

***OTP Microcontroller***

**Product Specification**

PS008704-0507



**Warning:** DO NOT USE IN LIFE SUPPORT

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## Features

Table 1 lists some of the features of the Z86E72/73 microcontrollers.

**Table 1. Z86E72/73 Features**

| Part   | ROM (KB) | RAM* (Bytes) | I/O | Voltage Range  |
|--------|----------|--------------|-----|----------------|
| Z86E73 | 32       | 236          | 31  | 3.0 V to 5.5 V |
| Z86E72 | 16       | 748          | 31  | 3.0 V to 5.5 V |

**Note:** \*General-purpose

- Low power consumption—60 mW (typical)
- Two standby modes (typical)
  - STOP—2  $\mu$ A
  - HALT—0.8 mA
- Special architecture to automate both generation and reception of complex pulses or signals:
  - One programmable 8-bit counter/timer with two capture registers
  - One programmable 16-bit counter/timer with one capture register
  - Programmable input glitch filter for pulse reception
- Five priority interrupts
  - Three external
  - Two assigned to counter/timers
- Two independent comparators with programmable interrupt polarity
- On-chip oscillator that accepts a crystal, ceramic resonator, LC, RC (mask option), or external clock drive
- Software-selectable  $200 \pm 50\%$  K $\Omega$  resistive transistor pull-ups on Port 0 and Port 2
  - Port 2 pull-ups are bit selectable
  - Pull-ups automatically disabled as outputs
- Software mouse/trackball interface on P00 through P03

## General Description

The Z86E7X family are OTP-based members of the Z8<sup>®</sup> MCU single-chip family with 236 or 748 bytes of general-purpose RAM. The only differentiating factor between the E72/73 versions is the availability of RAM and ROM. This EPROM microcontroller family of OTP controllers also offers the use of external memory, which enables this Z8 microcontroller to be used where code flexibility is required. ZiLOG's CMOS microcontrollers offer fast execution, efficient use of memory, sophisticated interrupts, input/output bit manipulation capabilities, automated pulse generation/reception, and easy hardware/software system expansion along with cost-effective and low power consumption.

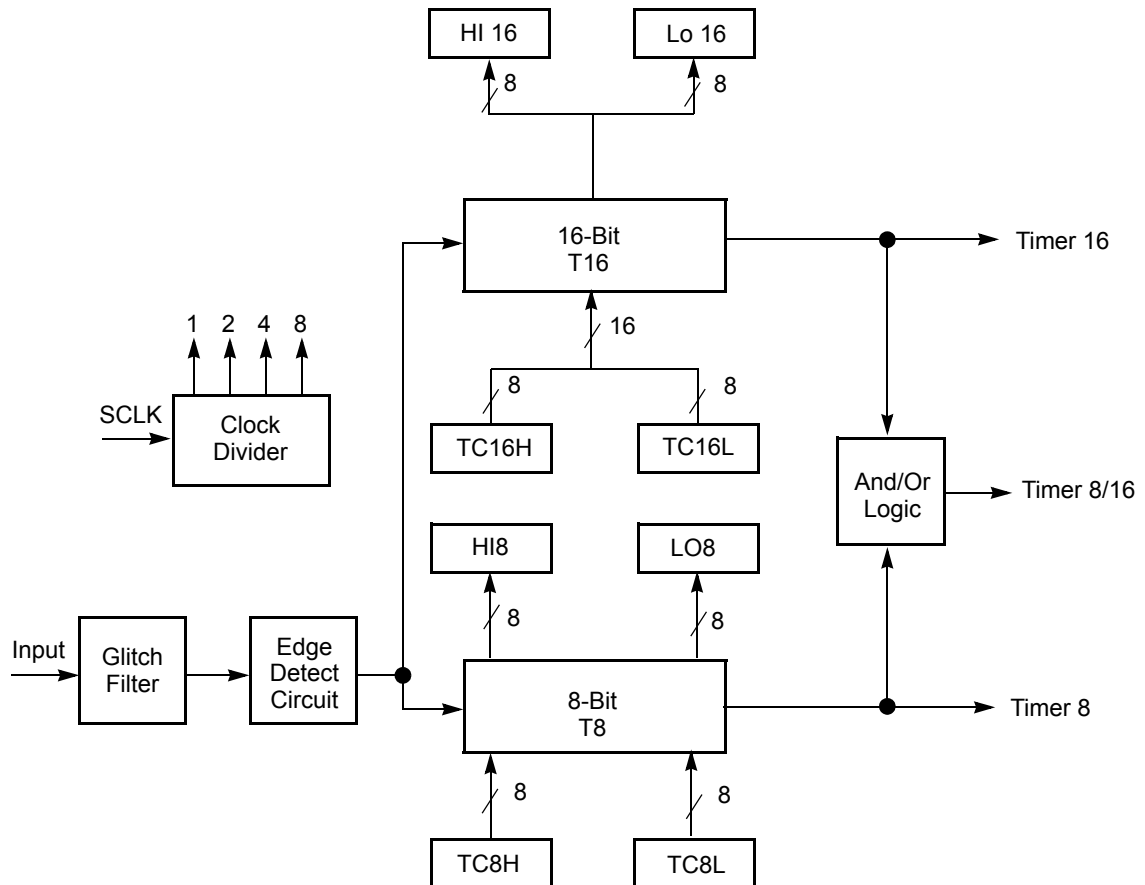
The Z86E7X architecture is based on ZiLOG's 8-bit microcontroller core with an Expanded Register File to allow access to register-mapped peripherals, I/O circuits, and powerful counter/timer circuitry. The Z8 offers a flexible I/O scheme, an efficient register and address space structure, and a number of ancillary features that are useful in many consumer, automotive, computer peripheral, and battery-operated hand-held applications.

Z8 applications demand powerful I/O capabilities. The Z86E7X family fulfills this with three package options in which the E72/73 versions provide 31 pins of dedicated input and output. These lines are grouped into four ports. Each port consists of eight lines (Port 3 has seven lines of I/O and one Pref comparator input) and is configurable under software control to provide timing, status signals, parallel I/O with or without handshake, and an address/data bus for interfacing external memory.

There are five basic address spaces available to support a wide range of configurations: program memory, register file, Expanded Register File, Extended Data RAM, and external memory. The register file is composed of 256 bytes of RAM. It includes 4 I/O port registers, 16 control and status registers, and the rest are general-purpose registers. The Extended Data RAM adds 512 (E72) of usable general-purpose registers. The Expanded Register File consists of two additional register groups (F and D).

To unburden the program from coping with such real-time problems as generating complex waveforms or receiving and demodulating complex waveform/pulses, the Z86E7X family offers a new intelligent counter/timer architecture with 8-bit and 16-bit counter/timers (Figure 1). Also included are a large number of user-selectable modes and two on-board comparators to process analog signals with separate reference voltages (Figure 19 on page 34).

► **Note:** All signals with a preceding front slash, “/”, are active Low. For example, B/W (WORD is active Low); /B/W (BYTE is active Low, only).



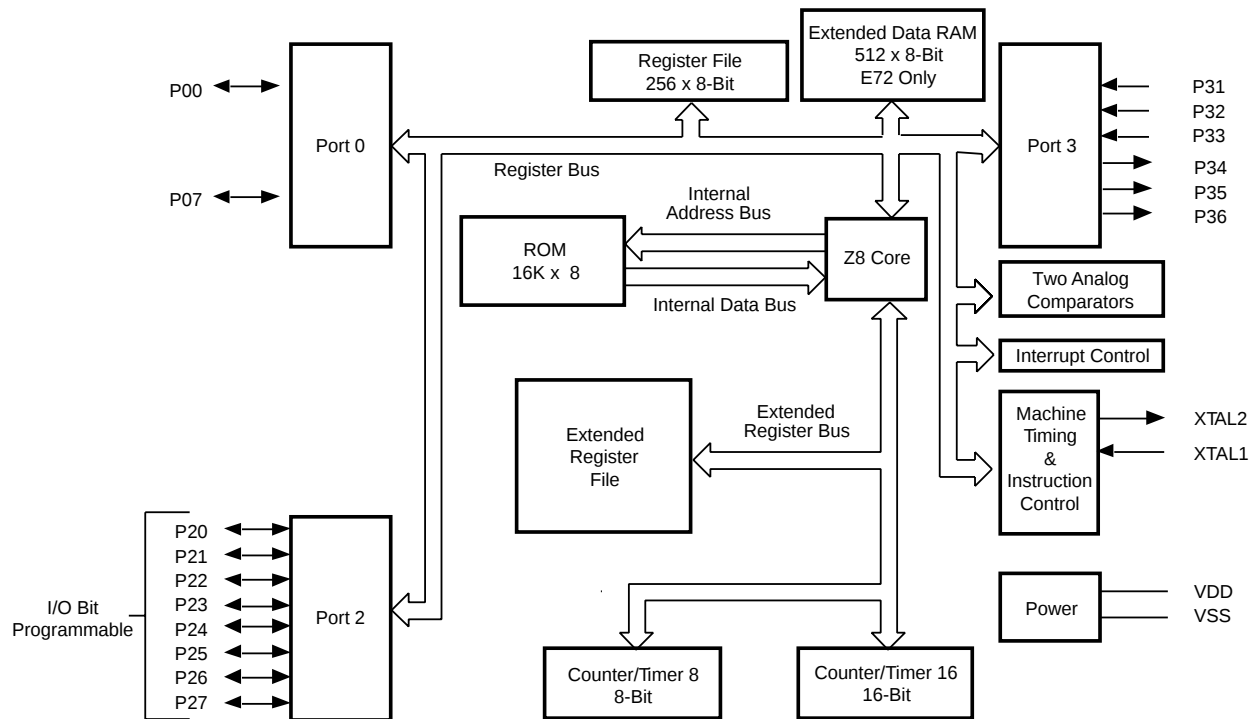
**Figure 1. Z86E7X Counter/Timer Block Diagram**

Power connections follow the conventions listed in [Table 2](#).

**Table 2. Power Connections**

| Connection | Circuit         | Device          |
|------------|-----------------|-----------------|
| Power      | V <sub>CC</sub> | V <sub>DD</sub> |
| Ground     | GND             | V <sub>SS</sub> |

[Figure 2](#) displays the functional block diagram.



**Figure 2. Z86E7X Functional Block Diagram**

## Pin Description

Figure 3 shows the pin assignments for the standard mode of the 40-pin dual in-line package (DIP). Figure 4 on page 6 shows the pin assignments for the electronically programmable read-only memory (EPROM) mode of the 40-pin DIP.

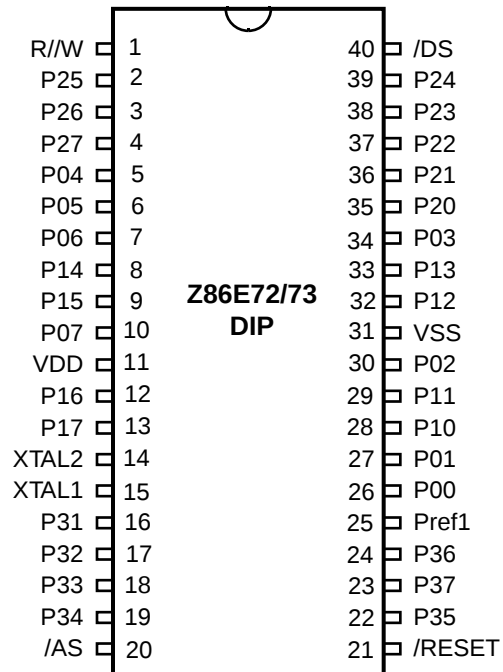
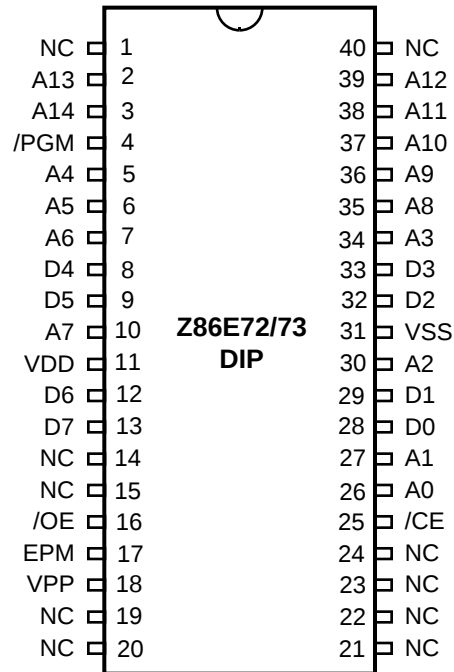
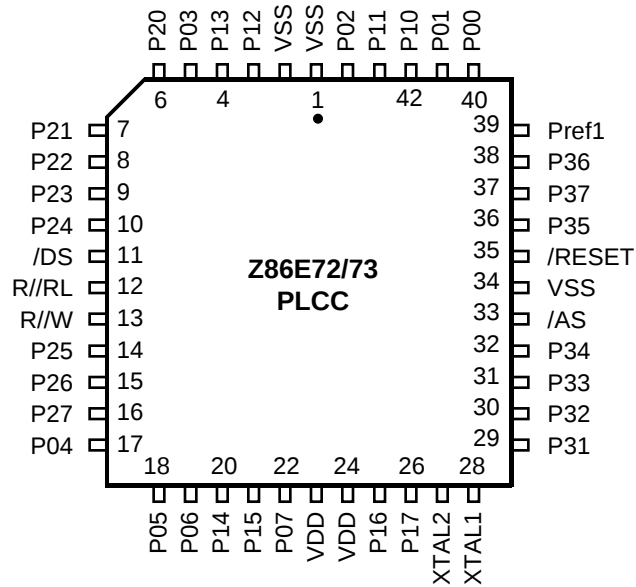


Figure 3. 40-Pin DIP Pin Assignments (Standard Mode)

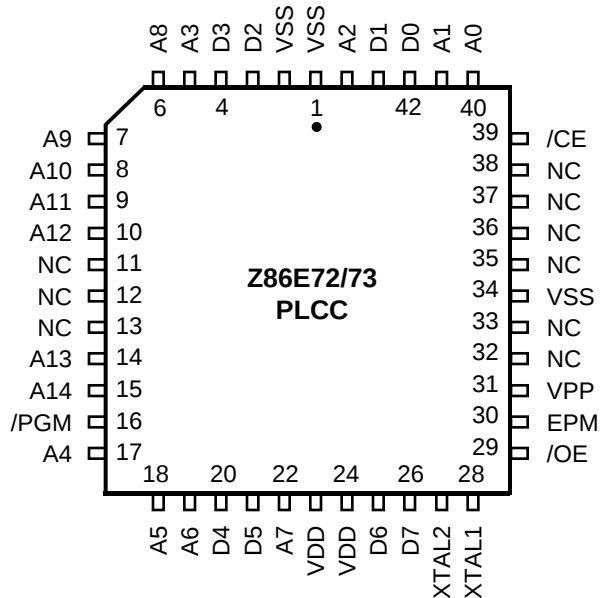


**Figure 4. 40-Pin DIP Pin Assignments (EPROM Mode)**

Figure 5 on page 7 shows the pin assignments for the standard mode of the 44-pin plastic leaded chip carrier (PLCC). Figure 6 on page 7 displays the pin assignments for the EPROM mode of the 44-pin PLCC.

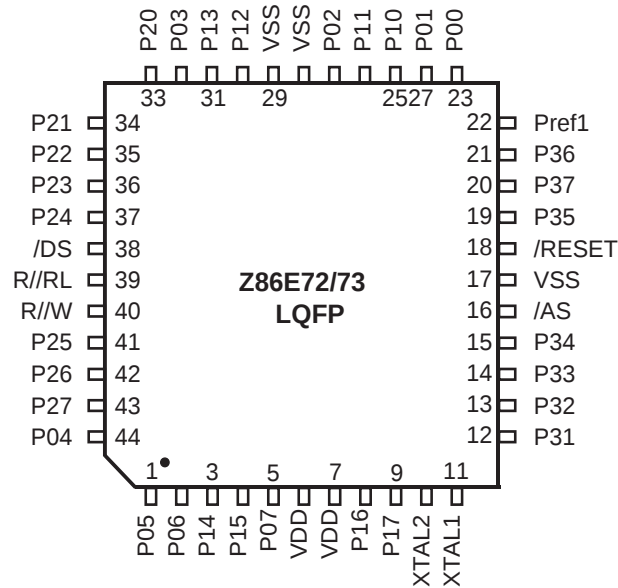


**Figure 5. 44-Pin PLCC Pin Assignments (Standard Mode)**

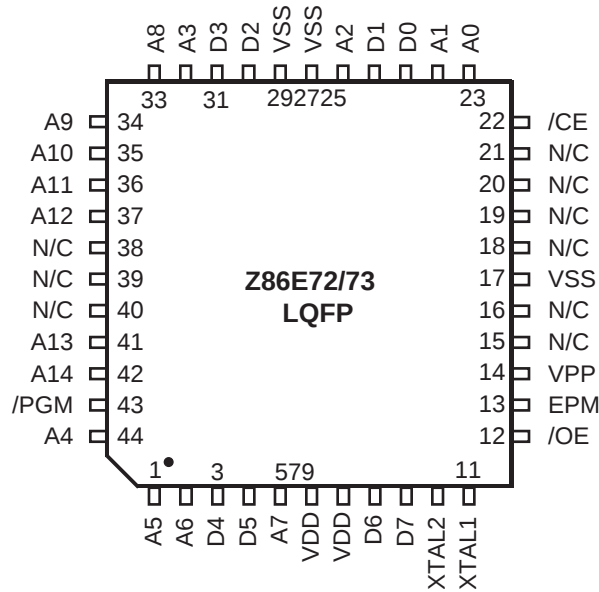


**Figure 6. 44-Pin PLCC Pin Assignments (EPROM Mode)**

Figure 7 displays the pin assignments for the standard mode of the 44-pin low-profile quad flat pack (LQFP). Figure 8 on page 9 shows the pin assignments for the EPROM mode of the 44-pin LQFP.



**Figure 7. 44-Pin LQFP Pin Assignments (Standard Mode)**



**Figure 8. 44-Pin LQFP Pin Assignments (EPROM Mode)**

Table 3 identifies the pins in packages in standard mode. Table 4 on page 11 identifies the pins in the 40-pin DIP in EPROM mode. Table 5 on page 12 identifies the pins in the 44-pin LQFP and PLCC.

**Table 3. Pin Identification (Standard Mode)**

| 40-Pin DIP # | 44-Pin PLCC # | 44-Pin LQFP # | Symbol | Direction    | Description                                         |
|--------------|---------------|---------------|--------|--------------|-----------------------------------------------------|
| 26           | 40            | 23            | P00    | Input/Output | Port 0 is Nibble Programmable.                      |
| 27           | 41            | 24            | P01    | Input/Output | Port 0 can be configured as A15–A8 external program |
| 30           | 44            | 27            | P02    | Input/Output |                                                     |
| 34           | 5             | 32            | P03    | Input/Output | ROM Address Bus.                                    |
| 5            | 17            | 44            | P04    | Input/Output | Port 0 can be configured as a                       |
| 6            | 18            | 1             | P05    | Input/Output | mouse/trackball input.                              |
| 7            | 19            | 2             | P06    | Input/Output |                                                     |
| 10           | 22            | 5             | P07    | Input/Output |                                                     |
| 28           | 42            | 25            | P10    | Input/Output | Port 1 is byte programmable.                        |



**Table 3. Pin Identification (Standard Mode) (Continued)**

| 40-Pin DIP # | 44-Pin PLCC # | 44-Pin LQFP # | Symbol | Direction    | Description                                                                               |
|--------------|---------------|---------------|--------|--------------|-------------------------------------------------------------------------------------------|
| 29           | 43            | 26            | P11    | Input/Output | Port 1 can be configured as multiplexed A7–A0/D7–D0 external program ROM Address/Data Bus |
| 32           | 3             | 30            | P12    | Input/Output |                                                                                           |
| 33           | 4             | 31            | P13    | Input/Output |                                                                                           |
| 8            | 20            | 3             | P14    | Input/Output |                                                                                           |
| 9            | 21            | 4             | P15    | Input/Output |                                                                                           |
| 12           | 25            | 8             | P16    | Input/Output |                                                                                           |
| 13           | 26            | 9             | P17    | Input/Output |                                                                                           |
| 35           | 6             | 33            | P20    | Input/Output | Port 2 pins are individually configurable as input or output                              |
| 36           | 7             | 34            | P21    | Input/Output |                                                                                           |
| 37           | 8             | 35            | P22    | Input/Output |                                                                                           |
| 38           | 9             | 36            | P23    | Input/Output |                                                                                           |
| 39           | 10            | 37            | P24    | Input/Output |                                                                                           |
| 2            | 14            | 41            | P25    | Input/Output |                                                                                           |
| 3            | 15            | 42            | P26    | Input/Output |                                                                                           |
| 4            | 16            | 43            | P27    | Input/Output |                                                                                           |
| 16           | 29            | 12            | P31    | Input        | IRQ2/Modulator input                                                                      |
| 17           | 30            | 13            | P32    | Input        | IRQ0                                                                                      |
| 18           | 31            | 14            | P33    | Input        | IRQ1                                                                                      |
| 19           | 32            | 15            | P34    | Output       | T8 output                                                                                 |
| 22           | 36            | 19            | P35    | Output       | T16 output                                                                                |
| 24           | 38            | 21            | P36    | Output       | T8/T16 output                                                                             |
| 23           | 37            | 20            | P37    | Output       |                                                                                           |
| 20           | 33            | 16            | /AS    | Output       | Address Strobe                                                                            |
| 40           | 11            | 38            | /DS    | Output       | Data Strobe                                                                               |
| 1            | 13            | 40            | R/W    | Output       | Read/Write                                                                                |
| 21           | 35            | 18            | /RESET | Input        | Reset                                                                                     |
| 15           | 28            | 11            | XTAL1  | Input        | Crystal, Oscillator Clock                                                                 |



**Table 3. Pin Identification (Standard Mode) (Continued)**

| 40-Pin DIP # | 44-Pin PLCC # | 44-Pin LQFP # | Symbol          | Direction | Description               |
|--------------|---------------|---------------|-----------------|-----------|---------------------------|
| 14           | 27            | 10            | XTAL2           | Output    | Crystal, Oscillator Clock |
| 11           | 23, 24        | 6, 7          | V <sub>DD</sub> |           | Power Supply              |
| 31           | 1, 2, 34      | 17, 28, 29    | V <sub>SS</sub> |           | Ground                    |
| 25           | 39            | 22            | Pref1           | Input     | Comparator 1 Reference    |
| NC           | 12            | 39            | R//RL           | Input     | ROM//ROMless              |

**Table 4. Z86E72/73 40-Pin DIP Identification—EPROM Mode**

| 40-Pin # | Symbol          | Function         | Direction    |
|----------|-----------------|------------------|--------------|
| 1        | N/C             | Not Connected    |              |
| 2–3      | A13–14          | Address 13, 14   | Input        |
| 4        | /PGM            | Program Mode     | Input        |
| 5–7      | A4–A6           | Address 4, 5, 6  | Input        |
| 8–9      | D4–D5           | Data 4, 5        | Input/Output |
| 10       | A7              | Address 7        | Input        |
| 11       | V <sub>DD</sub> | Power Supply     |              |
| 12–13    | D6–D7           | Data 6, 7        | Input/Output |
| 14–15    | N/C             | Not Connected    |              |
| 16       | /OE             | Output Enable    | Input        |
| 17       | EPM             | EPROM Prog. Mode | Input        |
| 18       | V <sub>PP</sub> | Prog. Voltage    | Input        |
| 19–24    | N/C             | Not Connected    |              |
| 25       | /CE             | Chip Enable      | Input        |
| 26–27    | A0–A1           | Address 0, 1     | Input        |
| 28–29    | D0–D1           | Data 0, 1        | Input/Output |
| 30       | A2              | Address 2        | Input        |
| 31       | V <sub>SS</sub> | Ground           |              |
| 32–33    | D2–D3           | Data 2, 3        | Input/Output |



**Table 4. Z86E72/73 40-Pin DIP Identification—EPROM Mode (Continued)**

| 40-Pin # | Symbol | Function                 | Direction |
|----------|--------|--------------------------|-----------|
| 34       | A3     | Address 3                | Input     |
| 35–39    | A8–A12 | Address 8, 9, 10, 11, 12 | Input     |
| 40       | N/C    | Not Connected            |           |

**Table 5. Z86E72/73 44-Pin LQFP/PLCC Pin Identification—EPROM Mode**

| 44-Pin LQFP | 44-Pin PLCC | Symbol          | Function                 | Direction    |
|-------------|-------------|-----------------|--------------------------|--------------|
| 1–2         | 18–19       | A5–A6           | Address 5, 6             | Input        |
| 3–4         | 20–21       | D4–D5           | Data 4, 5                | Input/Output |
| 5           | 22          | A7              | Address 7                | Input        |
| 6–7         | 23–24       | V <sub>DD</sub> | Power Supply             |              |
| 8–9         | 25–26       | D6–D7           | Data 6, 7                | Input/Output |
| 10          | 27          | XTAL2           | Crystal Oscillator Clock |              |
| 11          | 28          | XTAL1           | Crystal Oscillator Clock |              |
| 12          | 29          | /OE             | Output Enable            | Input        |
| 13          | 30          | EPM             | EPROM Prog. Mode         | Input        |
| 14          | 31          | V <sub>PP</sub> | Prog. Voltage            | Input        |
| 15–16       | 32–33       | N/C             | Not Connected            |              |
| 17          | 34          | V <sub>SS</sub> | Ground                   |              |
| 18–21       | 35–38       | N/C             | Not Connected            |              |
| 22          | 39          | /CE             | Chip Select              | Input        |
| 23–24       | 40–41       | A0–A1           | Address 0, 1             | Input        |
| 25–26       | 42–43       | D0–D1           | Data 0, 1                | Input/Output |
| 27          | 44          | A2              | Address 2                | Input        |
| 28–29       | 1–2         | V <sub>SS</sub> | Ground                   |              |
| 30–31       | 3–4         | D2–D3           | Data 2, 3                | Input/Output |
| 32          | 5           | A3              | Address 3                | Input        |
| 33–37       | 6–10        | A8–A12          | Address 8, 9, 10, 11, 12 | Input        |
| 38–40       | 11–13       | N/C             | Not Connected            |              |

**Table 5. Z86E72/73 44-Pin LQFP/PLCC Pin Identification—EPROM Mode**

| 44-Pin LQFP | 44-Pin PLCC | Symbol  | Function       | Direction |
|-------------|-------------|---------|----------------|-----------|
| 41–42       | 14–15       | A13–A14 | Address 13, 14 | Input     |
| 43          | 16          | /PGM    | Prog. Mode     | Input     |
| 44          | 17          | A4      | Address 4      | Input     |

## Absolute Maximum Ratings

Table 6 lists the absolute maximum ratings for the Z86E72/73 microcontrollers.

**Table 6. Absolute Maximum Ratings**

| Symbol    | Description               | Min  | Max   | Units |
|-----------|---------------------------|------|-------|-------|
| $V_{MAX}$ | Supply Voltage (*)        | –0.3 | +7.0  | V     |
| $T_{STG}$ | Storage Temperature       | –65° | +150° | C     |
| $T_A$     | Oper. Ambient Temperature |      | †     | C     |

**Notes:**

\* Voltage on all pins with respect to GND.

† See “Ordering Information” on page 97.

Stresses greater than those listed under Absolute Maximum Ratings might cause permanent damage to the device. This rating is a stress rating only. Operation of the device at any condition above those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for an extended period might affect device reliability.

## Standard Test Conditions

The characteristics listed below apply for standard test conditions as noted. All voltages are referenced to GND. Positive current flows into the referenced pin (see [Figure 9](#)).

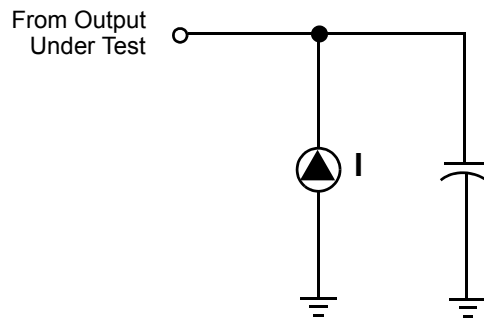


Figure 9. Test Load Diagram

## Capacitance

[Table 7](#) lists the capacitances for the Z86E72/73 microcontrollers.

Table 7. Capacitance

| Parameter                                                                                                                               | Max   |
|-----------------------------------------------------------------------------------------------------------------------------------------|-------|
| Input capacitance                                                                                                                       | 12 pF |
| Output capacitance                                                                                                                      | 12 pF |
| I/O capacitance                                                                                                                         | 12 pF |
| Note: $T_A = 25\text{ }^{\circ}\text{C}$ , $V_{CC} = \text{GND} = 0\text{ V}$ , $f = 1.0\text{ MHz}$ , unmeasured pins returned to GND. |       |

## DC Characteristics

Table 8 lists the direct current (DC) characteristics.

**Table 8. DC Characteristics**

| Sym.                | Parameter                                   | V <sub>CC</sub> | T <sub>A</sub> = 0 °C to +70 °C |                       | Typical<br>@ 25°C   | Units | Conditions                             |
|---------------------|---------------------------------------------|-----------------|---------------------------------|-----------------------|---------------------|-------|----------------------------------------|
|                     |                                             |                 | Min                             | Max                   |                     |       |                                        |
|                     | Max Input Voltage                           | 3.0 V           |                                 | 7                     |                     | V     | I <sub>IN</sub> 250 μA                 |
|                     |                                             | 5.5 V           |                                 | 7                     |                     | V     | I <sub>IN</sub> 250 μA                 |
| V <sub>CH</sub>     | Clock Input<br>High Voltage                 | 3.0 V           | 0.9 V <sub>CC</sub>             | V <sub>CC</sub> + 0.3 |                     | V     | Driven by External                     |
|                     |                                             | 5.5 V           | 0.9 V <sub>CC</sub>             | V <sub>CC</sub> + 0.3 |                     | V     | Clock Generator                        |
| V <sub>CL</sub>     | Clock Input<br>Low Voltage                  | 3.0 V           | V <sub>SS</sub> - 0.3           | 0.2 V <sub>CC</sub>   |                     | V     | Driven by External                     |
|                     |                                             | 5.5 V           | V <sub>SS</sub> - 0.3           | 0.2 V <sub>CC</sub>   |                     | V     | Clock Generator                        |
| V <sub>IH</sub>     | Input High Voltage                          | 3.0 V           | 0.7 V <sub>CC</sub>             | V <sub>CC</sub> + 0.3 | 0.5 V <sub>CC</sub> | V     |                                        |
|                     |                                             | 5.5 V           | 0.7 V <sub>CC</sub>             | V <sub>CC</sub> + 0.3 | 0.5 V <sub>CC</sub> | V     |                                        |
| V <sub>IL</sub>     | Input Low Voltage                           | 3.0 V           | V <sub>SS</sub> - 0.3           | 0.2 V <sub>CC</sub>   | 0.5 V <sub>CC</sub> | V     |                                        |
|                     |                                             | 5.5 V           | V <sub>SS</sub> - 0.3           | 0.2 V <sub>CC</sub>   | 0.5 V <sub>CC</sub> | V     |                                        |
| V <sub>OH1</sub>    | Output High Voltage                         | 3.0 V           | V <sub>CC</sub> - 0.4           |                       | 2.9                 | V     | I <sub>OH</sub> = -0.5 mA              |
|                     |                                             | 5.5 V           | V <sub>CC</sub> - 0.4           |                       | 5.4                 | V     | I <sub>OH</sub> = -0.5 mA              |
| V <sub>OH2</sub>    | Output High Voltage<br>(P00, P01, P36, P37) | 3.0 V           | V <sub>CC</sub> 0.7             |                       |                     | V     | I <sub>OH</sub> = -7 mA                |
|                     |                                             | 5.5 V           | V <sub>CC</sub> 0.7             |                       |                     | V     | I <sub>OH</sub> = -7 mA                |
| V <sub>OL1</sub>    | Output Low Voltage                          | 3.0 V           |                                 | 0.4                   | 0.1                 | V     | I <sub>OL</sub> = 1.0 mA               |
|                     |                                             | 5.5 V           |                                 | 0.4                   | 0.2                 | V     | I <sub>OL</sub> = 4.0 mA               |
| V <sub>OL2*</sub>   | Output Low Voltage                          | 3.0 V           |                                 | 0.8                   | 0.5                 | V     | I <sub>OL</sub> = 5.0 mA               |
|                     |                                             | 5.5 V           |                                 | 0.8                   | 0.3                 | V     | I <sub>OL</sub> = 7.0 mA               |
| V <sub>OL2</sub>    | Output Low Voltage<br>(P00, P01, P36, P37)  | 3.0 V           |                                 | 0.8                   | 0.3                 | V     | I <sub>OL</sub> = 10 mA                |
|                     |                                             | 5.5 V           |                                 | 0.8                   | 0.2                 | V     | I <sub>OL</sub> = 10 mA                |
| V <sub>RH</sub>     | Reset Input<br>High Voltage                 | 3.0 V           | 0.8 V <sub>CC</sub>             | V <sub>CC</sub>       | 1.5                 | V     |                                        |
|                     |                                             | 5.5 V           | 0.8 V <sub>CC</sub>             | V <sub>CC</sub>       | 2.5                 | V     |                                        |
| V <sub>RI</sub>     | Reset Input<br>Low Voltage                  | 3.0 V           | V <sub>SS</sub> - 0.3           | 0.2 V <sub>CC</sub>   | 0.9                 |       |                                        |
|                     |                                             | 5.5 V           | V <sub>SS</sub> - 0.3           | 0.2 V <sub>CC</sub>   | 1.8                 |       |                                        |
| V <sub>OFFSET</sub> | Comparator Input<br>Offset Voltage          | 3.0 V           |                                 | 25                    | 10                  | mV    |                                        |
|                     |                                             | 5.5 V           |                                 | 25                    | 10                  | mV    |                                        |
| I <sub>IL</sub>     | Input Leakage                               | 3.0 V           | -1                              | 1                     | < 1                 | μA    | V <sub>IN</sub> = 0 V, V <sub>CC</sub> |
|                     |                                             | 5.5 V           | -1                              | 1                     | < 1                 | μA    | V <sub>IN</sub> = 0 V, V <sub>CC</sub> |
| I <sub>OL</sub>     | Output Leakage                              | 3.0 V           | -1                              | 1                     | < 1                 | μA    | V <sub>IN</sub> = 0 V, V <sub>CC</sub> |
|                     |                                             | 5.5 V           | -1                              | 1                     | < 1                 | μA    | V <sub>IN</sub> = 0 V, V <sub>CC</sub> |

**Table 8. DC Characteristics (Continued)**

| Sym.             | Parameter                          | V <sub>CC</sub> | T <sub>A</sub> = 0 °C to +70 °C |                        | Typical<br>@ 25°C | Units | Conditions                                                                                    |
|------------------|------------------------------------|-----------------|---------------------------------|------------------------|-------------------|-------|-----------------------------------------------------------------------------------------------|
|                  |                                    |                 | Min                             | Max                    |                   |       |                                                                                               |
| I <sub>IR</sub>  | Reset Input Current                | 3.0 V           |                                 | –230                   | –50               | μA    |                                                                                               |
|                  |                                    | 5.5 V           |                                 | –400                   | –80               | μA    |                                                                                               |
| I <sub>CC</sub>  | Supply Current<br>(WDT off)        | 3.0 V           |                                 | 10                     | 4                 | mA    | @ 8.0 MHz                                                                                     |
|                  |                                    | 5.5 V           |                                 | 15                     | 10                | mA    | @ 8.0 MHz                                                                                     |
| I <sub>CC1</sub> | Standby Current<br>(WDT Off)       | 3.0 V           |                                 | 3                      | 1                 | mA    | HALT Mode<br>V <sub>IN</sub> = 0 V,<br>V <sub>CC</sub> at 8.0 MHz,<br>Notes 1, 2              |
|                  |                                    | 5.5 V           |                                 | 5                      | 4                 | mA    | HALT Mode<br>V <sub>IN</sub> = 0 V, V <sub>CC</sub><br>@ 8.0 MHz,<br>Notes 1, 2               |
|                  |                                    | 3.0 V           |                                 | 2                      | 0.8               | mA    | Clock Divide-by-16<br>@ 8.0 MHz<br>Notes 1, 2                                                 |
|                  |                                    | 5.5 V           |                                 | 4                      | 2.5               | mA    | Clock Divide-by-16<br>@ 8.0 MHz<br>Notes 1, 2                                                 |
| I <sub>CC2</sub> | Standby Current                    | 3.0 V           |                                 | 8                      | 2                 | μA    | STOP Mode<br>V <sub>IN</sub> = 0 V, V <sub>CC</sub><br>WDT is not<br>Running<br>Notes 3, 5, 9 |
|                  |                                    | 5.5 V           |                                 | 10                     | 3                 | μA    | STOP Mode<br>V <sub>IN</sub> = 0 V, V <sub>CC</sub><br>WDT is not<br>Running<br>Notes 3, 5, 9 |
|                  |                                    | 3.0 V           |                                 | 500                    | 310               | μA    | STOP Mode<br>Notes 3, 5                                                                       |
|                  |                                    | 5.5 V           |                                 | 800                    | 600               | μA    | V <sub>IN</sub> = 0 V, V <sub>CC</sub><br>WDT is Running                                      |
| V <sub>ICR</sub> | Input Common<br>Mode Voltage Range | 3.0 V           | 0                               | V <sub>CC</sub> –1.0 V | V                 |       | Note 8                                                                                        |
|                  |                                    | 5.5 V           | 0                               | V <sub>CC</sub> –1.0 V | V                 |       |                                                                                               |
| V <sub>LV</sub>  | VCC Low-Voltage<br>Detection       |                 |                                 | 2.9 V                  | 2.55 V            |       | Note 6                                                                                        |
| T <sub>POR</sub> | Power-On Reset                     | 3.0 V           | 12                              | 75                     | 18                | ms    |                                                                                               |
|                  |                                    | 5.5 V           | 5                               | 20                     | 7                 | ms    |                                                                                               |



**Table 8. DC Characteristics (Continued)**

| Sym.             | Parameter                         | V <sub>CC</sub>  | T <sub>A</sub> = 0 °C to +70 °C |             | Typical<br>@ 25°C | Units | Conditions                                           |
|------------------|-----------------------------------|------------------|---------------------------------|-------------|-------------------|-------|------------------------------------------------------|
|                  |                                   |                  | Min                             | Max         |                   |       |                                                      |
| V <sub>RAM</sub> | Static RAM Data Retention Voltage | V <sub>ram</sub> |                                 |             | 0.5               | V     | Worst case 0.8 V guaranteed by design only<br>Note 6 |
| <b>Notes:</b>    |                                   |                  |                                 |             |                   |       |                                                      |
|                  | <b>ICC1</b>                       | <b>Typ</b>       | <b>Max</b>                      | <b>Unit</b> | <b>Frequency</b>  |       |                                                      |
|                  | Crystal/Resonator                 | 3.0 mA           | 5                               | mA          | 8.0 MHz           |       |                                                      |
|                  | External Clock Drive              | 0.3 mA           | 5                               | mA          | 8.0 MHz           |       |                                                      |

1. All outputs unloaded, inputs at rail
  2. CL1 = CL2 = 100 pF
  3. Same as note [4] except inputs at V<sub>CC</sub>
  4. The V<sub>LV</sub> increases as the temperature decreases.
  5. Oscillator stopped
  6. Oscillator does not stop when V<sub>CC</sub> falls below V<sub>LV</sub> threshold.
  7. 32 kHz clock driver input
  8. For analog comparator, inputs when analog comparators are enabled
  9. WDT, Comparators, Low Voltage Detection, and ADC (if applicable) are disabled. The IC might draw more current if any of the above peripherals is enabled.
- \* All outputs excluding P00, P01, P36, and P37

## AC Characteristics

Figure 10 shows the external input/output (I/O) or memory read and write timing.  
Table 9 describes the I/O or memory read and write timing.

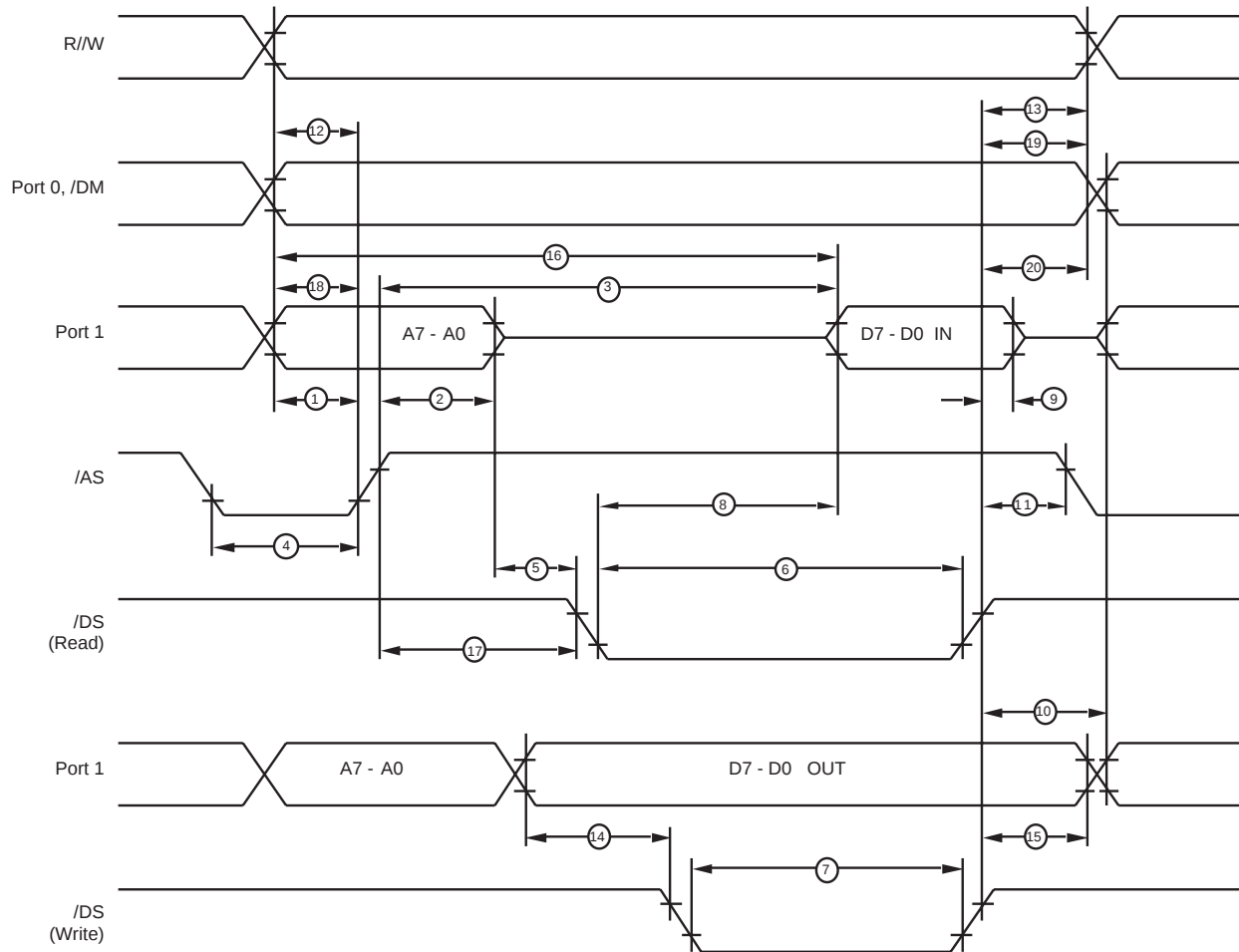


Figure 10. External I/O or Memory Read/Write Timing

**Table 9. External I/O or Memory Read and Write Timing**

| T <sub>A</sub> = 0 °C to +70 °C<br>16 MHz |           |                                               |                 |            |            |                       |
|-------------------------------------------|-----------|-----------------------------------------------|-----------------|------------|------------|-----------------------|
| No.                                       | Symbol    | Parameter                                     | V <sub>CC</sub> | Min.       | Max.       | Units Notes           |
| 1                                         | TdA(AS)   | Address Valid to /AS Rising Delay             | 3.0 V<br>5.5 V  | 55<br>55   |            | ns<br>ns 2            |
| 2                                         | TdAS(A)   | /AS Rising to Address Float Delay             | 3.0 V<br>5.5 V  | 70<br>70   |            | ns<br>ns 2            |
| 3                                         | TdAS(DR)  | /AS Rising to Read Data Required Valid        | 3.0 V<br>5.5 V  |            | 400<br>400 | ns<br>ns 1, 2<br>1, 2 |
| 4                                         | TwAS      | /AS Low Width                                 | 3.0 V<br>5.5 V  | 80<br>80   |            | ns<br>ns 2<br>2       |
| 5                                         | Td        | Address Float to /DS Falling                  | 3.0 V<br>5.5 V  | 0<br>0     |            | ns<br>ns              |
| 6                                         | TwDSR     | /DS (Read) Low Width                          | 3.0 V<br>5.5 V  | 300<br>300 |            | ns<br>ns 1, 2         |
| 7                                         | TwDSW     | /DS (Write) Low Width                         | 3.0 V<br>5.5 V  | 165<br>165 |            | ns<br>ns 1, 2         |
| 8                                         | TdDSR(DR) | /DS Falling to Read Data Required Valid       | 3.0 V<br>5.5 V  |            | 260<br>260 | ns<br>ns 1, 2         |
| 9                                         | ThDR(DS)  | Read Data to /DS Rising Hold Time             | 3.0 V<br>5.5 V  | 0<br>0     |            | ns<br>ns              |
| 10                                        | TdDS(A)   | /DS Rising to Address Active Delay            | 3.0 V<br>5.5 V  | 85<br>95   |            | ns<br>ns 2            |
| 11                                        | TdDS(AS)  | /DS Rising to /AS Falling Delay               | 3.0 V<br>5.5 V  | 60<br>70   |            | ns<br>ns 2            |
| 12                                        | TdR/W(AS) | R/W Valid to /AS Rising Delay                 | 3.0 V<br>5.5 V  | 70<br>70   |            | ns<br>ns 2            |
| 13                                        | TdDS(R/W) | /DS Rising to R/W Not Valid                   | 3.0 V<br>5.5 V  | 70<br>70   |            | ns<br>ns 2            |
| 14                                        | TdDW(DSW) | Write Data Valid to /DS Falling (Write) Delay | 3.0 V<br>5.5 V  | 80<br>80   |            | ns<br>ns 2            |
| 15                                        | TdDS(DW)  | /DS Rising to Write Data Not Valid Delay      | 3.0 V<br>5.5 V  | 70<br>80   |            | ns<br>ns 2            |
| 16                                        | TdA(DR)   | Address Valid to Read Data Required Valid     | 3.0 V<br>5.5 V  |            | 475<br>475 | ns<br>ns 1, 2         |

**Table 9. External I/O or Memory Read and Write Timing (Continued)**

| $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$<br>16 MHz |          |                                     |          |      |      |             |
|----------------------------------------------------------------------------|----------|-------------------------------------|----------|------|------|-------------|
| No.                                                                        | Symbol   | Parameter                           | $V_{CC}$ | Min. | Max. | Units Notes |
| 17                                                                         | TdAS(DS) | /AS Rising to                       | 3.0 V    | 100  |      | ns 2        |
|                                                                            |          | /DS Falling Delay                   | 5.5 V    | 100  |      | ns 2        |
| 18                                                                         | TdDM(AS) | /DM Valid to /AS                    | 3.0 V    | 55   |      | ns 2        |
|                                                                            |          | Falling Delay                       | 5.5 V    | 55   |      | ns          |
| 19                                                                         | TdDS(DM) | /DS Rise to                         | 3.0 V    | 70   |      | ns          |
|                                                                            |          | /DM Valid Delay                     | 5.5 V    | 70   |      | ns          |
| 20                                                                         | ThDS(A)  | /DS Rise to Address Valid Hold Time | 3.0 V    | 70   |      | ns          |
|                                                                            |          |                                     | 5.5 V    | 70   |      | ns          |

**Notes:**

1. When using extended memory timing, add 2 TpC.

2. Timing numbers given are for minimum TpC.

Standard Test Load

All timing references use 0.9  $V_{CC}$  for a logic 1 and 0.1  $V_{CC}$  for a logic 0.

Figure 11 shows additional timing. Table 10 describes the additional timing.

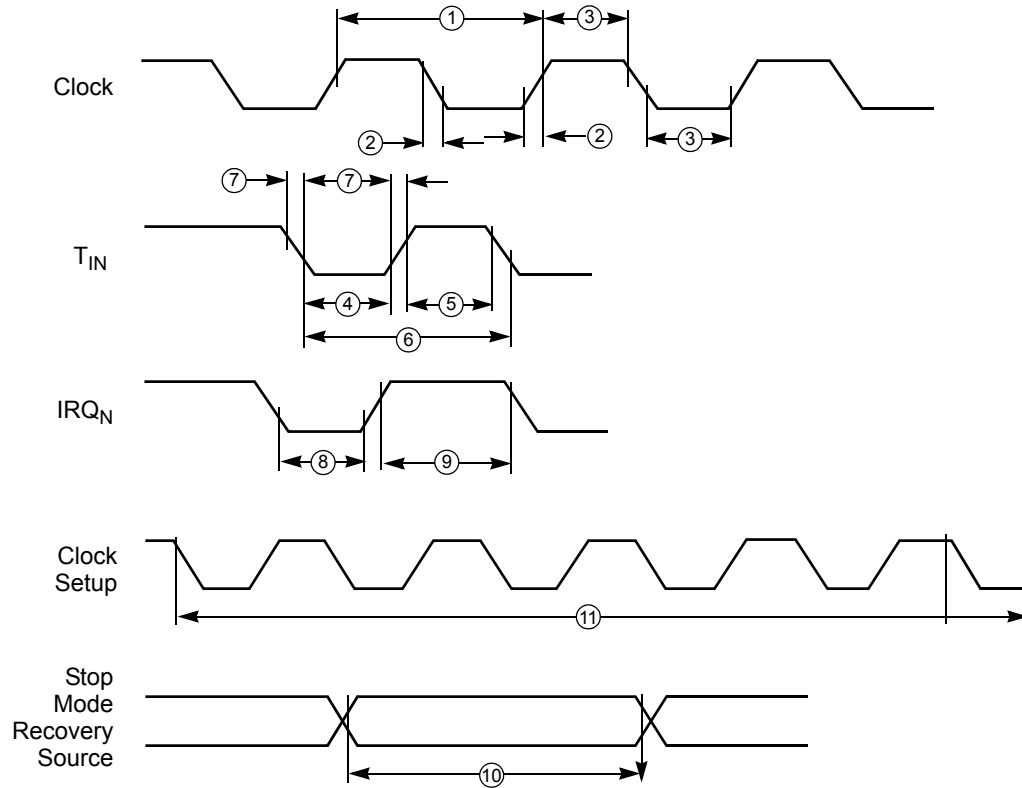


Figure 11. Additional Timing

Table 10. Additional Timing

| $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ |          |                                 |          |      |     |       |       |
|---------------------------------------------------|----------|---------------------------------|----------|------|-----|-------|-------|
| No                                                | Symbol   | Parameter                       | $V_{CC}$ | Min  | Max | Units | Notes |
| 1                                                 | TpC      | Input Clock Period              | 3.0 V    | 121  | DC  | ns    | 1     |
|                                                   |          |                                 | 5.5 V    | 121  | DC  | ns    | 1     |
| 2                                                 | TrC, TfC | Clock Input Rise and Fall Times | 3.0 V    |      | 25  | ns    | 1     |
|                                                   |          |                                 | 5.5 V    |      | 25  | ns    | 1     |
| 3                                                 | TwC      | Input Clock Width               | 3.0 V    | 37   |     | ns    | 1     |
|                                                   |          |                                 | 5.5 V    | 37   |     | ns    | 1     |
| 4                                                 | TwTinL   | Timer Input Low Width           | 3.0 V    | 100  |     | ns    | 1     |
|                                                   |          |                                 | 5.5 V    | 70   |     | ns    | 1     |
| 5                                                 | TwTinH   | Timer Input High Width          | 3.0 V    | 3TpC |     |       | 1     |
|                                                   |          |                                 | 5.5 V    | 3TpC |     |       | 1     |

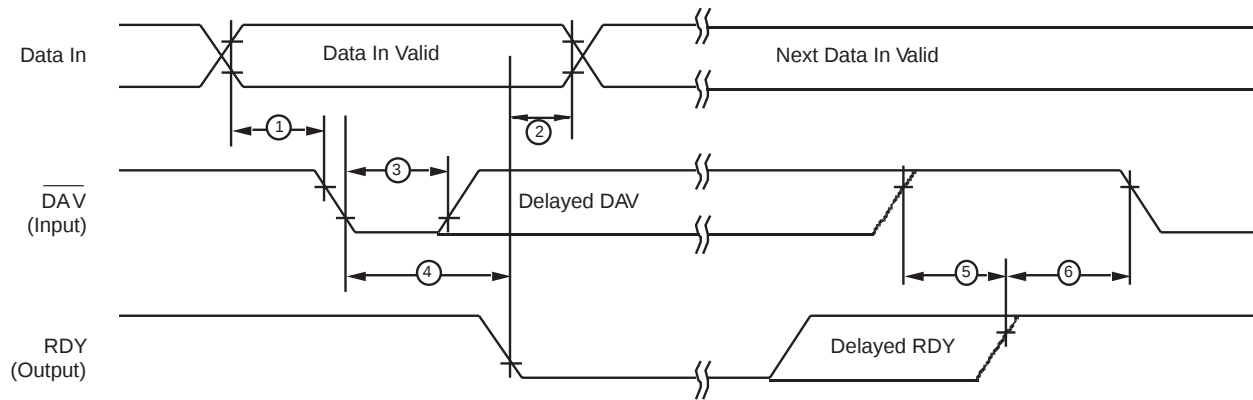
**Table 10. Additional Timing (Continued)**

| $T_A = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ |            |                                      |                                  |                          |              |          |                  |
|---------------------------------------------------|------------|--------------------------------------|----------------------------------|--------------------------|--------------|----------|------------------|
| No                                                | Symbol     | Parameter                            | $V_{CC}$                         | Min                      | Max          | Units    | Notes            |
| 6                                                 | TpTi       | Timer Input Period                   | 3.0 V<br>5.5 V                   | 8TpC<br>8TpC             |              |          | 1                |
| 7                                                 | TrTin,TfTi | Timer Input Rise and Fall Timers     | 3.0 V<br>5.5 V                   | 100<br>70                |              | ns<br>ns | 1<br>1           |
| 8A                                                | TwIL       | Interrupt Request Low Time           | 3.0 V<br>5.5 V                   | 100<br>70                |              | ns<br>ns | 1, 2<br>1, 2     |
| 8B                                                | TwIL       | Int. Request Low Time                | 4.5 V<br>5.5 V                   | 3TpC<br>5TpC             |              |          | 1, 3<br>1, 3     |
| 9                                                 | TwIH       | Interrupt Request Input High Time    | 4.5 V<br>5.5 V                   | 5TpC<br>5TpC             |              |          | 1, 2<br>1, 2     |
| 10                                                | Twsm       | Stop-Mode Recovery Width Spec        | 3.0 V<br>5.5 V<br>3.0 V<br>5.5 V | 12<br>12<br>5TpC<br>5TpC |              | ns<br>ns | 7<br>7<br>6<br>6 |
| 11                                                | Tost       | Oscillator Start-up Time             | 3.0 V<br>5.5 V                   |                          | 5TpC<br>5TpC |          | 4                |
| 12                                                | Twdt       | Watch-Dog Timer Delay Time<br>(5 ms) | 3.0 V<br>5.5 V                   | 12<br>5                  | 75<br>20     | ms<br>ms |                  |
|                                                   |            | (10 ms)                              | 3.0 V<br>5.5 V                   | 25<br>10                 | 150<br>40    | ms<br>ms |                  |
|                                                   |            | (20 ms)                              | 3.0 V<br>5.5 V                   | 50<br>20                 | 300<br>80    | ms<br>ms |                  |
|                                                   |            | (80 ms)                              | 3.0 V<br>5.5 V                   | 225<br>80                | 1200<br>320  | ms<br>ms |                  |

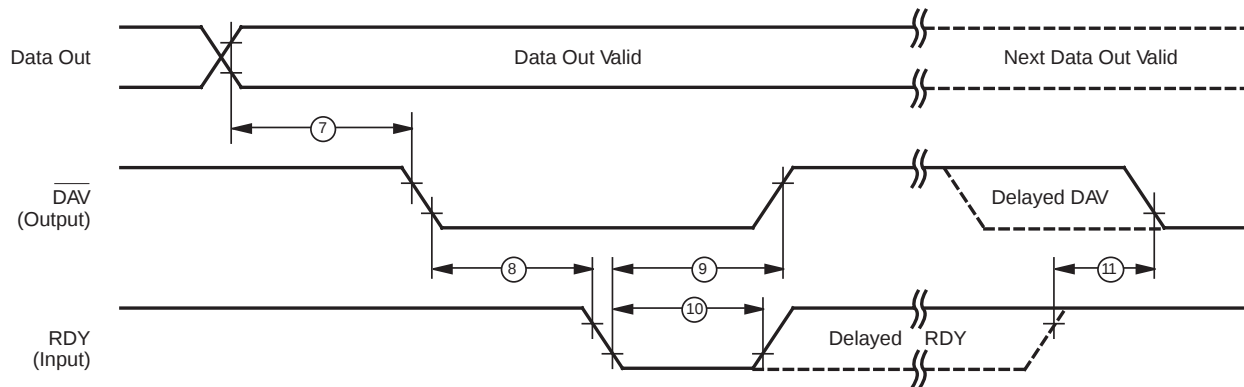
**Notes:**

1. Timing Reference uses 0.9  $V_{CC}$  for a logic 1 and 0.1  $V_{CC}$  for a logic 0.
2. Interrupt request through Port 3 (P33–P31).
3. Interrupt request through Port 3 (P30).
4. SMR – D5 = 0
5. Reg. WDTMR
6. Reg. SMR – D5 = 0
7. Reg. SMR – D5 = 1

Figure 12 shows the input handshake timing, and Figure 13 shows the output handshake timing. Table 11 describes the handshake timing.



**Figure 12. Input Handshake Timing**



**Figure 13. Output Handshake Timing**

**Table 11. Handshake Timing**

|    |              |                                     |                 | $T_A = 0\text{ }^{\circ}\text{C to }+70\text{ }^{\circ}\text{C}$<br>16 MHz |            | Data       |
|----|--------------|-------------------------------------|-----------------|----------------------------------------------------------------------------|------------|------------|
| No | Symbol       | Parameter                           | V <sub>CC</sub> | Min                                                                        | Max        | Direction  |
| 1  | TsDI(DAV)    | Data In Setup Time                  | 4.0 V<br>5.5 V  | 0                                                                          |            | IN<br>IN   |
| 2  | ThDI(DAV)    | Data In Hold Time                   | 4.0 V<br>5.5 V  | 0<br>0                                                                     |            | IN<br>IN   |
| 3  | TwDAV        | Data Available Width                | 4.0 V<br>5.5 V  | 155<br>110                                                                 |            | IN<br>IN   |
| 4  | TdDAVI(RDY)  | DAV Falling to RDY<br>Falling Delay | 4.0 V<br>5.5 V  |                                                                            | 160<br>115 | IN<br>IN   |
| 5  | TdDAVId(RDY) | DAV Rising to RDY<br>Falling Delay  | 4.0 V<br>5.5 V  |                                                                            | 120<br>80  | IN<br>IN   |
| 6  | TdRDYO(DAV)  | RDY Rising to DAV<br>Falling Delay  | 4.0 V<br>5.5 V  | 0<br>0                                                                     |            | IN<br>IN   |
| 7  | TdDO(DAV)    | Data Out to DAV<br>Falling Delay    | 4.0 V<br>5.5 V  | 63<br>63                                                                   |            | OUT<br>OUT |
| 8  | TdDAV0(RDY)  | DAV Falling to RDY<br>Falling Delay | 4.0 V<br>5.5 V  | 0<br>0                                                                     |            | OUT<br>OUT |
| 9  | TdRDY0(DAV)  | RDY Falling to DAV<br>Rising Delay  | 4.0 V<br>5.5 V  |                                                                            | 160<br>115 | OUT<br>OUT |
| 10 | TwRDY        | RDY Width                           | 4.0 V<br>5.5 V  | 110<br>80                                                                  |            | OUT<br>OUT |
| 11 | TdRDY0d(DAV) | RDY Rising to DAV<br>Falling Delay  | 4.0 V<br>5.5 V  |                                                                            | 110<br>80  | OUT        |

## Pin Functions

### **/DS (Output, Active Low)**

Data Strobe is activated once for each external memory transfer. For a READ operation, data must be available before the trailing edge of /DS. For WRITE operations, the falling edge of /DS indicates that output data is valid.

### **/AS (Output, Active Low)**

Address Strobe is pulsed once at the beginning of each machine cycle. Address output is through Port 0/Port 1 for all external programs. Memory address transfers are valid at the trailing edge of /AS. Under program control, /AS is placed in the high-impedance state along with Ports 0 and 1, Data Strobe, and Read/Write.

### **XTAL1 Crystal 1 (Time-Based Input)**

This pin connects a parallel-resonant crystal, ceramic resonator, LC, or RC network or an external single-phase clock to the on-chip oscillator input.

### **XTAL2 Crystal 2 (Time-Based Output)**

This pin connects a parallel-resonant, crystal, ceramic resonant, LC, or RC network to the on-chip oscillator output.

### **R//W Read/Write (Output, Write Low)**

The R//W signal is Low when the CCP is writing to the external program or data memory.

### **R//RL (Input)**

This pin, when connected to GND, disables the internal ROM and forces the device to function as a ROMless Z8.

► **Note:** When left unconnected or pulled high to  $V_{CC}$ , the part functions normally as a Z8 ROM version.

### **Port 0 (P07–P00)**

Port 0 is an 8-bit, bidirectional, CMOS-compatible port. These eight I/O lines are configured under software control as a nibble I/O port or as an address port for interfacing external memory. The output drivers are push-pull. Port 0 is placed under handshake control. In this configuration, Port 3, lines P32 and P35 are used as the handshake control /DAV0 and RDY0. Handshake signal direction is

dictated by the I/O direction to Port 0 of the upper nibble P07–P04. The lower nibble must have the same direction as the upper nibble.

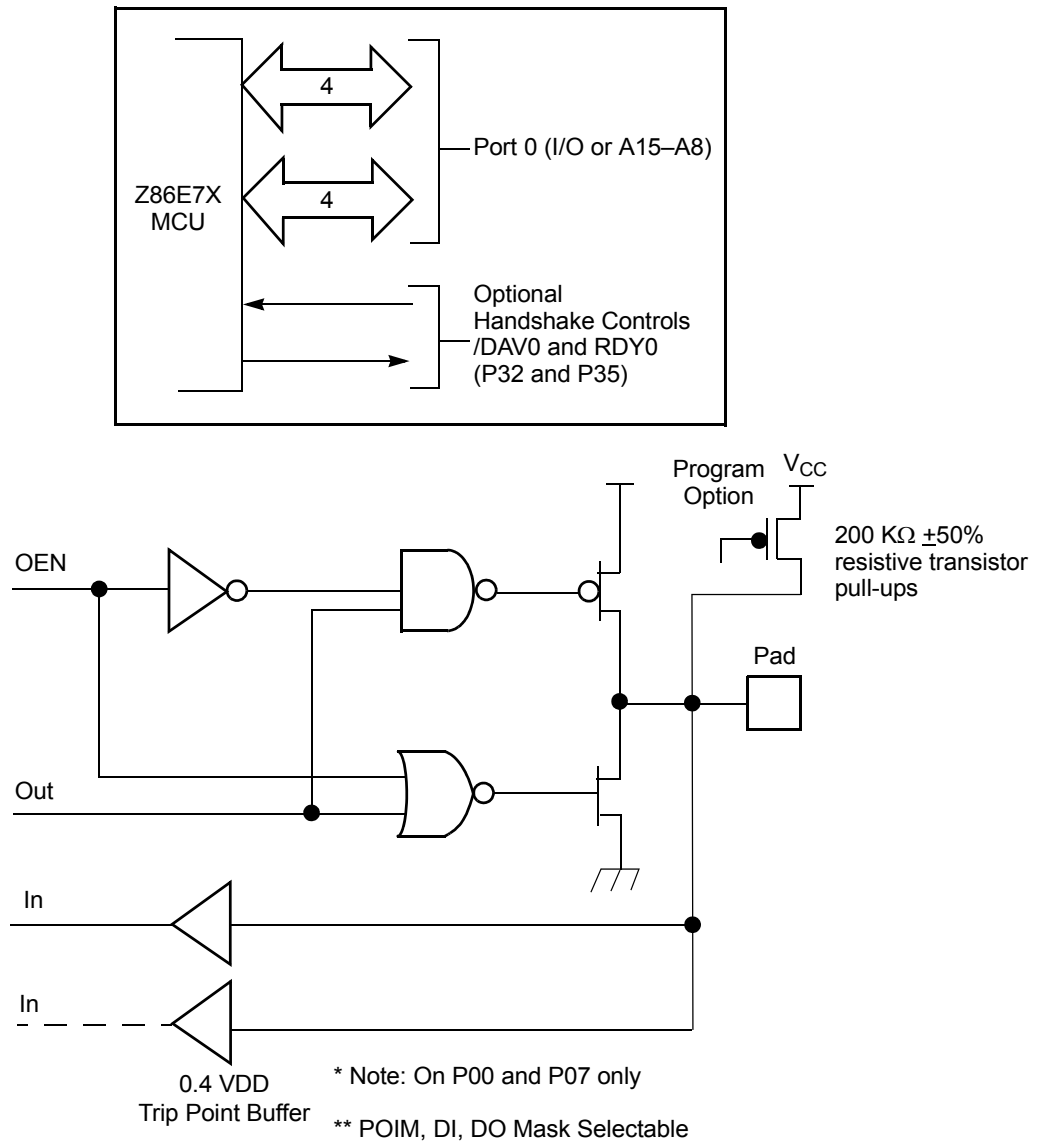
For external memory references, Port 0 can provide address bits A11–A8 (lower nibble) or A15–A8 (lower and upper nibble) depending on the required address space. If the address range requires 12 bits or less, the upper nibble of Port 0 can be programmed independently as I/O while the lower nibble is used for addressing. If one or both nibbles are needed for I/O operation, they must be configured by writing to the Port 0 mode register. After a hardware reset, Port 0 is configured as an input port.

Port 0 is set in the High-Impedance Mode if selected as an address output state along with Port 1 and the control signals /AS, /DS, and R/W.

A software option is available to program 0.4 V<sub>DD</sub> CMOS trip inputs on P00–P03. This allows direct interface to mouse/trackball IR sensors.

An optional 200±50% KΩ resistive transistor pull-up is available as a software option of all Port 0 bits with nibble select.

These pull-ups are disabled when configured (bit by bit) as an output. See [Figure 14](#).



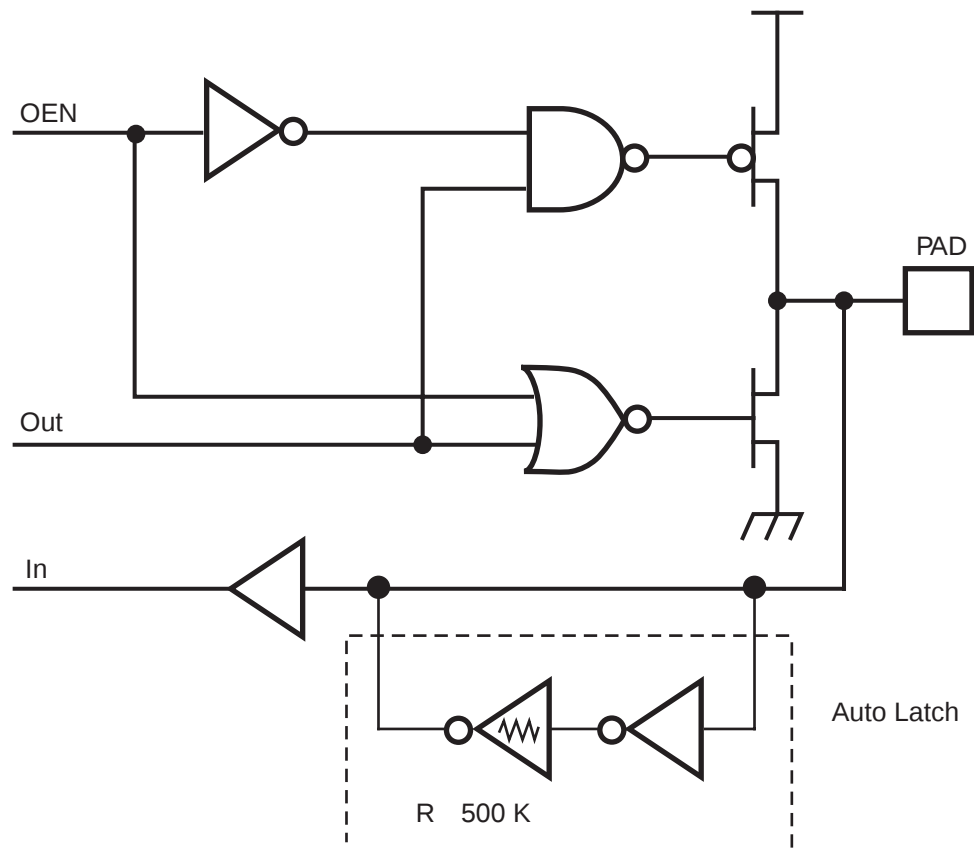
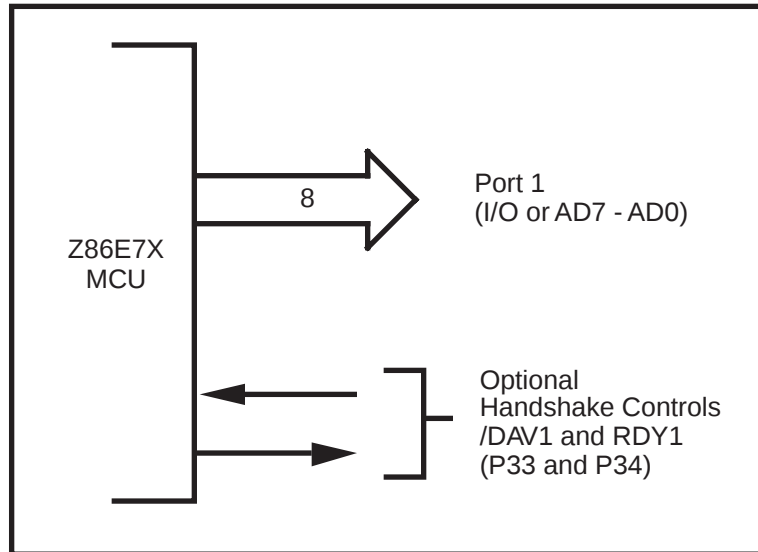
**Figure 14. Port 0 Configuration**



## **Port 1 (P17–P10)**

Port 1 is a multiplexed Address (A7–A0) and Data (D7–D0), CMOS-compatible port. Port 1 is dedicated to the ZiLOG ZBus<sup>®</sup>-compatible memory interface. The operations of Port 1 are supported by the Address Strobe (/AS) and Data Strobe (/DS) lines and by the Read/Write (R/W) and Data Memory (/DM) control lines. Data memory read/write operations are done through this port. If more than 256 external locations are required, Port 0 outputs the additional lines.

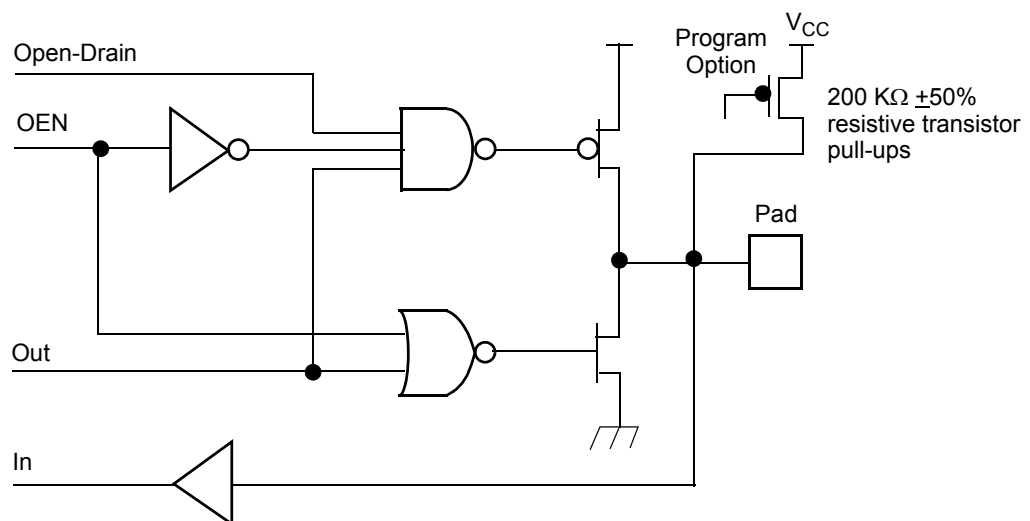
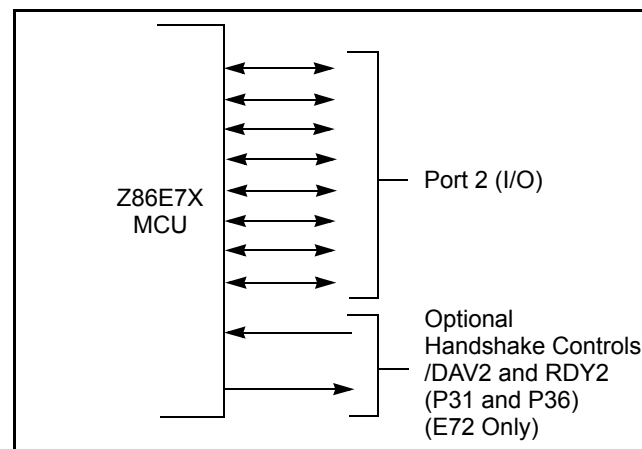
Port 1 can be placed in the high-impedance state along with Port 0, /AS, /DS, and R/W, allowing the Z86E7X to share common resources in multiprocessor and DMA applications. Port 1 can also be configured for standard port output mode. See [Figure 15](#).



**Figure 15. Port 1 Configuration**

## Port 2 (P27–P20)

Port 2 is an 8-bit, bidirectional, CMOS-compatible I/O port (see Figure 16). These eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A software option is available to connect eight 200 K $\Omega$  ( $\pm 50\%$ ) pull-up resistors on this port. Bits programmed as outputs are globally programmed as either push-pull or open-drain. Port 2 can be placed under handshake control. In this configuration, Port 3 lines, P31 and P36 are used as the handshake controls lines /DAV2 and RDY2. The handshake signal assignment for Port 3, lines P31 and P36 is dictated by the direction (input or output) assigned to Bit 7, Port 2.



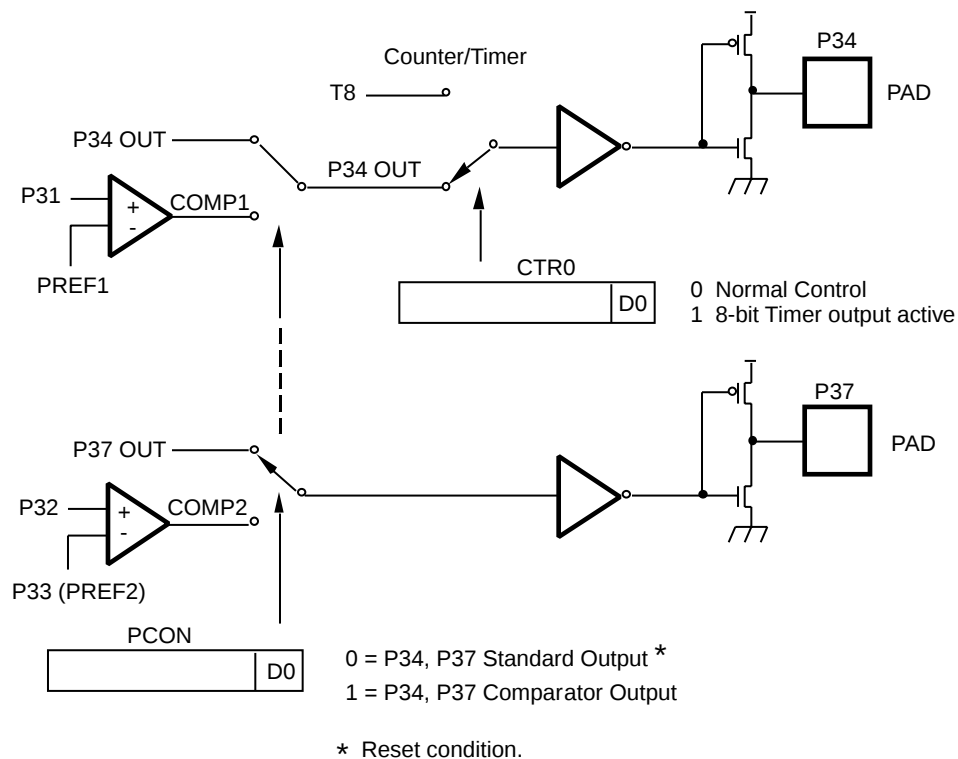
**Figure 16. Port 2 Configuration**

The CCP wakes up with the 8 bits of Port 2 configured as inputs with open-drain outputs.

Port 2 also has an 8-bit input OR and an AND gate that can be used to wake up the part. P20 can be programmed to access the edge-selection circuitry.

### Port 3 (P37–P31)

Port 3 is a 7-bit, CMOS-compatible port (see [Figure 17](#)). Port 3 consists of three fixed inputs (P33–P31) and four fixed outputs (P37–P34) and can be configured under software control for Input/Output, Interrupt, Port handshake, Data Memory functions, and output from the counter/timers. P31, P32, and P33 are standard CMOS inputs; outputs are push-pull.



**Figure 17. Port 3 Configuration**

Two on-board comparators process analog signals on P31 and P32 with reference to the voltage on Pref1 and P33. The analog function is enabled by program-

ming the Port 3 Mode Register (bit 1). P31 and P32 are programmable as rising, falling, or both edge-triggered interrupts (IRQ register bits 6 and 7). Pref1 and P33 are the comparator reference voltage inputs. Access to the Counter Timer edge-detection circuit is through P31 or P20 (see “CTR1(D)01h Register” on page 48).

Port 3 provides the following control functions: handshake for Ports 0, 1, and 2 (/DAV and RDY); three external interrupt request signals (IRQ2–IRQ0); Data Memory Select (/DM). See [Table 12](#).

**Table 12. Pin Assignments**

| Pin   | I/O | C/T   | Comp. | Int. | P0 HS | P1 HS | P2 HS | Ext |
|-------|-----|-------|-------|------|-------|-------|-------|-----|
| Pref1 | IN  |       | RF1   |      |       |       |       |     |
| P31   | IN  | IN    | AN1   | IRQ2 |       |       | D/R   |     |
| P32   | IN  |       | AN2   | IRQ0 | D/R   |       |       |     |
| P33   | IN  |       | RF2   | IRQ1 |       | D/R   |       |     |
| P34   | OUT | T8    | A01   |      |       | R/D   |       | D/M |
| P35   | OUT | T16   |       |      | R/D   |       |       |     |
| P36   | OUT | T8/16 |       |      |       |       | R/D   |     |
| P37   | OUT |       | A02   |      |       |       |       |     |
| P20   | I/O | IN    |       |      |       |       |       |     |

**Notes:**

HS = Handshake Signals

D = /DAV

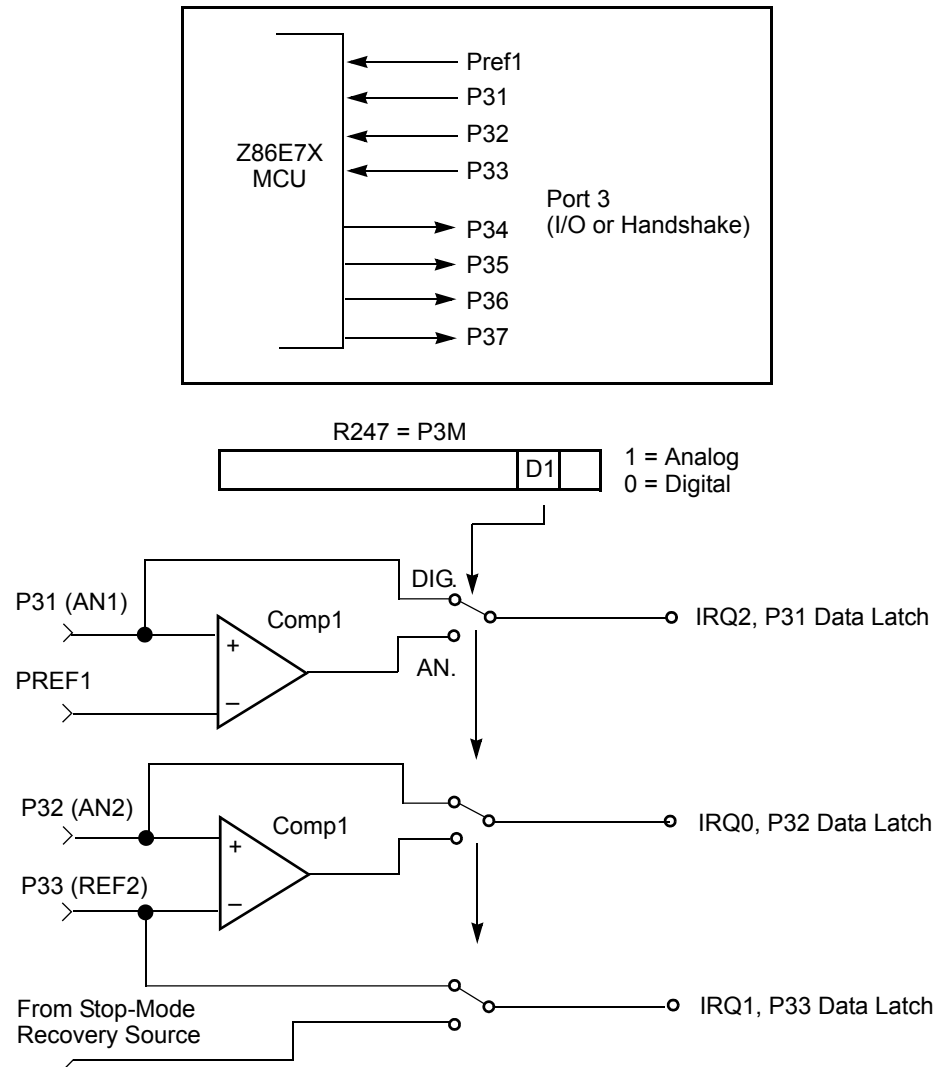
R = RDY

Port 3 also provides output for each of the counter/timers and the AND/OR Logic. Control is performed by programming bits D5–D4 of CTR1, bit 0 of CTR0, and bit 0 of CTR2.

## Comparator Inputs

In Analog Mode, Port 3 (P31 and P32) has a comparator front end. The comparator reference is supplied to P33 and Pref1. In this mode, the P33 internal data latch and its corresponding IRQ1 are diverted to the SMR sources (excluding P31, P32, and P33) as shown in [Figure 18](#). In digital mode, P33 is used as D3 of the Port 3 input register which then generates IRQ1 as shown in [Figure 23](#).

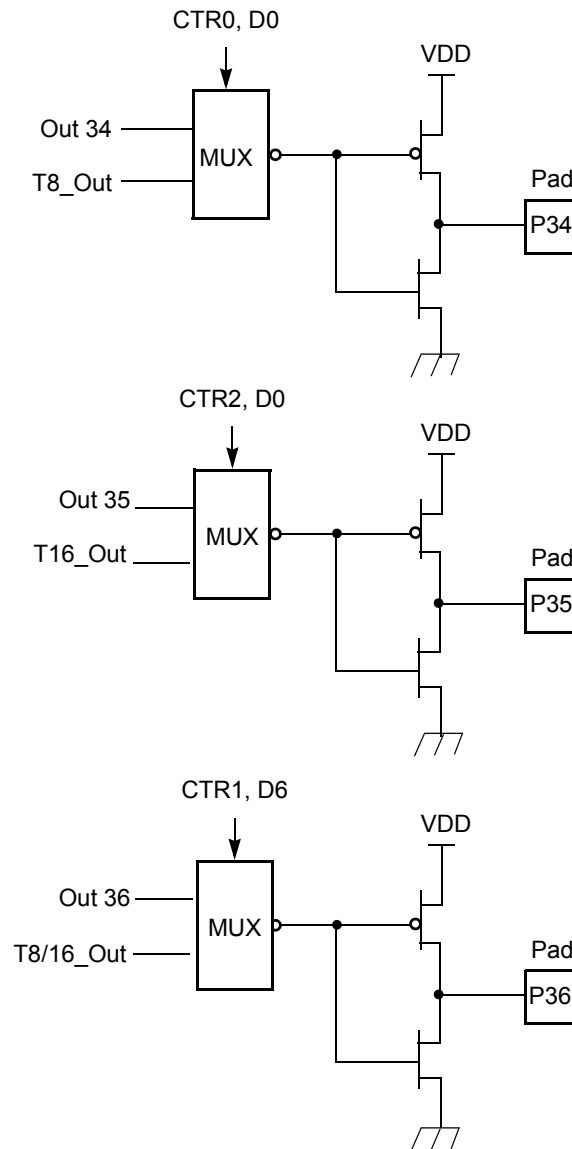
- **Note:** Comparators are disabled/powered down by entering STOP Mode. For P31–P33 to be used as a Stop-Mode recovery source, these inputs must be placed into digital mode.



**Figure 18. Port 3 Configuration**

## Comparator Outputs

These outputs can be programmed to be output on P34 and P37 through the PCON register ([Figure 19](#)).



**Figure 19. Port 3 Configuration**

## **/RESET (Input, Active Low)**

Reset initializes the MCU. Reset is accomplished either through Power-On, Watch-Dog Timer, Stop-Mode Recovery, Low-Voltage detection, or external reset. During Power-On Reset and Watch-Dog Timer Reset, the internally generated reset drives the reset pin Low for the POR time. Any devices driving the reset line need to be open-drain to avoid damage from a possible conflict during reset conditions. Pull-up is provided internally. There is no condition internal to the Z86E7X that does not allow an external reset to occur.

After the POR time, /RESET is a Schmitt-triggered input. To avoid asynchronous and noisy reset problems, the Z86E7X is equipped with a reset filter of four external clocks (4TpC). If the external reset signal is less than 4TpC in duration, no reset occurs. On the fifth clock after the reset is detected, an internal RST signal is latched and held for an internal register count of 18 external clocks or for the duration of the external reset, whichever is longer.

During the reset cycle, /DS is held active Low while /AS cycles at a rate of TpC/2. Program execution begins at location 000CH, 5–10 TpC cycles after the RST is released. For Power-On Reset, the typical reset output time is 5 ms.

- **Note:** The Z86E7X devices do not have internal pull resistors on Port 3 inputs.



## Functional Description

The Z86E72/73 microcontrollers incorporate special functions to enhance the Z8's functionality in consumer and battery-operated applications.

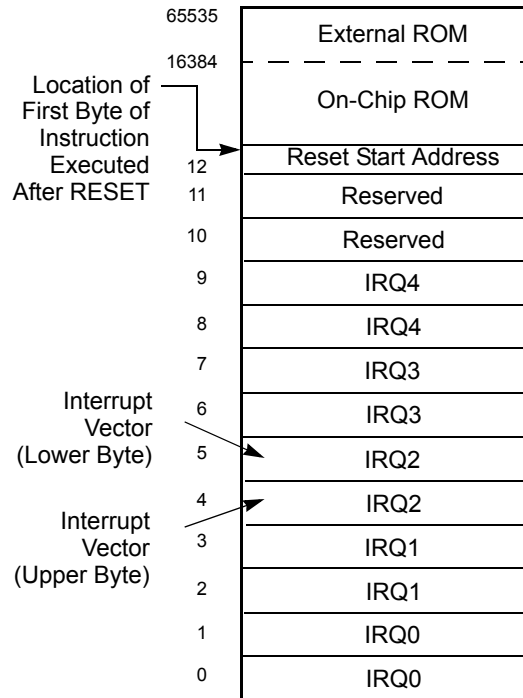
### Reset

The device is reset in one of the following conditions:

- Power-On Reset
- Watch-Dog Timer
- Stop-Mode Recovery Source
- Low Voltage Detection
- External Reset

### Program Memory

The Z86E72/73 microcontrollers address up to 16K/32 KB of internal program memory, with the remainder being external memory ([Figure 20](#)). The first 12 bytes of program memory are reserved for the interrupt vectors. These locations contain five 16-bit vectors that correspond to the five available interrupts. Addresses of 16K/32K consist of on-chip OTP. At addresses 16K or 32K and greater, the Z86E72/73 microcontrollers execute external program memory fetches (see “External Memory” on page 38).



**Figure 20. Program Memory Map**

## RAM

The Z86E72 has a 768-byte RAM; 256 bytes make up the register file. The remaining 512 bytes make up the Extended Data RAM. The Z86E73 has just the 256 bytes of the register file.

## Extended Data RAM

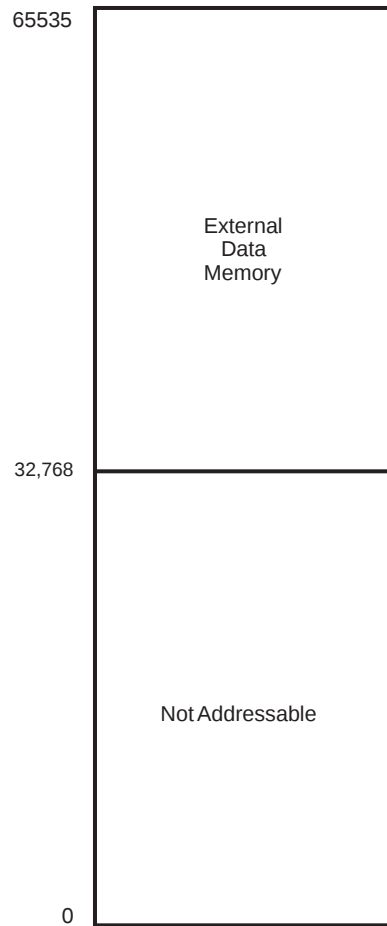
The Extended Data RAM of the Z86E72 occupies the address range FE00H–FFFFH (512 bytes). This range of addresses FD00H–FFFFH cannot be used to directly read from or write to external memory. Accessing the Extended Data RAM is accomplished by using LDE or LDEI instructions. Port 1 and Port 0 are free to be set as I/O or ADDR/DATA modes; expect high-impedance when accessing Extended Data RAM. In addition, if the external memory uses the same address range of the Extended Data RAM, it can be used as the External Stack only.

Exercise caution when using extended data RAM (not Z8 RAM) on the Z86E72 OTP microcontroller. Extended RAM spaces FF0C–FF0F, FF10, FE0C–FE0F, and FE10 are reserved. Do not use these extended RAM locations.

- **Note:** The Extended Data RAM cannot be used as STACK or instruction/code memory. Accessing the Extended Data RAM has the following condition: P01M register bits D4–D3 cannot be set to 11.

## External Memory

The Z86E72/73 microcontrollers address up to 32 KB (minus FD00H–FFFFH) of external memory beginning at address 8000H (32K+1). External data memory is included with, or separated from, the external program memory space. /DM, an optional I/O function that is programmed to appear on P34, is used to distinguish between data and program memory space. The state of the /DM signal is controlled by the type of instruction being executed. An LDC op code references PROGRAM (/DM inactive) memory, and an LDE instruction references data (/DM active Low) memory. See [Figure 21](#).



**Figure 21. External Memory Map**

## Expanded Register File

The register file has been expanded to allow for additional system control registers and for mapping of additional peripheral devices into the register address area. The Z8 register address space R0 through R15 has been implemented as 16 banks of 16 registers per bank. These register groups are known as the Expanded Register File (ERF).

Bits 7–4 of register RP select the working register group. Bits 3–0 of register RP select the expanded register file bank.

► **Note:** The expanded register bank is also referred to as the expanded register group (see [Figure 22](#)).

The upper nibble of the register pointer ([Figure 23](#) on page 42) selects which working register group of 16 bytes in the register file, out of the possible 256, is accessed. The lower nibble selects the expanded register file bank and, in the case of the Z86E7X family, banks 0, F, and D are implemented. A 0h in the lower nibble allows the normal register file (bank 0) to be addressed, but any other value from 1h to Fh exchanges the lower 16 registers to an expanded register bank.

For example, Z86E73 (see [Figure 22](#)):

```
R253 RP = 00H
      R0 = Port0
      R1 = Port1
      R2 = Port2
      R3 = Port3
```

But if:

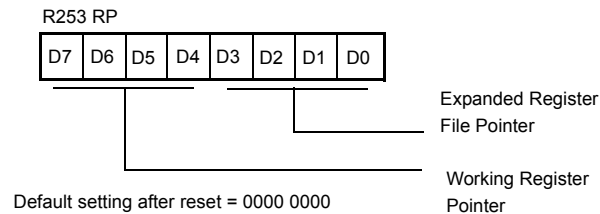
```
R253 RP = 0DH
      R0 = CTRL0
      R1 = CTRL1
      R2 = CTRL2
      R3 = Reserved
```

The counter/timers are mapped into ERF group D. Access is easily done using the following example:

```
LD      RP,#0Dh      ; Select ERF D for access and register
                        ; Bank 0 as the working register group.
LD      R0,#xx        ; access CTRL0
LD      1,#xx        ; access CTRL1
LD      RP,#7Dh      ; Select expanded register group (ERF)
                        ; group D for access and register
                        ; Bank 7 as the working register bank.
LD      R1,2          ; CTRL2→register 71H
```



**Figure 22. Expanded Register File Architecture**

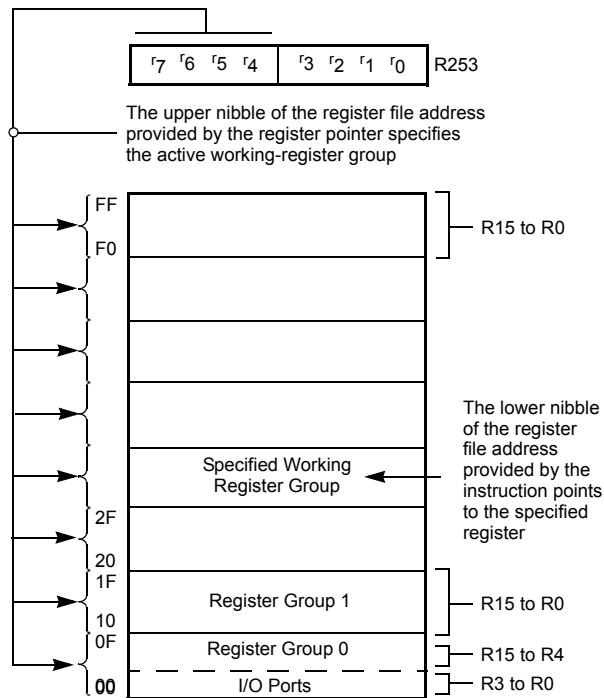


**Figure 23. Register Pointer**

## Register File

The register file (bank 0) consists of 4 I/O port registers, 236 general-purpose registers, and 16 control and status registers (R0–R3, R4–R239, and R240–R255, respectively), plus two expanded registers groups (Banks D and F). Instructions can access registers directly or indirectly through an 8-bit address field. This allows a short, 4-bit register address using the register pointer ([Figure 24](#)). In the 4-bit mode, the register file is divided into 16 working register groups, each occupying 16 continuous locations. The register pointer addresses the starting location of the active working register group.

- **Note:** Working register group E0–EF of Bank 0 are only accessed through working registers and indirect addressing modes.



**Figure 24. Register Pointer**

## Stack

The Z86E7X external data memory or the internal register file is used for the stack. An 8-bit stack pointer (R255) is used for the internal stack that resides in the general-purpose registers (R4–R239). SPH is used as a general-purpose register only when using internal stacks.

- **Note:** When SPH is used as a general-purpose register and Port 0 is in address mode, the contents of SPH are loaded into Port 0 whenever the internal stack is accessed.

## Counter/Timer Register Description

Table 13 describes the expanded register group D.

**Table 13. Expanded Register Group D**

|         |          |
|---------|----------|
| (D) 0Ch | Reserved |
| (D) 0Bh | HI8      |
| (D) 0Ah | LO8      |

**Table 13. Expanded Register Group D (Continued)**

|         |          |
|---------|----------|
| (D) 09h | HI16     |
| (D) 08h | LO16     |
| (D) 07h | TC16H    |
| (D) 06h | TC16L    |
| (D) 05h | TC8H     |
| (D) 04h | TC8L     |
| (D) 03h | Reserved |
| (D) 02h | CTR2     |
| (D) 01h | CTR1     |
| (D) 00h | CTR0     |

#### HI8(D)0Bh Register

This register ([Table 14](#)) holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 1.

**Table 14. HI8(D)0Bh Register**

| Field         | Bit Position | Value | Description                |
|---------------|--------------|-------|----------------------------|
| T8_Capture_HI | 76543210     | R/W   | Captured Data<br>No Effect |

#### LO8(D)0Ah Register

This register ([Table 15](#)) holds the captured data from the output of the 8-bit Counter/Timer0. This register is typically used to hold the number of counts when the input signal is 0.

**Table 15. LO8(D)0Ah Register**

| Field         | Bit Position | Value | Description                |
|---------------|--------------|-------|----------------------------|
| T8_Capture_LO | 76543210     | R/W   | Captured Data<br>No Effect |

### HI16(D)09h Register

This register ([Table 16](#)) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the MS-Byte of the data.

**Table 16. HI16(D)09h Register**

| Field          | Bit Position | Value | Description                |
|----------------|--------------|-------|----------------------------|
| T16_Capture_HI | 76543210     | R/W   | Captured Data<br>No Effect |

### LO16(D)08h Register

This register ([Table 17](#)) holds the captured data from the output of the 16-bit Counter/Timer16. This register holds the LS-Byte of the data.

**Table 17. LO16(D)08h Register**

| Field          | Bit Position | Value | Description                |
|----------------|--------------|-------|----------------------------|
| T16_Capture_LO | 76543210     | R/W   | Captured Data<br>No Effect |

### TC16H(D)07h Register

[Table 18](#) describes the Counter/Timer2 MS-Byte Hold Register.

**Table 18. TC16H(D)07h Register**

| Field       | Bit Position | Value | Description |
|-------------|--------------|-------|-------------|
| T16_Data_HI | 76543210     | R/W   | Data        |

### TC16L(D)06h Register

[Table 19](#) describes the Counter/Timer2 LS-Byte Hold Register.

**Table 19. TC16L(D)06h Register**

| Field       | Bit Position | Value | Description |
|-------------|--------------|-------|-------------|
| T16_Data_LO | 76543210     | R/W   | Data        |

### TC8H(D)05h Register

Table 20 describes the Counter/Timer8 High Hold Register.

**Table 20. TC8H(D)05h Register**

| Field       | Bit Position | Value | Description |
|-------------|--------------|-------|-------------|
| T8_Level_HI | 76543210     | R/W   | Data        |

### TC8L(D)04h Register

Table 21 describes the Counter/Timer8 Low Hold Register.

**Table 21. TC8L(D)04h Register**

| Field       | Bit Position | Value | Description |
|-------------|--------------|-------|-------------|
| T8_Level_LO | 76543210     | R/W   | Data        |

### CTR0(D)00h Register

Table 22 describes the Counter/Timer8 Control Register.

**Table 22. CTR0(D)00h Register**

| Field            | Bit Position |     | Value | Description               |
|------------------|--------------|-----|-------|---------------------------|
| T8_Enable        | 7-----       | R   | 0*    | Counter Disabled          |
|                  |              |     | 1     | Counter Enabled           |
|                  |              | W   | 0     | Stop Counter              |
|                  |              |     | 1     | Enable Counter            |
| Single/Modulo    | -6-----      | R/W | 0     | Modulo-N                  |
|                  |              |     | 1     | Single Pass               |
| Time_Out         | --5-----     | R   | 0     | No Counter Time-Out       |
|                  |              |     | 1     | Counter Time-Out Occurred |
|                  |              |     | 0     | No Effect                 |
|                  |              | W   | 1     | Reset Flag to 0           |
| T8_Clock         | ---43---     |     | R/W   | 0 0                       |
|                  |              | 0 1 |       | SCLK/2                    |
|                  |              | 1 0 |       | SCLK/4                    |
|                  |              | 1 1 |       | SCLK/8                    |
| Capture_INT_MASK | -----2--     | R/W | 0     | Disable Data Capture Int. |
|                  |              |     | 1     | Enable Data Capture Int.  |

**Table 22. CTR0(D)00h Register (Continued)**

| Field            | Bit Position |     | Value | Description           |
|------------------|--------------|-----|-------|-----------------------|
| Counter_INT_Mask | -----1-      | R/W | 0     | Disable Time-Out Int. |
|                  |              |     | 1     | Enable Time-Out Int.  |
| P34_Out          | -----0       | R/W | 0*    | P34 as Port Output    |
|                  |              |     | 1     | T8 Output on P34      |

Note: \*Indicates the value upon Power-On Reset

### T8 Enable

This field enables T8 when set (written) to 1.

### Single/Modulo-N

When set to 0 (modulo-n), the counter reloads the initial value when the terminal count is reached. When set to 1 (single pass), the counter stops when the terminal count is reached.

### Time-Out

This bit is set when T8 times out (terminal count reached). To reset this bit, a 1 must be written to this location.

- **Notes:** This is the only way to reset this status condition; therefore, you must reset this bit before using/enabling the counter/timers.

Care must be taken when using the OR or AND commands to manipulate CTR0, bit 5 and CTR1, bits 0 and 1 (demodulation mode). These instructions use a Read-Modify-Write sequence in which the current status from the CTR0 and CTR1 registers is ORed or ANDed with the designated value and then written back into the registers. For example, when the status of bit 5 is 1, a reset condition occurs.

### T8 Clock

This bit defines the frequency of the input signal to T8.

### Capture\_INT\_Mask

Set this bit to allow interrupt when data is captured into either LO8 or HI8 upon a positive or negative edge detection in demodulation mode.

### Counter\_INT\_Mask

Set this bit to allow interrupt when T8 has a time out.

### P34\_Out

This bit defines whether P34 is used as a normal output pin or the T8 output.

### CTR1(D)01h Register

This register ([Table 23](#)) controls the functions in common with the T8 and T16.

**Table 23. CTR1(D)01h Register**

| Field                          | Bit Position |     | Value | Description       |
|--------------------------------|--------------|-----|-------|-------------------|
| Mode                           | 7-----       | R/W | 0*    | Transmit Mode     |
|                                |              |     | 1     | Demodulation Mode |
| P36_Out/Demodulator_Input      | -6-----      | R/W | 0*    | Transmit Mode     |
|                                |              |     | 1     | Port Output       |
|                                |              |     | 0     | T8/16 Output      |
|                                |              |     | 1     | Demodulation Mode |
| T8/T16_Logic/Edge_Detect       | --54----     | R/W | 0 0   | P31               |
|                                |              |     | 0 1   | P20               |
|                                |              |     | 1 0   | Transmit Mode     |
|                                |              |     | 1 1   | AND               |
|                                |              |     | 0 0   | OR                |
|                                |              |     | 0 1   | NOR               |
|                                |              |     | 1 0   | NAND              |
|                                |              |     | 1 1   | Demodulation Mode |
| Transmit_Submode/Glitch_Filter | ----32--     | R/W | 0 0   | Falling Edge      |
|                                |              |     | 0 1   | Rising Edge       |
|                                |              |     | 1 0   | Both Edges        |
|                                |              |     | 1 1   | Reserved          |
|                                |              |     | 0 0   | Transmit Mode     |
|                                |              |     | 0 1   | Normal Operation  |
|                                |              |     | 1 0   | Ping-Pong Mode    |
|                                |              |     | 1 1   | T16_OUT = 0       |
|                                |              |     | 0 0   | T16_OUT = 1       |
|                                |              |     | 0 1   | Demodulation Mode |
|                                |              |     | 1 0   | No Filter         |
|                                |              |     | 1 1   | 4 SCLK Cycle      |
|                                |              |     | 0 0   | 8 SCLK Cycle      |
|                                |              |     | 0 1   | 16 SCLK Cycle     |

**Table 23. CTR1(D)01h Register (Continued)**

| Field                        | Bit Position |     | Value | Description                             |
|------------------------------|--------------|-----|-------|-----------------------------------------|
| Initial_T8_Out/Rising_Edge   | -----1-      | R/W | 0     | Transmit Mode<br>T8_OUT is 0 Initially  |
|                              |              |     | 1     | T8_OUT is 1 Initially                   |
|                              |              | R   | 0     | Demodulation Mode<br>No Rising Edge     |
|                              |              |     | 1     | Rising Edge Detected                    |
|                              |              | W   | 0     | No Effect                               |
|                              |              |     | 1     | Reset Flag to 0                         |
| Initial_T16_Out/Falling_Edge | -----0       | R/W | 0     | Transmit Mode<br>T16_OUT is 0 Initially |
|                              |              |     | 1     | T16_OUT is 1 Initially                  |
|                              |              | R   | 0     | Demodulation Mode<br>No Falling Edge    |
|                              |              |     | 1     | Falling Edge Detected                   |
|                              |              | W   | 0     | No Effect                               |
|                              |              |     | 1     | Reset Flag to 0                         |

Note: \* Indicates the value upon Power-On Reset.

### Mode

If it is 0, the counter/timers are in the transmit mode; otherwise, they are in the demodulation mode.

### P36\_Out/Demodulator\_Input

In transmit mode, this bit defines whether P36 is used as a normal output pin or the combined output of T8 and T16.

In demodulation mode, this bit defines whether the input signal to the counter/timers is from P20 or P31.

### T8/T16\_Logic/Edge \_Detect

In transmit mode, this field defines how the outputs of T8 and T16 are combined (AND, OR, NOR, NAND).

In demodulation mode, this field defines which edge needs to be detected by the edge detector.

### Transmit\_Submode/Glitch Filter

In transmit mode, this field defines whether T8 and T16 are in the “Ping-Pong” mode or in independent normal operation mode. Setting this field to “Normal

Operation Mode” terminates the “Ping-Pong Mode” operation. When set to 10, T16 is immediately forced to a 0. When set to 11, T16 is immediately forced to a 1.

In demodulation mode, this field defines the width of the glitch that must be filtered out.

#### **Initial\_T8\_Out/Rising\_Edge**

In transmit mode, if 0, the output of T8 is set to 0 when it starts to count. If 1, the output of T8 is set to 1 when it starts to count. When this bit is set to 1 or 0, T8\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled, a transition occurs to the initial state set by CTR1, D1.

In demodulation mode, this bit is set to 1 when a rising edge is detected in the input signal. To reset it, a 1 must be written to this location.

#### **Initial\_T16 Out/Falling\_Edge**

In transmit mode, if it is 0, the output of T16 is set to 0 when it starts to count. If it is 1, the output of T16 is set to 1 when it starts to count. This bit is effective only in Normal or Ping-Pong Mode (CTR1, D3, D2). When this bit is set, T16\_OUT is set to the opposite state of this bit. This ensures that when the clock is enabled a transition occurs to the initial state set by CTR1, D0.

In demodulation mode, this bit is set to 1 when a falling edge is detected in the input signal. To reset it, a 1 must be written to this location.

- **Note:** Modifying CTR1 (D1 or D0) while the counters are enabled causes unpredictable output from T8/T16 out.

## CTR2(D)02h Register

Table 24 describes the Counter/Timer16 Control Register.

**Table 24. CTR2(D)02h Register**

| Field            | Bit Position |     | Value | Description                 |
|------------------|--------------|-----|-------|-----------------------------|
| T16_Enable       | 7-----       | R   | 0*    | Counter Disabled            |
|                  |              |     | 1     | Counter Enabled             |
|                  |              | W   | 0     | Stop Counter                |
|                  |              |     | 1     | Enable Counter              |
| Submode/Modulo-N | -6-----      | R/W | 0     | Transmit Mode               |
|                  |              |     | 1     | Modulo-N                    |
|                  |              |     | 0     | Single Pass                 |
|                  |              |     | 1     | Demodulation Mode           |
| Time_Out         | --5-----     | R   | 0     | T16 Recognizes Edge         |
|                  |              |     | 1     | T16 Does Not Recognize Edge |
|                  |              | W   | 0     | No Counter Time-Out         |
|                  |              |     | 1     | Counter Time-Out Occurred   |
| T16_Clock        | ---43---     | R/W | 00    | No Effect                   |
|                  |              |     | 01    | Reset Flag to 0             |
|                  |              |     | 10    | SCLK                        |
|                  |              |     | 11    | SCLK/2                      |
| Capture_INT_Mask | -----2--     | R/W | 0     | SCLK/4                      |
|                  |              |     | 1     | SCLK/8                      |
| Counter_INT_Mask | -----1-      | R/W | 0     | Disable Data Capture Int.   |
|                  |              |     | 1     | Enable Data Capture Int.    |
| P35_Out          | -----0       | R/W | 0*    | Disable Time-Out Int.       |
|                  |              |     | 1     | Enable Time-Out Int.        |

Note: \* Indicates the value upon Power-On Reset.

### T16\_Enable

This field enables T16 when set to 1.

### Single/Modulo-N

In transmit mode, when set to 0, the counter reloads the initial value when terminal count is reached. When set to 1, the counter stops when the terminal count is reached.

In demodulation mode, when set to 0, T16 captures and reloads on detection of all the edges. When set to 1, T16 captures and detects on the first edge, but ignores the subsequent edges. For details, see “T16 Demodulation Mode” on page 60.

### Time\_Out

This bit is set when T16 times out (terminal count reached). To reset it, a 1 must be written to this location.

### T16\_Clock

This bit defines the frequency of the input signal to Counter/Timer16.

### Capture\_INT\_Mask

Set this bit to allow interrupt when data is captured into LO16 and HI16.

### Counter\_INT\_Mask

Set this bit to allow interrupt when T16 times out.

### P35\_Out

This bit defines whether P35 is used as a normal output pin or T16 output.

### SMR2(F)0Dh Register

[Table 25](#) describes Stop-Mode Recovery Register 2.

**Table 25. SMR2(F)0Dh Register**

| Field          | Bit Position |   | Value                                                 | Description                                                                                                                                                                                      |
|----------------|--------------|---|-------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Reserved       | 7-----       |   | 0                                                     | Reserved (Must be 0)                                                                                                                                                                             |
| Recovery Level | -6-----      | W | 0*<br>1                                               | Low<br>High                                                                                                                                                                                      |
| Reserved       | --5-----     |   | 0                                                     | Reserved (Must be 0)                                                                                                                                                                             |
| Source         | ---432--     | W | 000*<br>001<br>010<br>011<br>100<br>101<br>110<br>111 | A. POR Only<br>B. NAND of P23–P20<br>C. NAND or P27–P20<br>D. NOR of P33–P31<br>E. NAND of P33–P31<br>F. NOR of P33–P31, P00, P07<br>G. NAND of P33–P31, P00, P07<br>H. NAND of P33–P31, P22–P20 |
| Reserved       | -----10      |   | 00                                                    | Reserved (Must be 0)                                                                                                                                                                             |

Note: \* Indicates the value upon Power-On Reset.

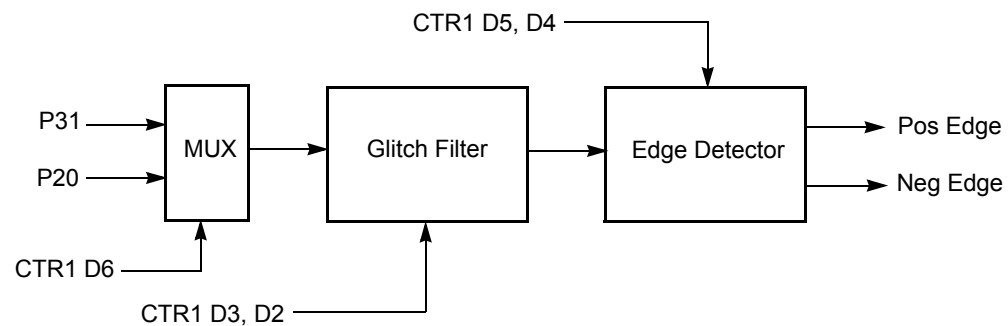
## Counter/Timer Functional Blocks

The following are the counter/timer functional blocks:

- Input circuit
- Eight-bit counter/timer circuits (page 54)
- Sixteen-bit counter/timer circuits (page 59)
- Output circuit (page 62)

### Input Circuit

The edge detector monitors the input signal on P31 or P20. Based on CTR1 D5–D4, a pulse is generated at the Pos Edge or Neg Edge line when an edge is detected. Glitches in the input signal that have a width less than specified (CTR1 D3, D2) are filtered out (see Figure 25).



**Figure 25. Glitch Filter Circuitry**

## Eight-Bit Counter/Timer Circuits

Figure 26 shows the 8-bit counter/timer circuits.

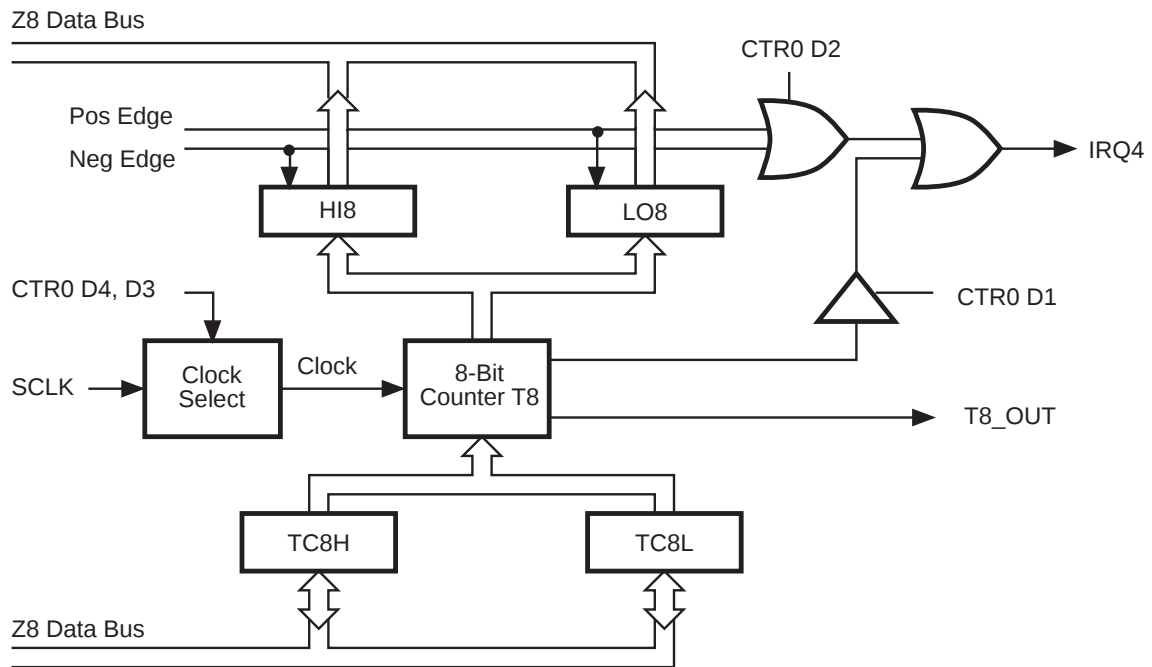


Figure 26. Eight-Bit Counter/Timer Circuits

### T8 Transmit Mode

When T8 is enabled, the output of T8 depends on CTR1, D1. If it is 0, T8\_OUT is 1. If it is 1, T8\_OUT is 0.

When T8 is enabled, the output T8\_OUT switches to the initial value (CTR1 D1). If the initial value (CTR1 D1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter (see Figure 27). In Single-Pass Mode (CTR0 D6), T8 counts down to 0 and stops, T8\_OUT toggles, the time-out status bit (CTR0 D5) is set, and a time-out interrupt can be generated if it is enabled (CTR0 D1). See Figure 28. In Modulo-N Mode, upon reaching terminal count, T8\_OUT is toggled, but no interrupt is generated. Then T8 loads a new count (if the T8\_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8\_OUT, sets the time-out status bit (CTR0 D5), and generates an interrupt if enabled (CTR0 D1). See Figure 29. This completes one cycle. T8 then loads from TC8H or TC8L according to the T8\_OUT level, and repeats the cycle.

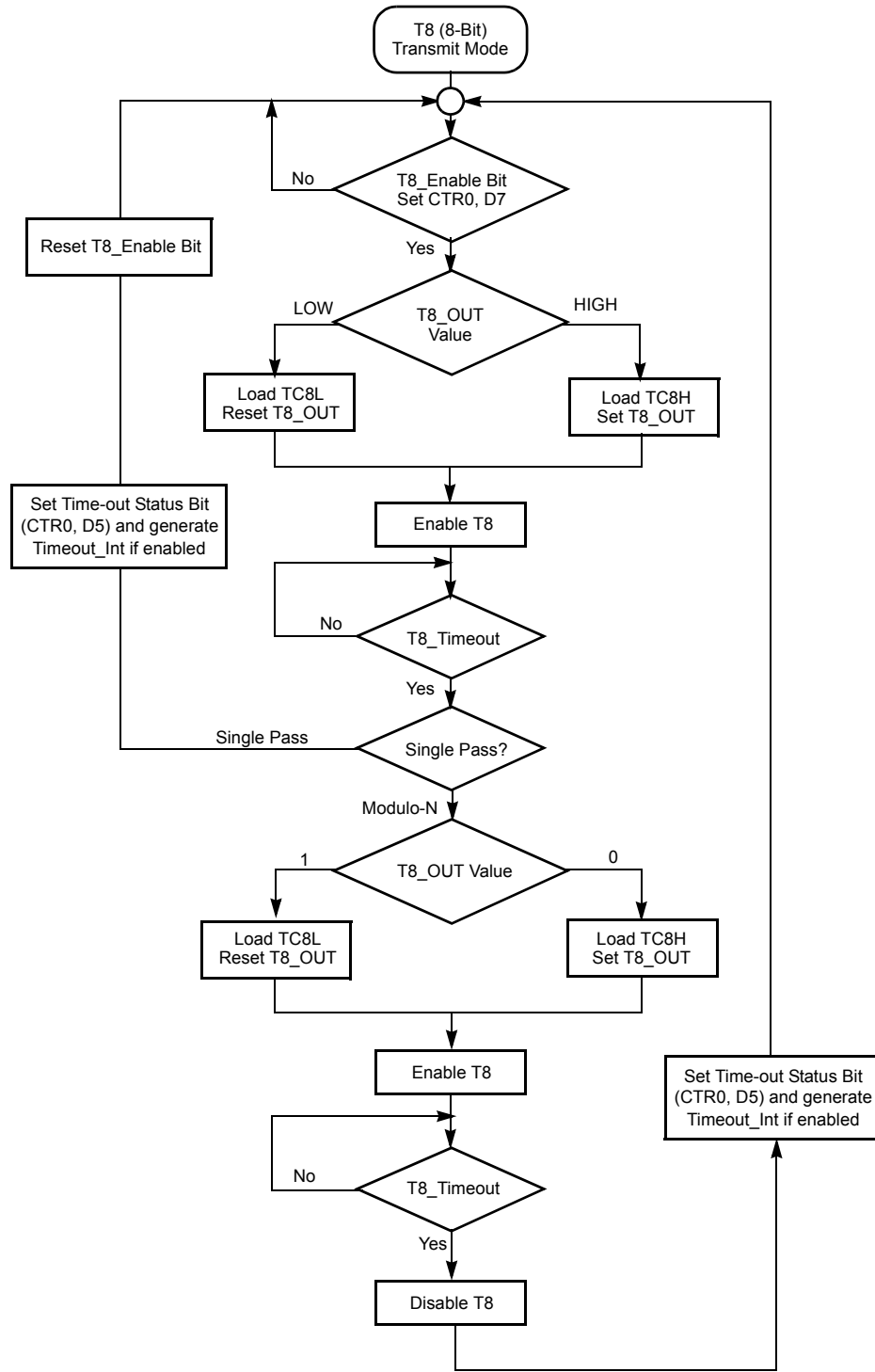
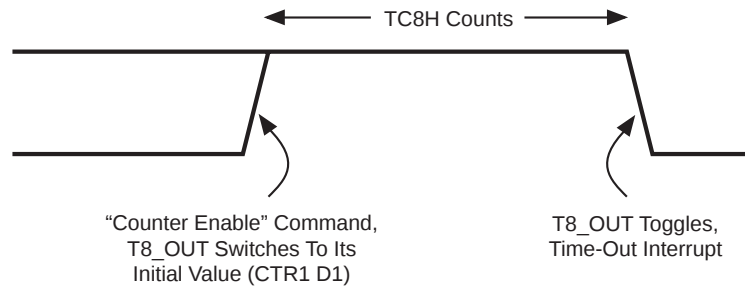
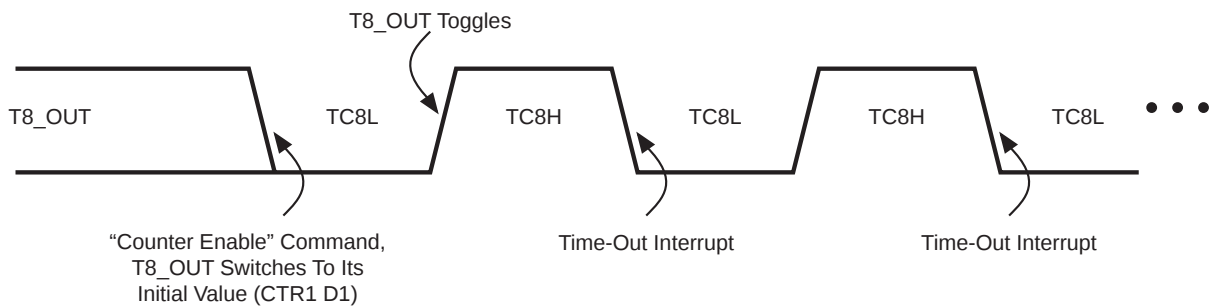


Figure 27. Transmit Mode Flowchart



**Figure 28. T8\_OUT in Single-Pass Mode**



**Figure 29. T8\_OUT in Modulo-N Mode**

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded. Do not write these registers at the time the values are to be loaded into the counter/timer, to ensure known operation. An initial count of 1 is not allowed (a nonfunction occurs). An initial count of 0 causes TC8 to count from 0 to FFh to FEh.

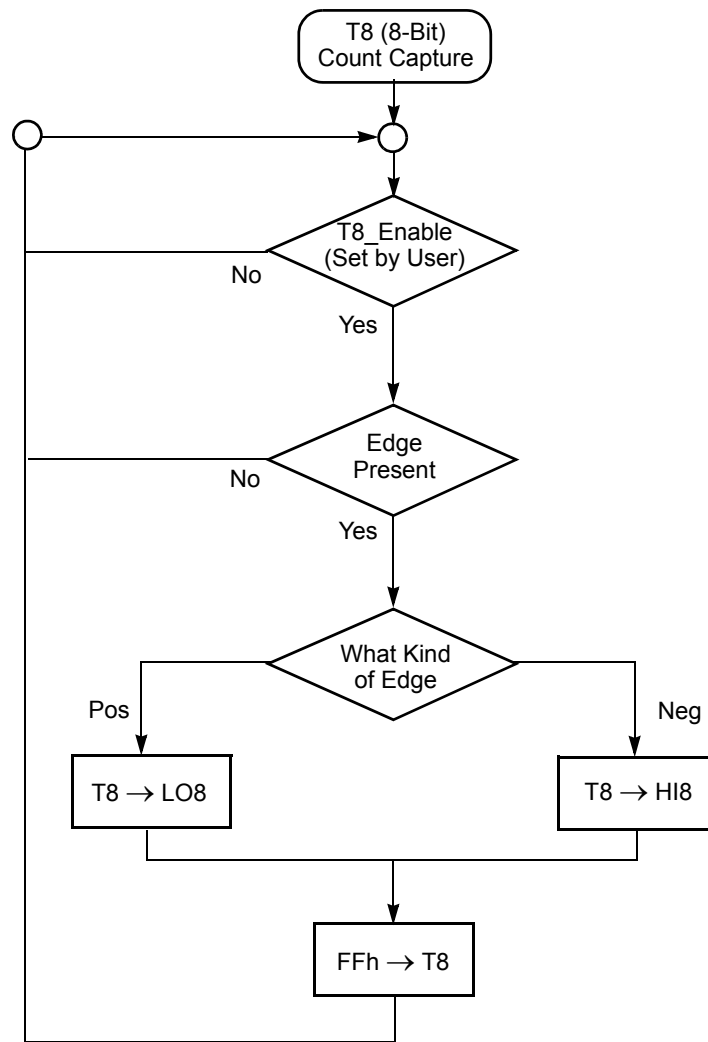
► **Note:** “h” is used for hexadecimal values.

Transition from 0 to FFh is not a time-out condition.

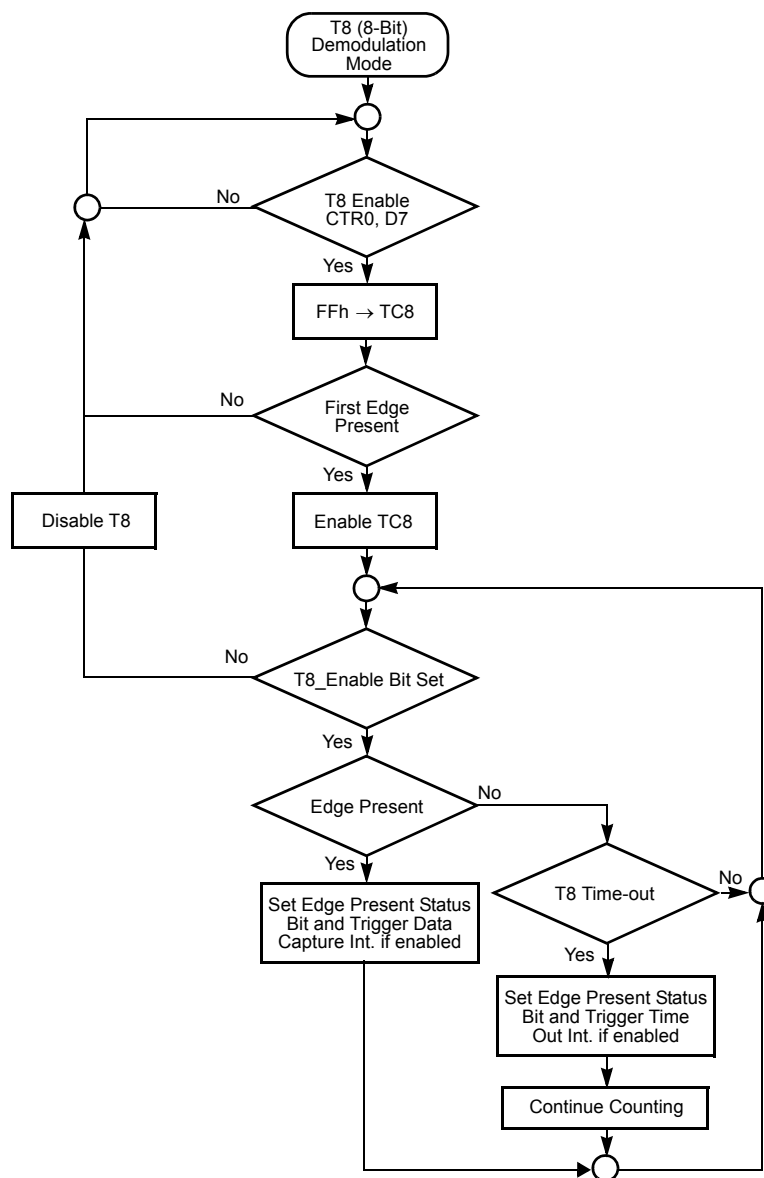
► **Note:** Do not use the same instructions for stopping the counter/timers and setting the status bits. Two successive commands are necessary. First, stop the counter/timers, and, second, reset the status bits. This is required because it takes one counter/timer clock interval for the initiated event to actually occur.

### T8 Demodulation Mode

You need to program TC8L and TC8H to FFh. After T8 is enabled, when the first edge (rising, falling, or both depending on CTR1 D5, D4) is detected, it starts to count down. When a subsequent edge (rising, falling, or both depending on CTR1 D5, D4) is detected during counting, the current value of T8 is one's complemented and put into one of the capture registers. If it is a positive edge, data is put into LO8; if negative edge, HI8. One of the edge-detect status bits (CTR1 D1, D0) is set, and an interrupt can be generated if enabled (CTR0 D2). Meanwhile, T8 is loaded with FFh and starts counting again. When T8 reaches 0, the time-out status bit (CTR0 D5) is set, an interrupt can be generated if enabled (CTR0 D1), and T8 continues counting from FFh (see [Figure 30](#) and [Figure 31](#)).



**Figure 30. Demodulation Mode Count Capture Flowchart**



**Figure 31. Demodulation Mode Flowchart**

## Sixteen-Bit Counter/Timer Circuits

Figure 32 shows the 16-bit counter/timer circuits.

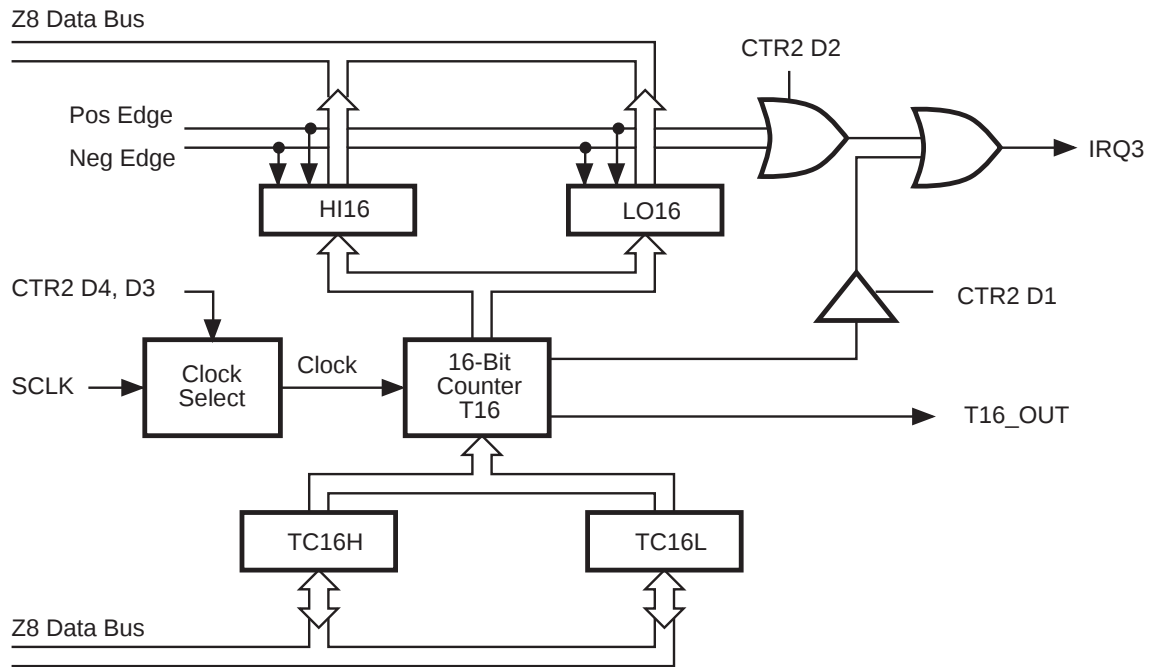


Figure 32. Sixteen-Bit Counter/Timer Circuits

### T16 Transmit Mode

In Normal or Ping-Pong Mode, the output of T16, when not enabled, is dependent on CTR1, D0. If it is a 0, T16\_OUT is a 1; if it is a 1, T16\_OUT is 0. You can force the output of T16 to either a 0 or 1 whether it is enabled or not by programming CTR1 D3, D2 to a 10 or 11.

When T16 is enabled, TC16H \* 256 + TC16L is loaded, and T16\_OUT is switched to its initial value (CTR1 D0). When T16 counts down to 0, T16\_OUT is toggled (in Normal or Ping-Pong Mode), an interrupt is generated if enabled (CTR2 D1), and a status bit (CTR2 D5) is set.

► **Note:** Global interrupts override this function as described in “Interrupts” on page 62.

If T16 is in Single-Pass Mode, it is stopped at this point (see Figure 33). If it is in Modulo-N Mode, it is loaded with TC16H \* 256 + TC16L, and the counting continues (see Figure 34).



### If D6 of CTR2 Is 1

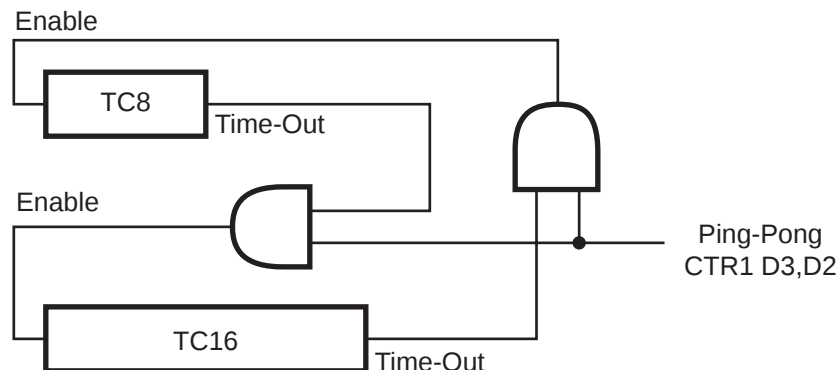
T16 ignores the subsequent edges in the input signal and continues counting down. A time out of T8 causes T16 to capture its current value and generate an interrupt if enabled (CTR2, D2). In this case, T16 does not reload and continues counting. If D6 bit of CTR2 is toggled (by writing a 0 and then a 1 to it), T16 captures and reloads on the next edge (rising, falling, or both, depending on CTR1 D5, D4) but continues to ignore subsequent edges.

When T16 reaches 0, it continues counting from FFFFh. Meanwhile, a status bit (CTR2 D5) is set, and an interrupt time-out can be generated if enabled (CTR2 D1).

### Ping-Pong Mode

This operation mode is only valid in transmit mode. T8 and T16 need to be programmed in Single-Pass Mode (CTR0 D6, CTR2 D6), and Ping-Pong Mode needs to be programmed in CTR1 D3, D2. You can begin the operation by enabling either T8 or T16 (CTR0 D7 or CTR2 D7). For example, if T8 is enabled, T8\_OUT is set to this initial value (CTR1 D1). According to T8\_OUT's level, TC8H or TC8L is loaded into T8. After the terminal count is reached, T8 is disabled and T16 is enabled. T16\_OUT switches to its initial value (CTR1 D0), data from TC16H and TC16L is loaded, and T16 starts to count. After T16 reaches the terminal count, it stops, T8 is enabled again, and the whole cycle repeats. Interrupts can be allowed when T8 or T16 reaches terminal control (CTR0 D1, CTR2 D1). To stop the Ping-Pong operation, write 00 to bits D3 and D2 of CTR1. See [Figure 35](#).

- **Note:** Enabling Ping-Pong operation while the counter/timers are running might cause intermittent counter/timer function. Disable the counter/timers and then reset the status flags before instituting this operation.



**Figure 35. Ping-Pong Mode**

### Starting Ping-Pong Mode

First, make sure both counter/timers are not running. Then set T8 into Single-Pass Mode (CTR0 D6), set T16 into Single-Pass Mode (CTR2 D6), and set Ping-Pong Mode (CTR1 D2, D3). These instructions do not have to be in any particular order. Finally, start Ping-Pong Mode by enabling either T8 (CTR0 D7) or T16 (CTR2 D7).

### During Ping-Pong Mode

The enable bits of T8 and T16 (CTR0 D7, CTR2 D7) are alternately set and cleared by hardware. The time-out bits (CTR0 D5, CTR2 D5) are set every time the counter/timers reach the terminal count.

### Output Circuit

Figure 36 shows the output circuit.

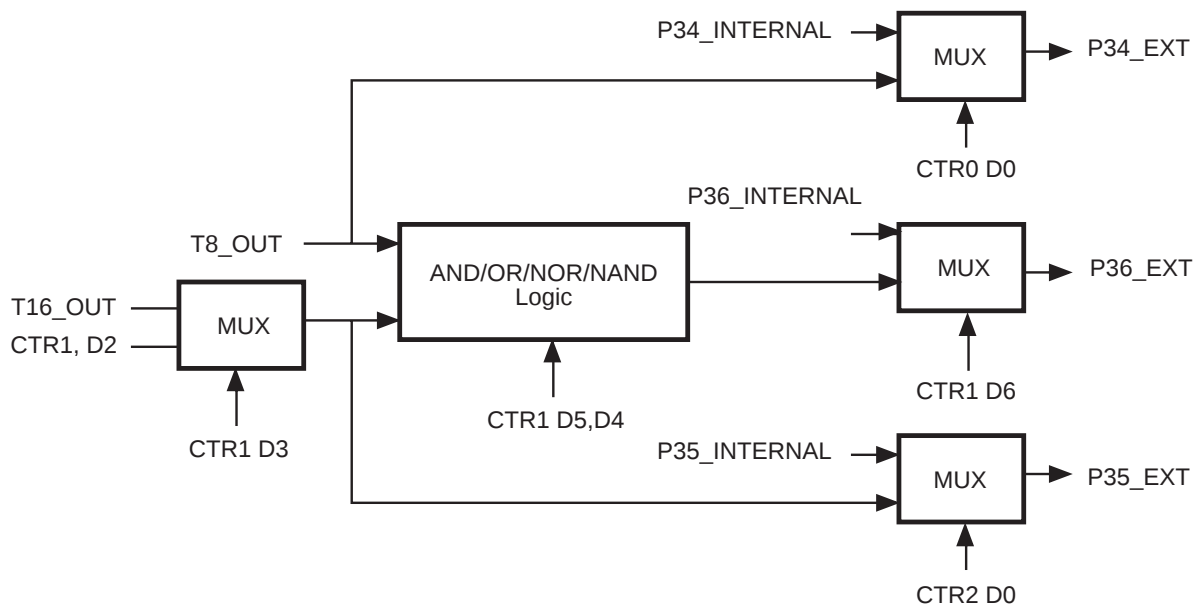
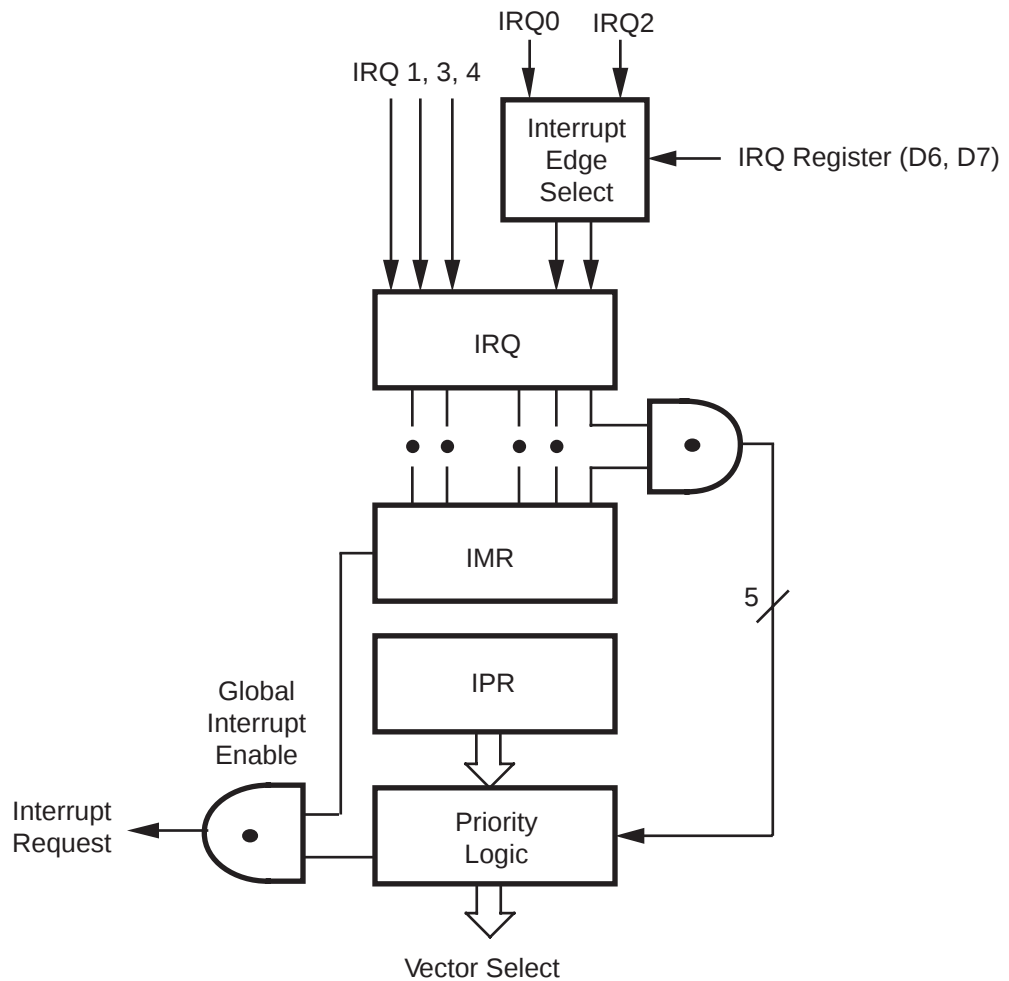


Figure 36. Output Circuit

### Interrupts

The Z86E7X has five different interrupts. The interrupts are maskable and prioritized, as shown in Figure 37. The five sources are divided as follows: three sources are claimed by Port 3 lines P33–P31 and the remaining two by the counter/timers (see Table 26). The Interrupt Mask Register globally or individually enables or disables the five interrupt requests.



**Figure 37. Interrupt Block Diagram**

**Table 26. Interrupt Types, Sources, and Vectors**

| Name | Source                       | Vector Location | Comments                                      |
|------|------------------------------|-----------------|-----------------------------------------------|
| IRQ0 | /DAV0, IRQ0                  | 0, 1            | External (P32), Rising Falling Edge Triggered |
| IRQ1 | IRQ1                         | 2, 3            | External (P33), Falling Edge Triggered        |
| IRQ2 | /DAV2, IRQ2, T <sub>IN</sub> | 4, 5            | External (P31), Rising Falling Edge Triggered |
| IRQ3 | T16                          | 6, 7            | Internal                                      |
| IRQ4 | T8                           | 8, 9            | Internal                                      |

When more than one interrupt is pending, priorities are resolved by a programmable priority encoder controlled by the Interrupt Priority register. An interrupt machine cycle is activated when an interrupt request is granted. This disables all subsequent interrupts, saves the Program Counter and Status Flags, and then branches to the program memory vector location reserved for that interrupt. All Z86E7X interrupts are vectored through locations in the program memory. This memory location and the next byte contain the 16-bit address of the interrupt service routine for that particular interrupt request. To accommodate polled interrupt systems, interrupt inputs are masked and the Interrupt Request register is polled to determine which of the interrupt requests need service.

An interrupt resulting from AN1 is mapped into IRQ2, and an interrupt from AN2 is mapped into IRQ0. Interrupts IRQ2 and IRQ0 can be rising, falling, or both edge triggered and are programmable by the user. The software can poll to identify the state of the pin.

Programming bits for the Interrupt Edge Select are located in the IRQ Register (R250), bits D7 and D6. The configuration is indicated in [Table 27](#).

**Table 27. IRQ Register**

| IRQ |    | Interrupt Edge |            |
|-----|----|----------------|------------|
| D7  | D6 | IRQ2 (P31)     | IRQ0 (P32) |
| 0   | 0  | F              | F          |
| 0   | 1  | F              | R          |
| 1   | 0  | F              | F          |
| 1   | 1  | R/F            | R/F        |

Notes:

F = Falling Edge

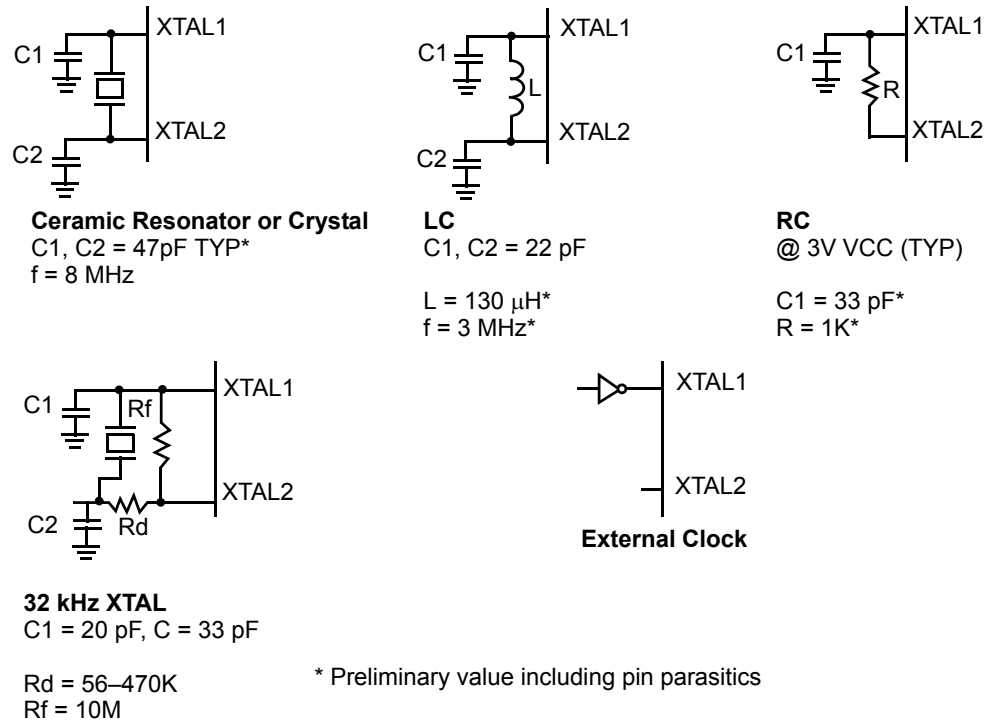
R = Rising Edge

In analog mode, the Stop-Mode Recovery sources selected by the SMR register are connected to the IRQ1 input. Any of the Stop-Mode Recovery sources for SMR (except P31, P32, and P33) can be used to generate IRQ1 (falling edge triggered).

## Clock

The Z86E7X on-chip oscillator has a high-gain, parallel-resonant amplifier for connection to a crystal, LC, ceramic resonator, or any suitable external clock source (XTAL1 = Input, XTAL2 = Output). The crystal must be AT cut, 1 MHz to 8 MHz maximum, with a series resistance (RS) less than or equal to 100 Ohms. The Z86E7X on-chip oscillator can be driven with a cost-effective RC network or other suitable external clock source.

The crystal must be connected across XTAL1 and XTAL2 using the recommended capacitors (capacitance greater than or equal to 22 pF) from each pin to ground. The RC oscillator configuration is an external resistor connected from XTAL1 to XTAL2, with a frequency-setting capacitor from XTAL1 to ground (see Figure 38).



**Figure 38. Oscillator Configuration**

## Power-On Reset (POR)

A timer circuit clocked by a dedicated on-board RC oscillator is used for the Power-On Reset (POR) timer function. The POR time allows VCC and the oscillator circuit to stabilize before instruction execution begins.

The POR timer circuit is a one-shot timer triggered by one of three conditions:

- Power Fail to Power OK status.
- Stop-Mode Recovery (if D5 of SMR = 1).
- WDT Time-Out.

The POR time is a nominal 5 ms. Bit 5 of the Stop-Mode Register determines whether the POR timer is bypassed after Stop-Mode Recovery (typical for external clock, RC, and LC oscillators).

## HALT

HALT turns off the internal CPU clock, but not the XTAL oscillation. The counter/timers and external interrupts IRQ0, IRQ1, IRQ2, IRQ3, and IRQ4 remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT Mode. After the interrupt service routine, the program continues from the instruction after the HALT.

## STOP

This instruction turns off the internal clock and external crystal oscillation and reduces the standby current to 10  $\mu$ A (typical) or less. STOP Mode is terminated only by a reset, such as WDT time-out, POR, SMR, or external reset. This causes the processor to restart the application program at address 000CH. To enter STOP (or HALT) mode, you need to first flush the instruction pipeline to avoid suspending execution in mid-instruction. To do this, you must execute a NOP (op code = FFH) immediately before the appropriate sleep instruction. For example:

```
FF      NOP      ; clear the pipeline
6F      STOP     ; enter STOP Mode
```

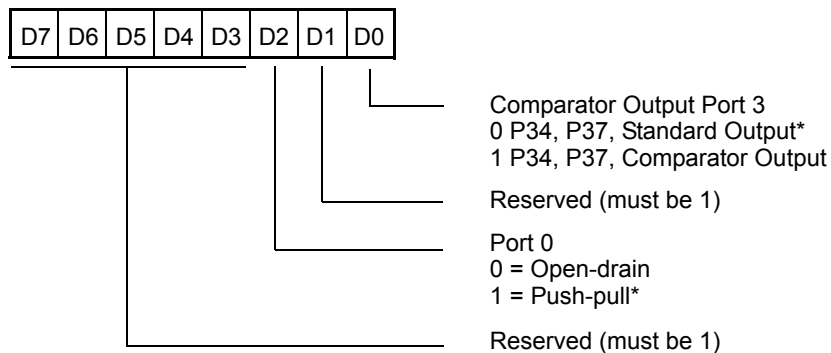
or

```
FF      NOP      ; clear the pipeline
7F      HALT     ; enter HALT Mode
```

## Port Configuration Register (PCON)

The PCON register ([Figure 39](#)) configures the comparator output on Port 3. It is located in the expanded register file at Bank F, location 00.

PCON (0F) 0H



\*Default setting after reset

**Figure 39. Port Configuration Register (PCON)—Write Only**

**Comparator Output Port 3 (D0)**

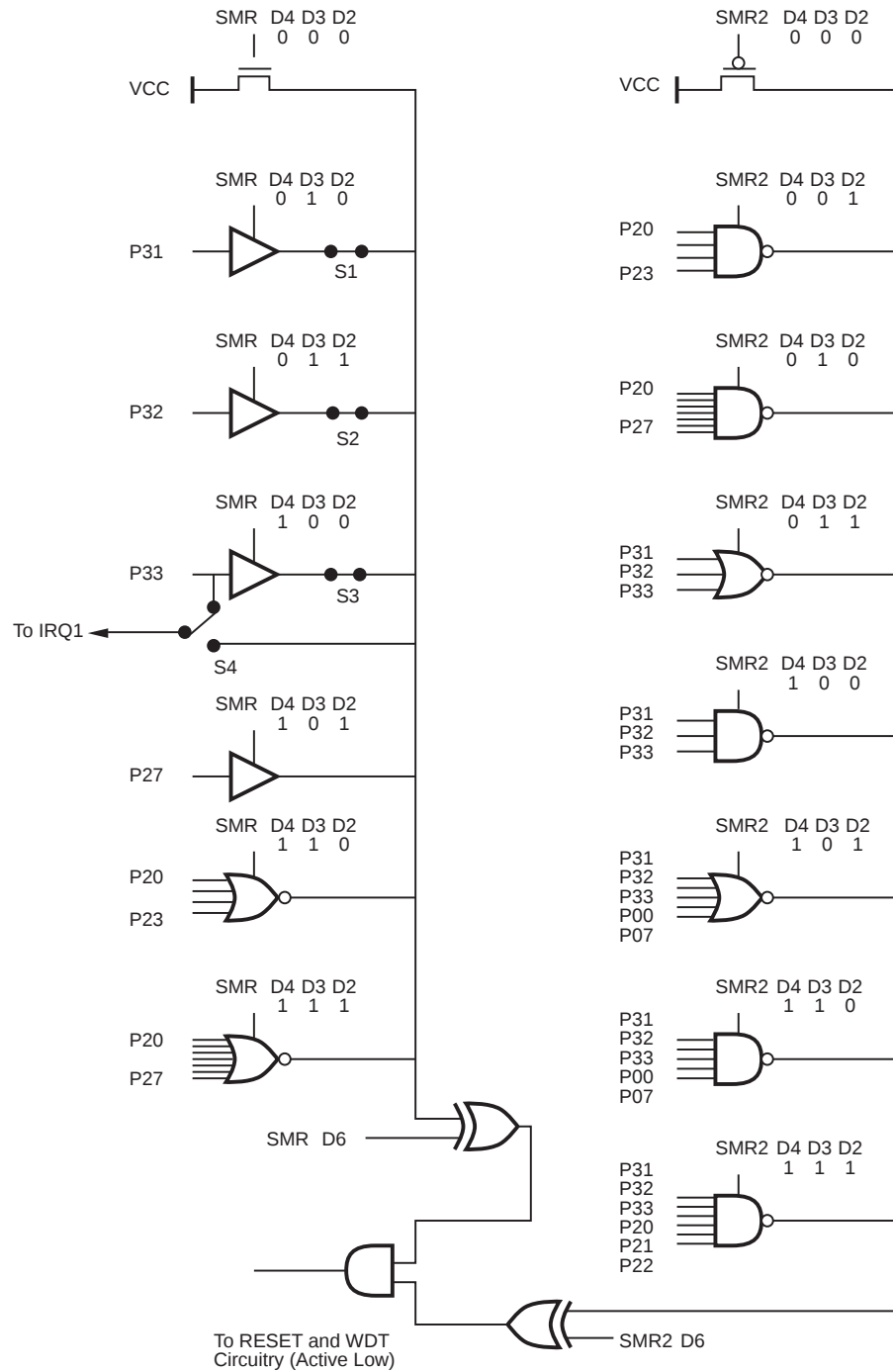
Bit 0 controls the comparator used in Port 3. A 1 in this location brings the comparator outputs to P34 and P37, and a 0 releases the port to its standard I/O configuration.

**Port 0 Output Mode (D2)**

Bit 2 controls the output mode of Port 0. A 1 in this location sets the output to push-pull, and a 0 sets the output to open-drain.

**Stop-Mode Recovery Register (SMR)**

This register selects the clock divide value and determines the mode of Stop-Mode Recovery ([Figure 40](#)). All bits are write only except bit 7, which is read only. Bit 7 is a flag bit that is hardware set on the condition of STOP recovery and reset by a power-on cycle. Bit 6 controls whether a low level or a high level is required from the recovery source. Bit 5 controls the reset delay after recovery. Bits D2, D3, and D4 of the SMR register specify the source of the Stop-Mode Recovery signal. Bit D0 determines if SCLK/TCLK are divided by 16 or not. The SMR is located in Bank F of the Expanded Register Group at address 0BH.



**Figure 40. Stop-Mode Recovery Register**

### SCLK/TCLK Divide-by-16 Select (D0)

D0 of the SMR controls a Divide-by-16 prescaler of SCLK/TCLK (Figure 41). The purpose of this control is to selectively reduce device power consumption during normal processor execution (SCLK control) and/or HALT Mode (where TCLK sources interrupt logic). After Stop-Mode Recovery, this bit is set to a 0.

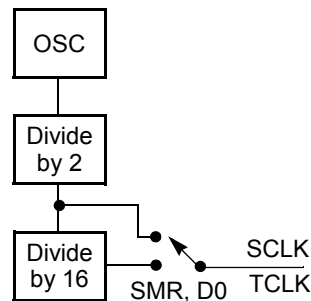


Figure 41. SCLK Circuit

### Stop-Mode Recovery Source (D2, D3, and D4)

These three bits of the SMR specify the wake-up source of the STOP recovery (Figure 40 on page 68 and Table 28).

Table 28. Stop-Mode Recovery Source

| SMR:432 |    |    | Operation                          |
|---------|----|----|------------------------------------|
| D4      | D3 | D2 | Description of Action              |
| 0       | 0  | 0  | POR and/or external reset recovery |
| 0       | 0  | 1  | Reserved                           |
| 0       | 1  | 0  | P31 transition                     |
| 0       | 1  | 1  | P32 transition                     |
| 1       | 0  | 0  | P33 transition                     |
| 1       | 0  | 1  | P27 transition                     |
| 1       | 1  | 0  | Logical NOR of P20 through P23     |
| 1       | 1  | 1  | Logical NOR of P20 through P27     |

► **Note:** Any Port 2 bit defined as an output drives the corresponding input to the default state to allow the remaining inputs to control the AND/OR function. Refer to “Stop-Mode Recovery Register 2 (SMR2)” on page 71 for other recovery sources.

### **Stop-Mode Recovery Delay Select (D5)**

This bit, if low, disables the 5 ms /RESET delay after Stop-Mode Recovery. The default configuration of this bit is one. If the “fast” wake up is selected, the Stop-Mode Recovery source needs to be kept active for at least 5TpC.

### **Stop-Mode Recovery Edge Select (D6)**

A 1 in this bit position indicates that a High level on any one of the recovery sources wakes the Z86E7X from STOP Mode. A 0 indicates Low level recovery. The default is 0 on POR.

### **Cold or Warm Start (D7)**

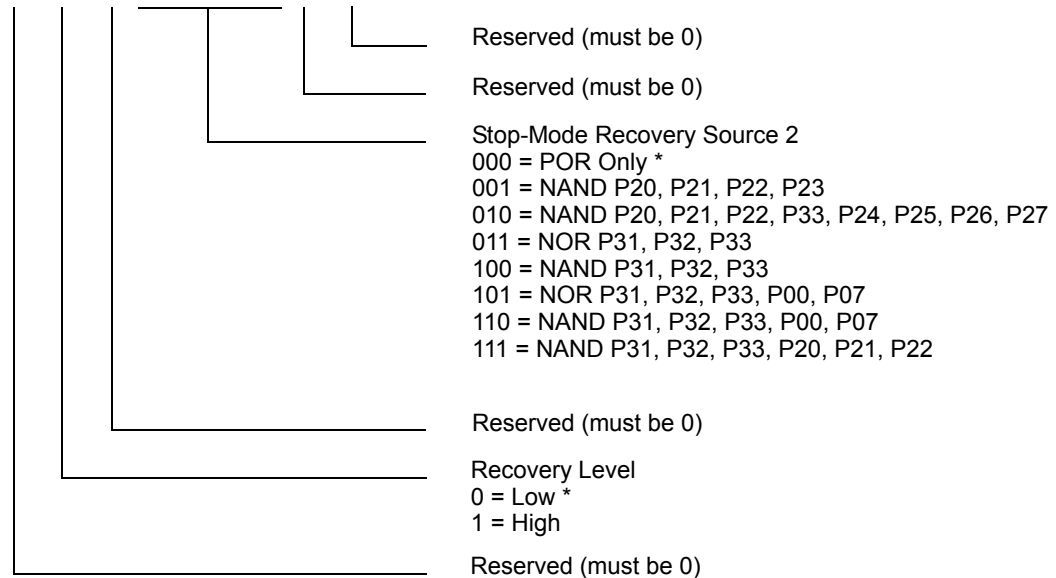
This bit is set by the device upon entering STOP Mode. It is a read-only Flag bit. A 1 in D7 (warm) indicates that the device awakes from a SMR source or a WDT while in STOP Mode. A 0 in this bit (cold) indicates that the device is reset by a POR or WDT while not in STOP Mode.

## Stop-Mode Recovery Register 2 (SMR2)

This register (see [Figure 42](#)) determines the mode of STOP Mode recovery for SMR2.

SMR2 (0F) DH

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|



\* Default setting after reset

Note: If used in conjunction with SMR, either of the two specified events causes a Stop-Mode Recovery.

**Figure 42. Stop-Mode Recovery Register 2—(0F) DH: D2–D4, D6 Write Only**

If SMR2 is used in conjunction with SMR, either of the specified events causes a Stop-Mode Recovery.

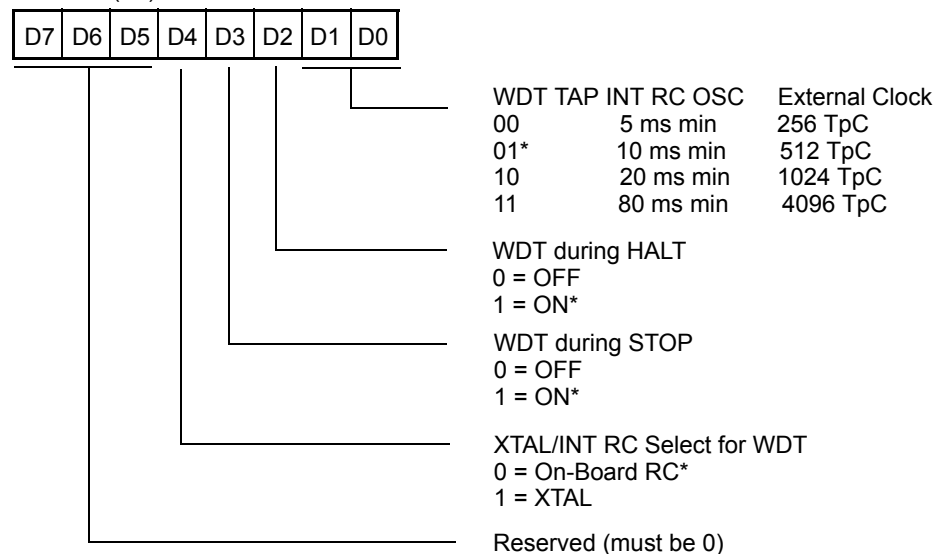
- **Note:** Port pins configured as outputs are ignored as a SMR or SMR2 recovery source. For example, if the NAND of P23–P20 is selected as the recovery source and P20 is configured as an output, the remaining SMR pins (P23–P21) form the NAND equation.

## Watch-Dog Timer Mode Register (WDTMR)

The WDT is a retriggerable one-shot timer that resets the Z8 if it reaches its terminal count. The WDT must initially be enabled by executing the WDT instruction and refreshed on subsequent executions of the WDT instruction. The WDT circuit is driven by an on-board RC oscillator or external oscillator from the XTAL1 pin. The WDT instruction affects the Zero (Z), Sign (S), and Overflow (V) flags.

The POR clock source is selected with bit 4 of the WDT register. Bit 0 and 1 control a tap circuit that determines the time-out period. Bit 2 determines whether the WDT is active during HALT, and Bit 3 determines WDT activity during STOP. Bits 5 through 7 are reserved. See [Figure 43](#).

WDTMR (0F) FH



\* Default setting after reset

**Figure 43. Watch-Dog Timer Mode Register—Write Only**

This register is accessible only during the first 60 processor cycles (SCLK) from the execution of the first instruction after Power-On-Reset, Watch-Dog Reset, or a Stop-Mode Recovery ([Figure 40](#) on page 68). After this point, the register cannot be modified by any means, intentional or otherwise. The WDTMR cannot be read and is located in Bank F of the Expanded Register Group at address location 0FH. It is organized as shown in [Figure 43](#).

### WDT Time Select (D0, D1)

This bit selects the WDT time period. It is configured as shown in [Table 29](#).

**Table 29. WDT Time Select**

| D1 | D0 | Time-Out of Internal RC OSC | Time-Out of XTAL Clock |
|----|----|-----------------------------|------------------------|
| 0  | 0  | 5 ms min                    | 256 TpC                |
| 0  | 1  | 10 ms min                   | 512 TpC                |
| 1  | 0  | 20 ms min                   | 1024 TpC               |
| 1  | 1  | 80 ms min                   | 4096 TpC               |

Notes:

TpC = XTAL clock cycle

The default on reset is 10 ms.

### WDTMR During HALT (D2)

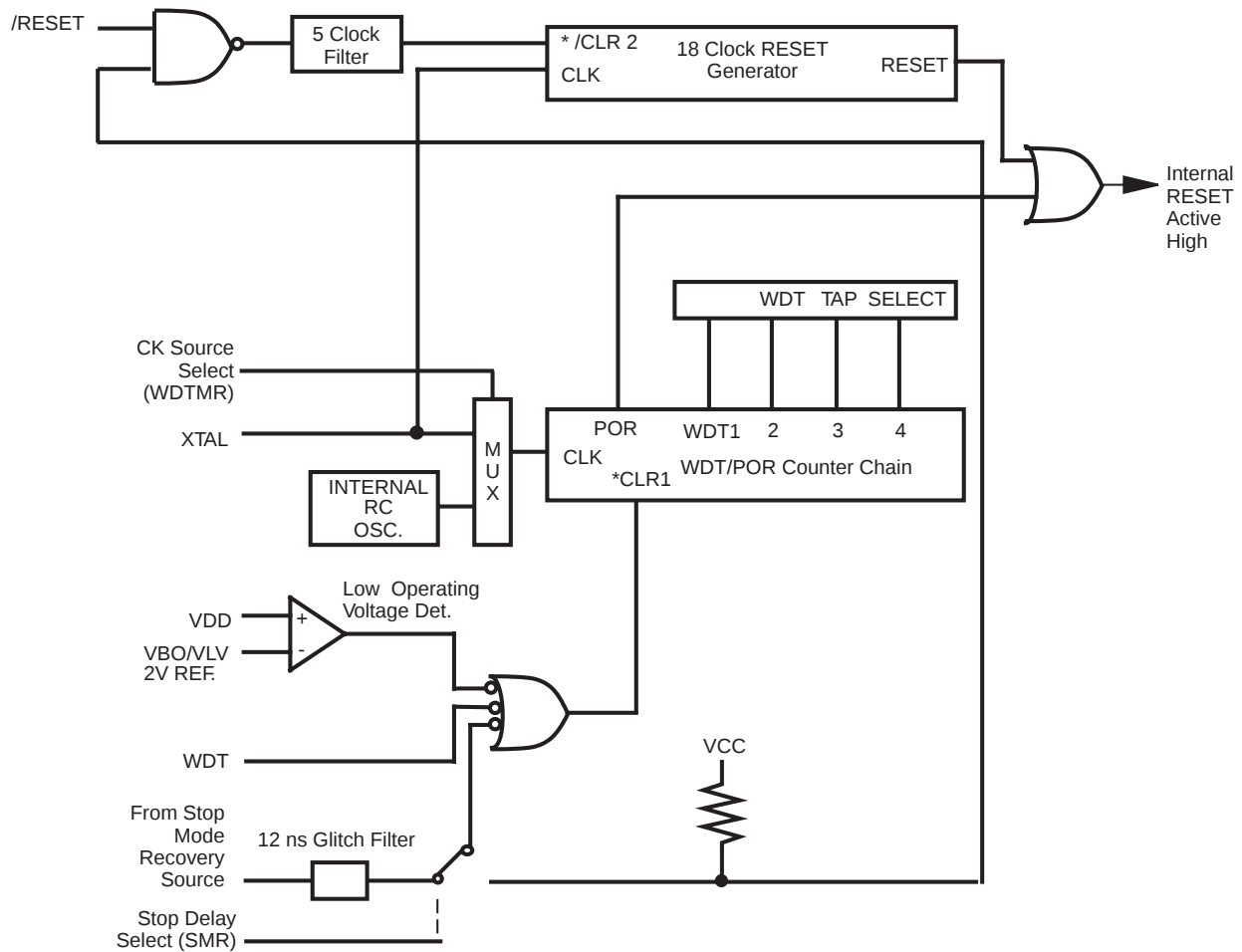
This bit determines whether or not the WDT is active during HALT Mode. A 1 indicates active during HALT. The default is 1.

### WDTMR During STOP (D3)

This bit determines whether or not the WDT is active during STOP Mode. Since the XTAL clock is stopped during STOP Mode, the on-board RC has to be selected as the clock source to the WDT/POR counter. A 1 indicates active during STOP. The default is 1.

### Clock Source for WDT (D4)

This bit determines which oscillator source is used to clock the internal POR and WDT counter chain. If the bit is a 1, the internal RC oscillator is bypassed, and the POR and WDT clock source is driven from the external pin, XTAL1. The default configuration of this bit is 0, which selects the RC oscillator. See [Figure 44](#).



\*  $\overline{\text{CLR1}}$  and  $\overline{\text{CLR2}}$  enable the WDT/POR and 18 Clock Reset timers upon a Low to High input translation.

**Figure 44. Resets and WDT**

## Low-Voltage Protection

An on-board Voltage Comparator checks that  $V_{CC}$  is at the required level to ensure correct operation of the device. Reset is globally driven if  $V_{CC}$  is below  $V_{LV}$  (Low Voltage). The minimum operating voltage varies with the temperature and operating frequency, while  $V_{LV}$  varies with temperature only.

- **Note:** The LVD flag will be valid after enabling the detection for 20  $\mu\text{S}$  (design estimation, not tested in production). LVD does not work at STOP mode. It must be disabled during STOP mode in order to reduce current.

## Software-Selectable Options

There are four Software-Selectable Options to choose from based on the ROM-based parts mask options. Register (F0) EH OTP byte is where these options are controlled. These options are listed in [Table 30](#).

**Table 30. Software-Selectable Options**

| Bit Name                       | Reg(F0)EH |
|--------------------------------|-----------|
| Port 0 Pull-ups (lower nibble) | On/Off    |
| Port 0 Pull-ups (upper nibble) | On/Off    |
| Port 2 Pull-ups                | On/Off    |
| Mouse/Normal                   | M/N       |

► **Note:** The RC oscillator Xtal1/2 option is invoked during OTP programming as a user-selectable item.

## Low-Voltage Detection

The device functions normally above 3.0 V under all conditions. The minimum functionality point below 3 V is to be defined. The  $V_{LV}$  is a function of temperature and process parameters. The device is forced into reset when  $V_{CC}$  drops below the  $V_{LV}$  voltage level.

## EPROM Programming

Table 31 describes the programming and test modes.

**Table 31. Programming and Test Modes**

| User/Test Mode<br>Device Pin #<br>User Modes | Device Pins            |                 |                 |                 |                 |      | Port 1<br>CNFG<br>DATA | Test<br>ADDR<br>A0–A3 | Note |
|----------------------------------------------|------------------------|-----------------|-----------------|-----------------|-----------------|------|------------------------|-----------------------|------|
|                                              | P33<br>V <sub>PP</sub> | P32<br>EPM      | Pref1<br>/CE    | P31<br>/OE      | P20<br>/PGM     | Addr | V <sub>CC</sub>        |                       |      |
| EPROM Read                                   | V <sub>CC</sub>        | V <sub>H</sub>  | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | Addr | 3.0 V                  | Out                   | XX   |
| Program                                      | V <sub>PP</sub>        | V <sub>CC</sub> | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | Addr | 6.0 V                  | In                    | XX   |
| Program Verify                               | V <sub>PP</sub>        | V <sub>CC</sub> | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | Addr | 6.0 V                  | Out                   | XX   |
| RC Option                                    | V <sub>PP</sub>        | V <sub>CC</sub> | V <sub>H</sub>  | V <sub>IH</sub> | V <sub>IL</sub> | XX   | 6.0 V                  | XX                    | XX   |
| Margin Read                                  | V <sub>VA</sub>        | V <sub>H</sub>  | V <sub>IL</sub> | V <sub>H</sub>  | V <sub>IH</sub> | Addr | 6.0 V                  | Out                   | 00 1 |
| Shadow Row Rd                                | V <sub>CC</sub>        | V <sub>H</sub>  | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | COL  | 3.0 V                  | Out                   | 01 1 |
| Shadow Row Prg                               | V <sub>PP</sub>        | V <sub>H</sub>  | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | COL  | 6.0 V                  | In                    | 01 1 |
| Shadow Row Ver                               | V <sub>PP</sub>        | V <sub>H</sub>  | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | COL  | 6.0 V                  | Out                   | 01 1 |
| Shadow Col Rd                                | V <sub>CC</sub>        | V <sub>H</sub>  | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | ROW  | 3.0 V                  | Out                   | 02 1 |
| Shadow Col Prg                               | V <sub>PP</sub>        | V <sub>H</sub>  | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | ROW  | 6.0 V                  | In                    | 03 1 |
| Shadow Col Ver                               | V <sub>PP</sub>        | V <sub>H</sub>  | V <sub>IL</sub> | V <sub>IL</sub> | V <sub>IH</sub> | ROW  | 6.0 V                  | Out                   | 02 1 |
| Page Prg 2 Byte                              | V <sub>PP</sub>        | V <sub>H</sub>  | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | TBD  | 6.0 V                  | In                    | 04 1 |
| Page Prg 4 Byte                              | V <sub>PP</sub>        | V <sub>H</sub>  | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | TBD  | 6.0 V                  | In                    | 05 1 |
| Page Prg 8 Byte                              | V <sub>PP</sub>        | V <sub>H</sub>  | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | TBD  | 6.0 V                  | In                    | 06 1 |
| Page Prg 16 Byte                             | V <sub>PP</sub>        | V <sub>H</sub>  | V <sub>IL</sub> | V <sub>IH</sub> | V <sub>IL</sub> | TBD  | 6.0 V                  | In                    | 07 1 |

Notes:

1. All test modes are entered by first setting up the corresponding test address and then latching the address by bringing the /OE to V<sub>H</sub> and then to V<sub>IL</sub>, except for the margin read which requires /OE to be kept at V<sub>H</sub>.

V<sub>VA</sub> = Variable from V<sub>CC</sub> to V<sub>PP</sub>

V<sub>PP</sub> = 12.5 V ± 0.5 V

V<sub>H</sub> = 12.5 V ± 0.5 V

V<sub>IH</sub> = 3 V

V<sub>IL</sub> = 0 V

XX = Irrelevant

I<sub>PP</sub> during programming = 40 mA maximum

I<sub>CC</sub> during programming, verify, or read = 40 mA maximum.

Table 32 lists the timing of the programming waveform.

**Table 32. Timing of Programming Waveform**

| Parameters | Name                       | Min  | Max | Units |
|------------|----------------------------|------|-----|-------|
| 1          | Address Setup Time         | 2    |     | μs    |
| 2          | Data Setup Time            | 2    |     | μs    |
| 3          | V <sub>PP</sub> Setup Time | 2    |     | μs    |
| 4          | V <sub>CC</sub> Setup Time | 2    |     | μs    |
| 5          | Chip Enable Setup Time     | 2    |     | μs    |
| 6          | Program Pulse Width        | 0.95 |     | μs    |
| 7          | Data Hold Time             | 2    |     | μs    |
| 8          | /OE Setup Time             | 2    |     | μs    |
| 9          | Data Access Time           |      | 200 | ns    |
| 10         | Data Output Float Time     |      | 100 | ns    |
| 11         | Overprogram Pulse Width    | 2.85 |     | ms    |
| 12         | EPM Setup Time             | 2    |     | μs    |
| 13         | /PGM Setup Time            | 2    |     | μs    |
| 14         | Address to /OE Setup Time  | 2    |     | μs    |
| 15         | Option Program Pulse Width | 78   |     | ms    |

Figure 45 shows the EPROM read timing diagram. Figure 46 on page 79 shows the EPROM program and verify timing diagram. Figure 47 on page 80 shows the programming EPROM, RAM protect, and 16K size selection timing diagram.

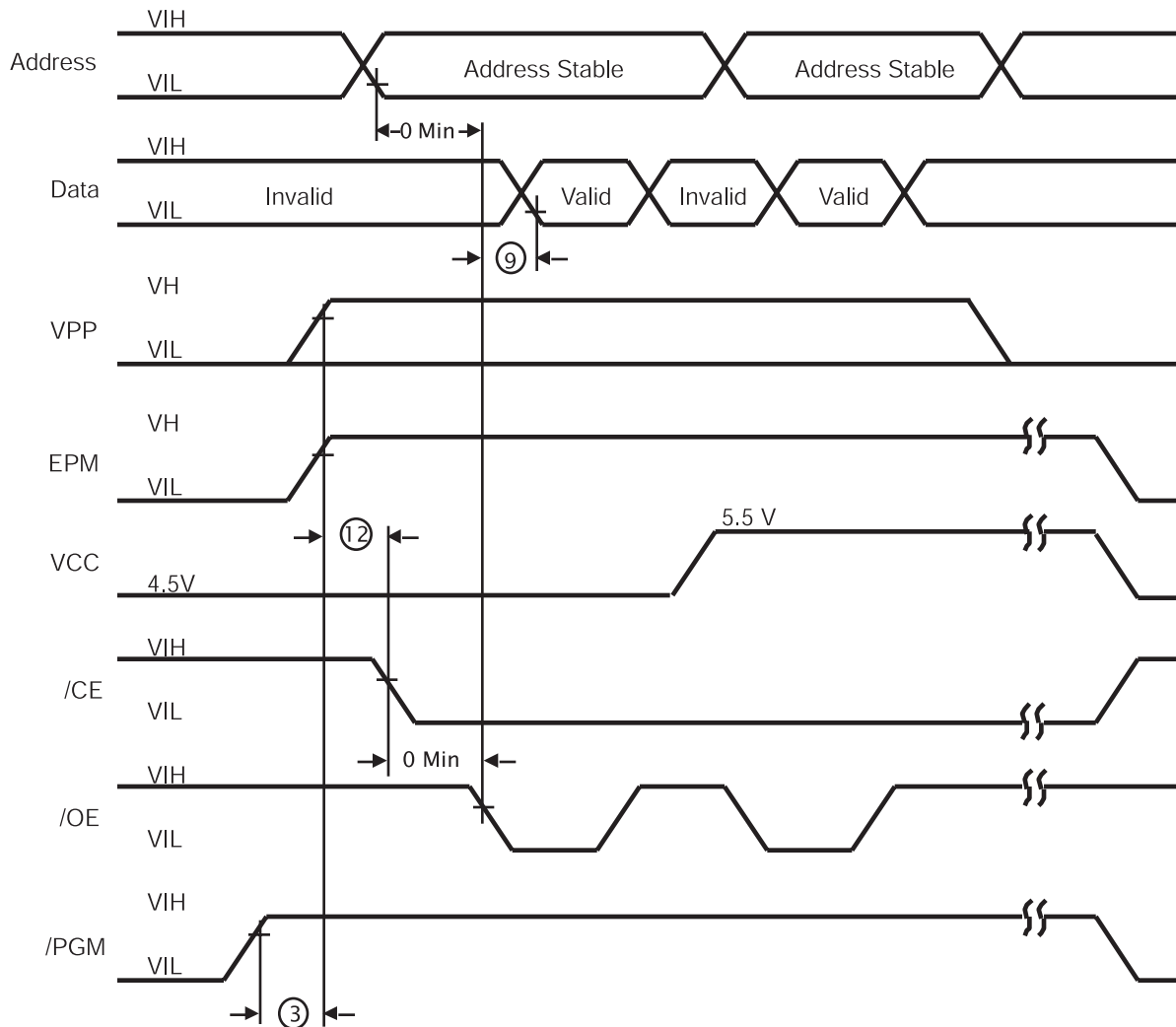


Figure 45. EPROM Read

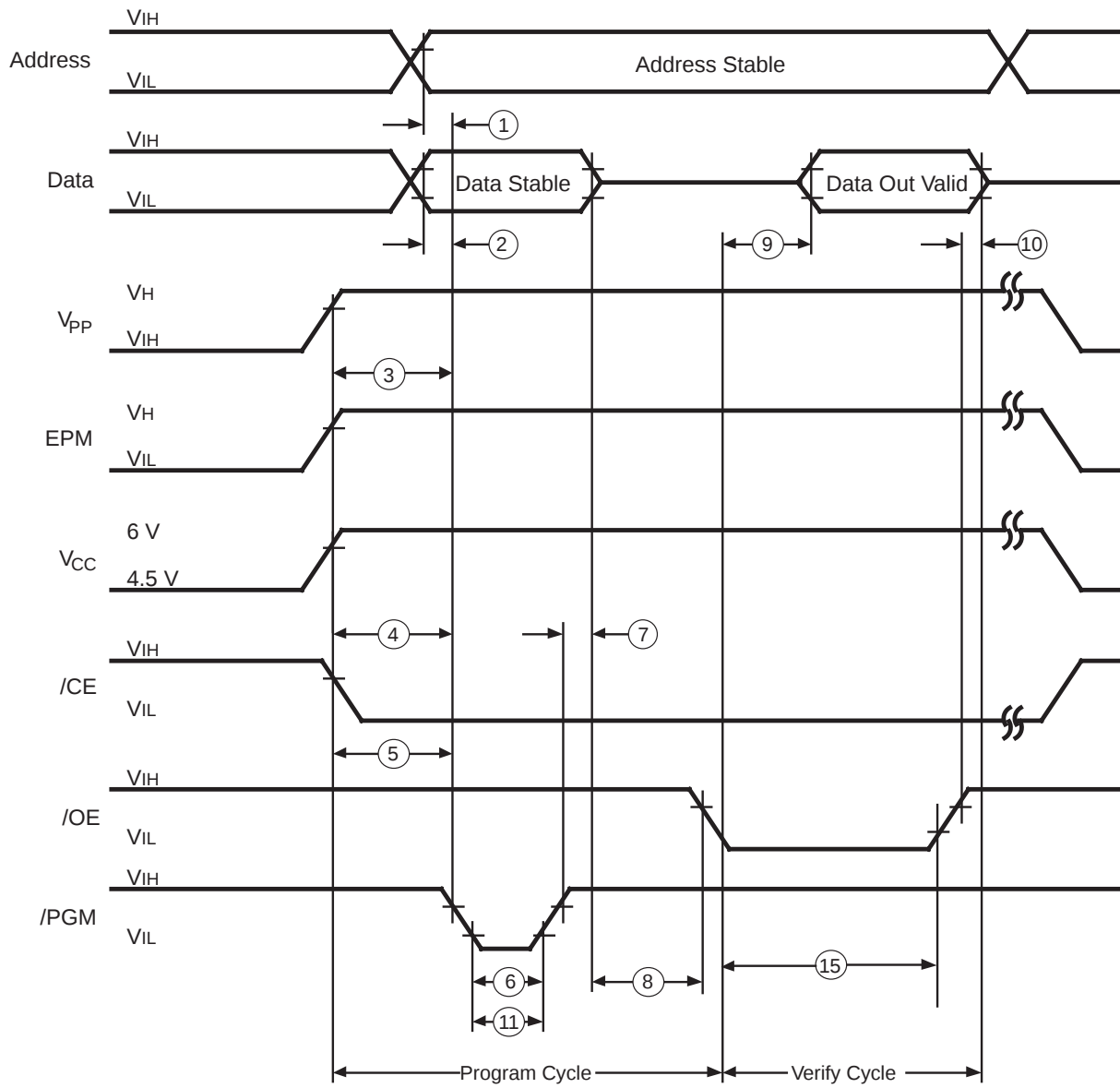
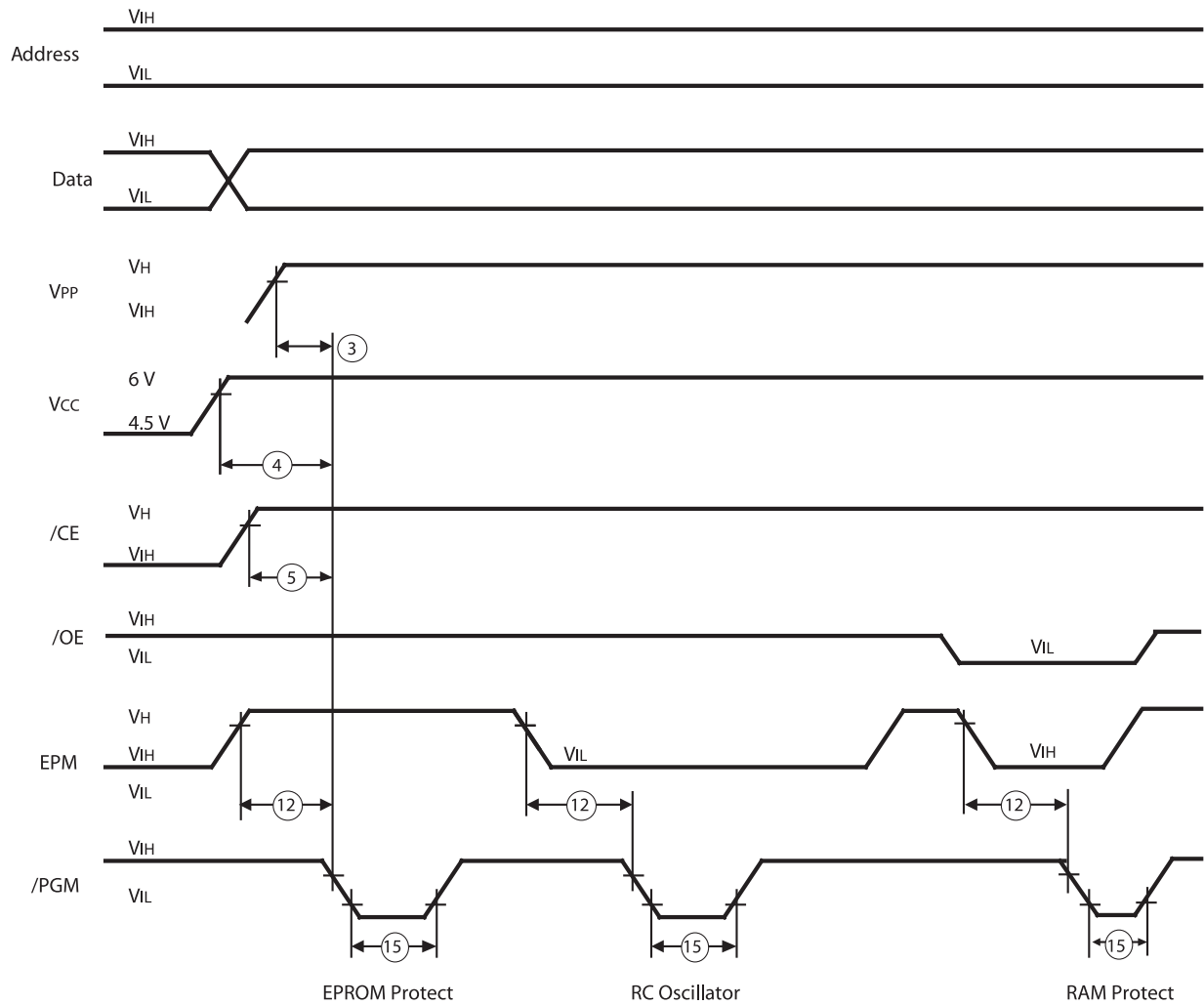


Figure 46. EPROM Program and Verify



**Figure 47. Programming EPROM, RAM Protect, and 16K Size Selection**

Figure 48 shows the programming flowchart.

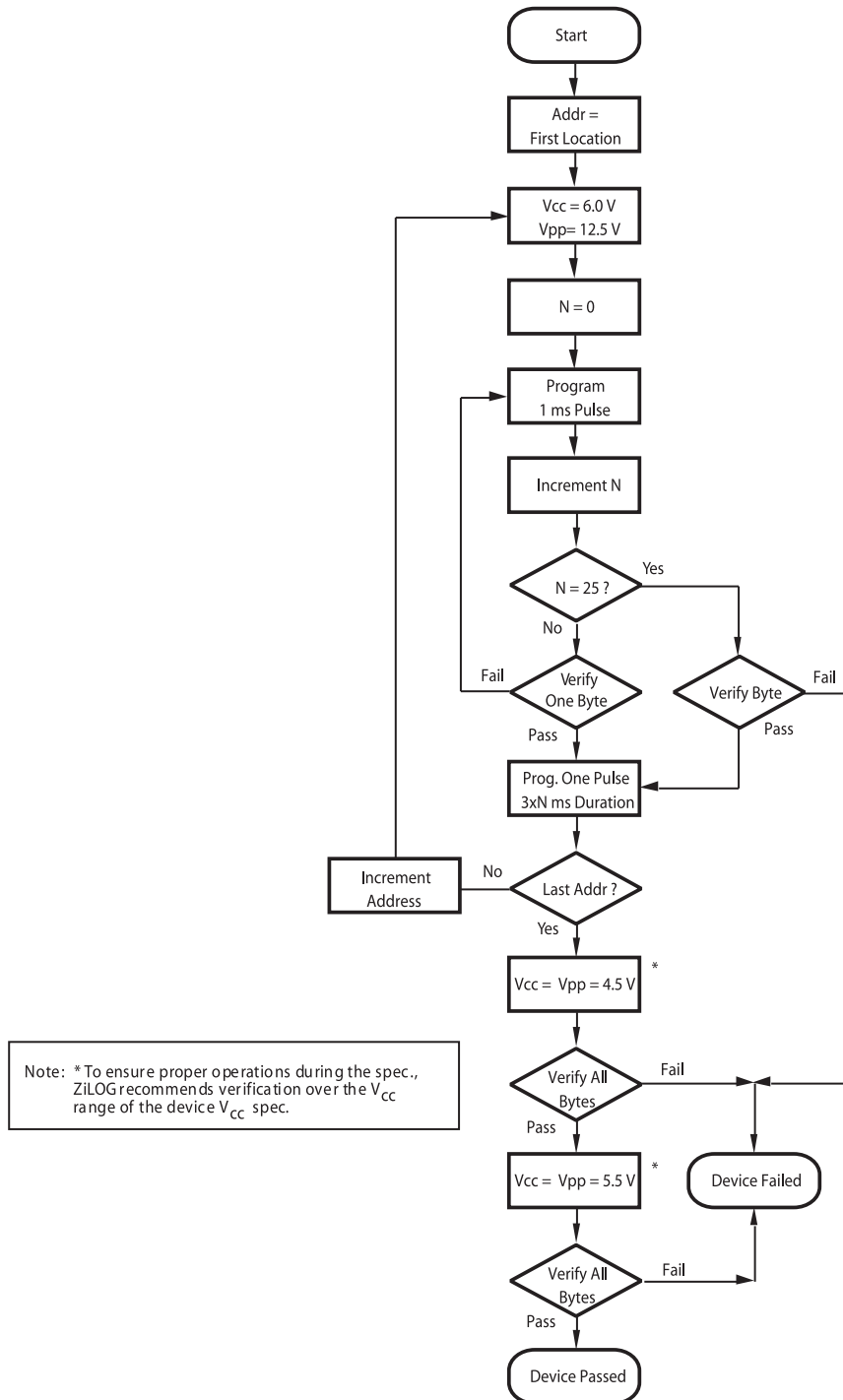


Figure 48. Programming Flowchart

## Expanded Register File Control Registers (0D)

Figure 49 through Figure 51 show the expanded register file control registers (0D).

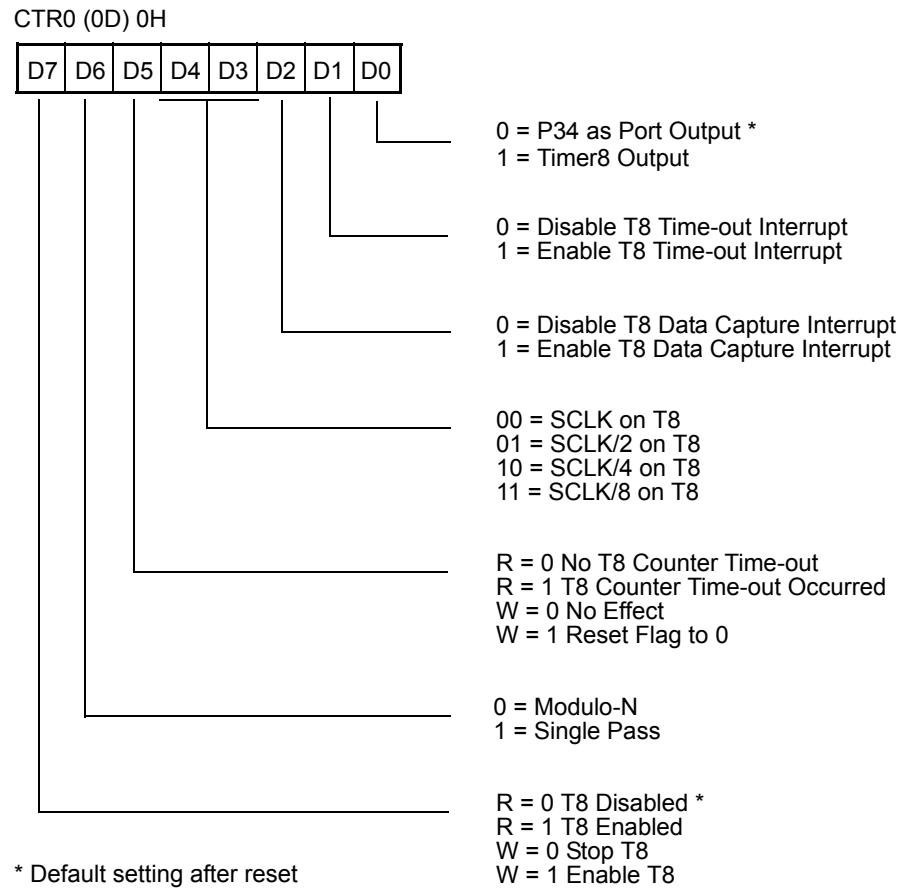
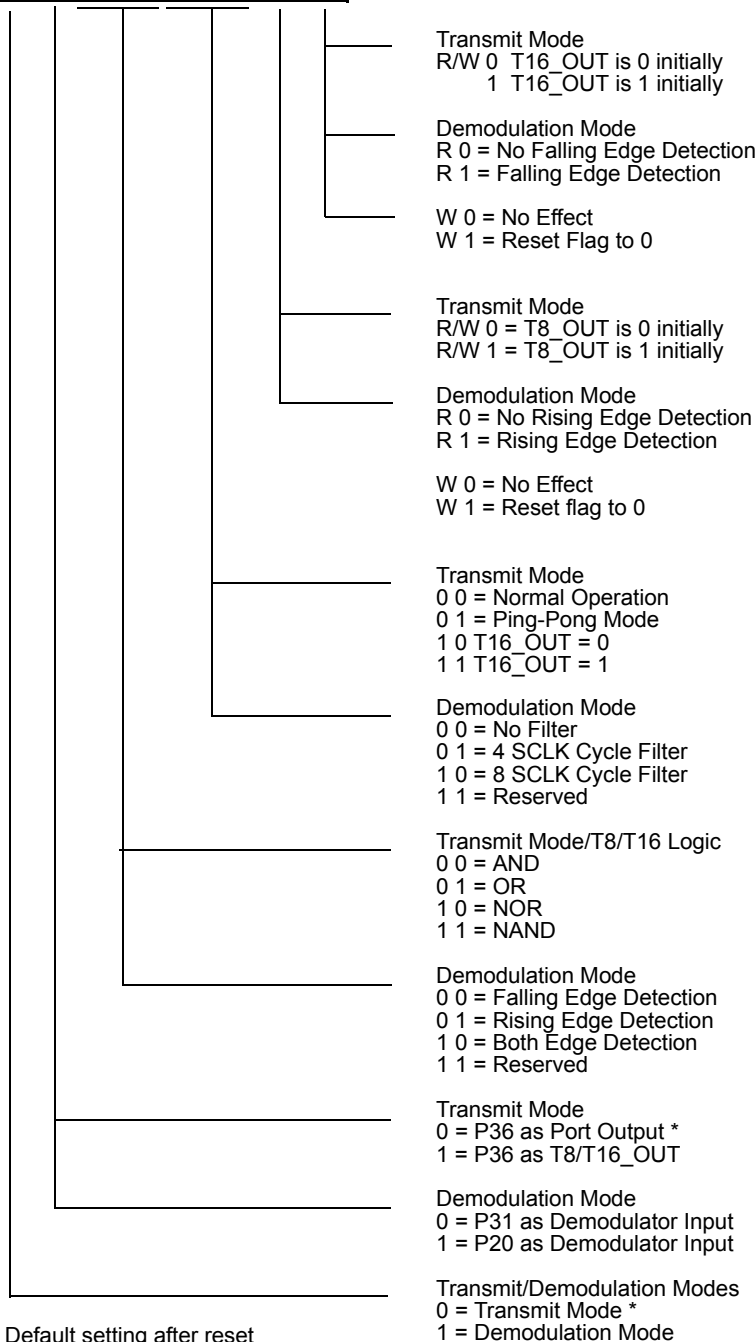


Figure 49. TC8 Control Register—(0D) 0H: Read/Write Except Where Noted

CTR1 (0D) 1H

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|



\* Default setting after reset

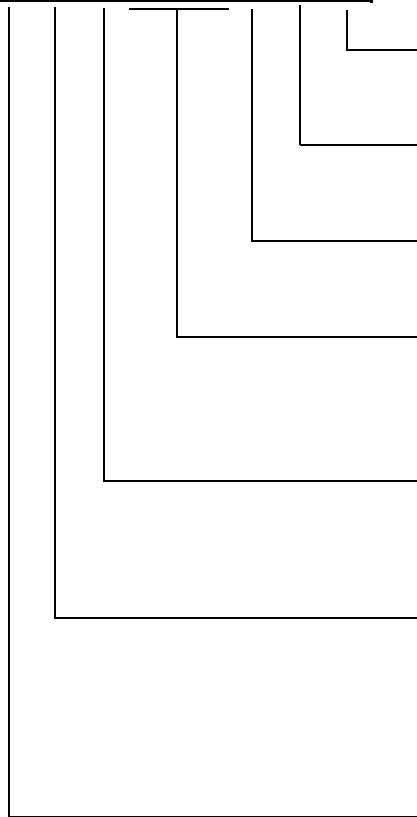
Note: Care must be taken in differentiating transmit mode from demodulation mode. Depending on which of these two modes is operating, the CTR1 bit has different functions.

Note: Changing from one mode to another cannot be done without disabling the counter/timers.

Figure 50. T8 and T16 Common Control Functions—(0D) 1H: Read/Write

CTR2 (0D) 02H

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|



0 = P35 is Port Output \*  
1 = P35 is TC16 Output

0 = Disable T16 Time-out Interrupt  
1 = Enable T16 Time-out Interrupt

0 = Disable T16 Data Capture Interrupt  
1 = Enable T16 Data Capture Interrupt

00 = SCLK on T16  
01 = SCLK/2 on T16  
10 = SCLK/4 on T16  
11 = SCLK/8 on T16

R = 0 No T16 Time-out  
R = 1 T16 Time-out Occurs  
W = 0 No Effect  
W = 1 Reset Flag to 0

Transmit Mode  
0 = Modulo-N for T16  
1 = Single Pass for T16

Demodulator Mode  
0 = T16 Recognizes Edge  
1 = T16 Does Not Recognize Edge

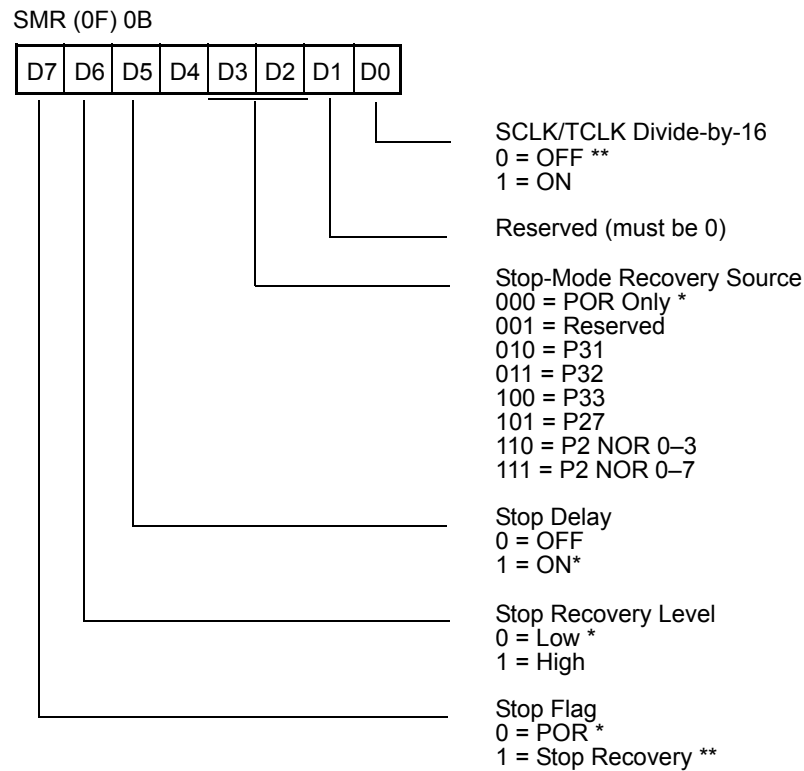
R = 0 T16 Disabled \*  
R = 1 T16 Enabled  
W = 0 Stop T16  
W = 1 Enable T16

\* Default setting after reset

**Figure 51. T16 Control Register—(0D) 2H: Read/Write Except Where Noted**

## Expanded Register File Control Registers (0F)

Figure 52 through Figure 57 show the expanded register file control registers (0F).



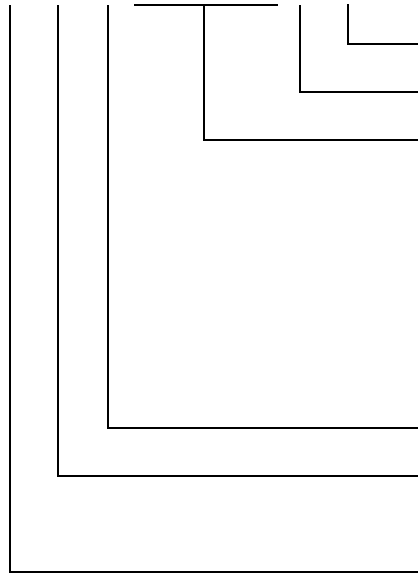
\* Default setting after reset

\*\* Default setting after reset and Stop-Mode Recovery

**Figure 52. Stop-Mode Recovery Register—(F) 0BH: D6–D0=Write Only, D7=Read Only**

SMR2 (0F) DH

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|----|----|----|----|----|----|----|----|
|----|----|----|----|----|----|----|----|



Reserved (must be 0)

Reserved (must be 0)

Stop-Mode Recovery Source 2

000 = POR Only \*

001 = NAND P20, P21, P22, P23

010 = NAND P20, P21, P22, P33, P24, P25, P26, P27

011 = NOR P31, P32, P33

100 = NAND P31, P32, P33

101 = NOR P31, P32, P33, P00, P07

110 = NAND P31, P32, P33, P00, P07

111 = NAND P31, P32, P33, P20, P21, P22

Reserved (must be 0)

Recovery Level

0 = Low \*

1 = High

Reserved (must be 0)

\* Default setting after reset

Note: If used in conjunction with SMR,  
either of the two specified events  
causes a Stop-Mode Recovery.

**Figure 53. Stop-Mode Recovery Register 2—(0F) DH: D2–D4, D6 Write Only**

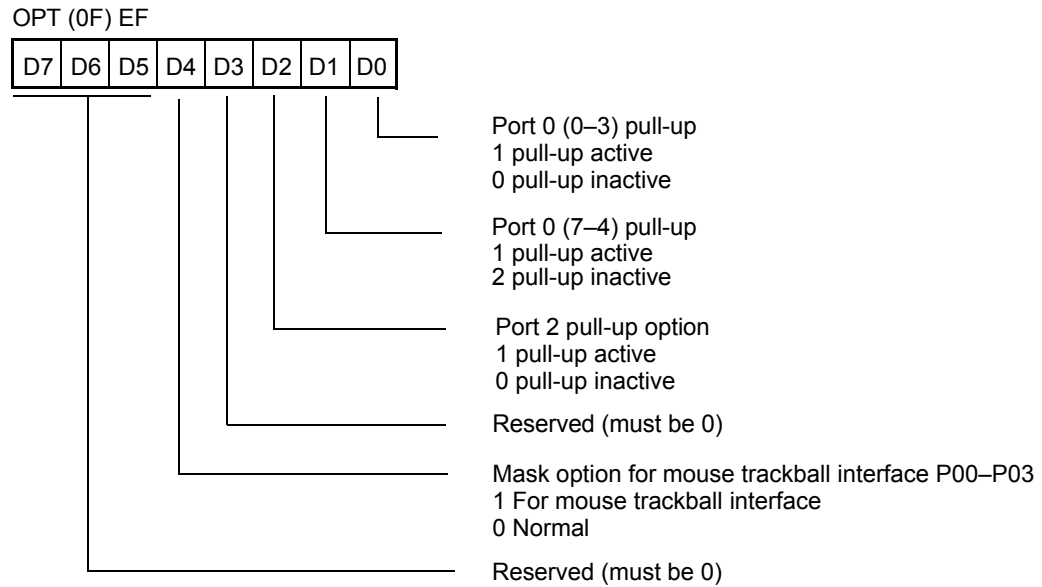
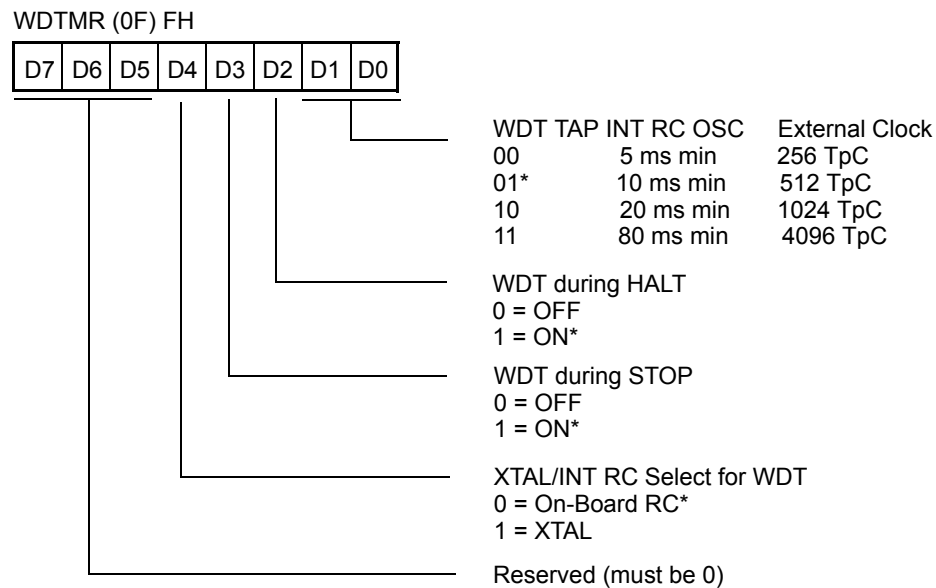
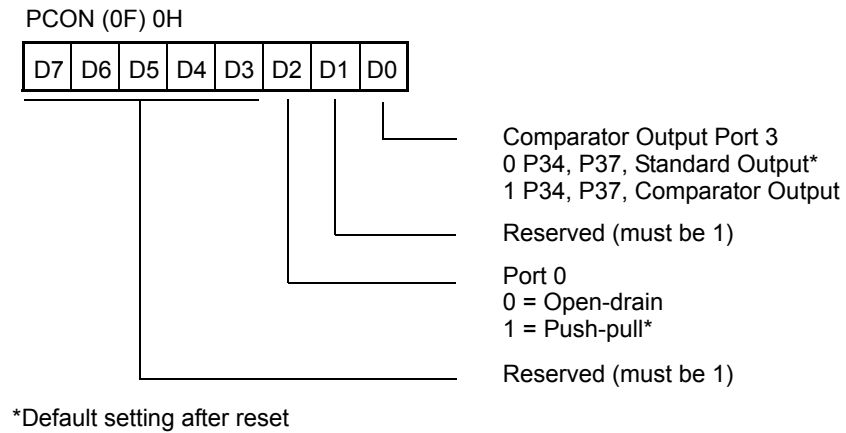


Figure 54. Option Bit Register

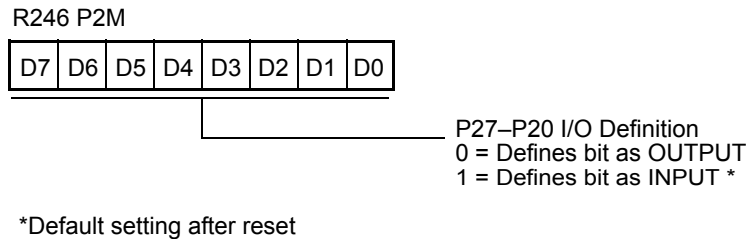


\* Default setting after reset

Figure 55. Watch-Dog Timer Mode Register—(F) 0FH: Write Only



**Figure 56. Port Configuration Register (PCON)—(0F) 0H: Write Only**

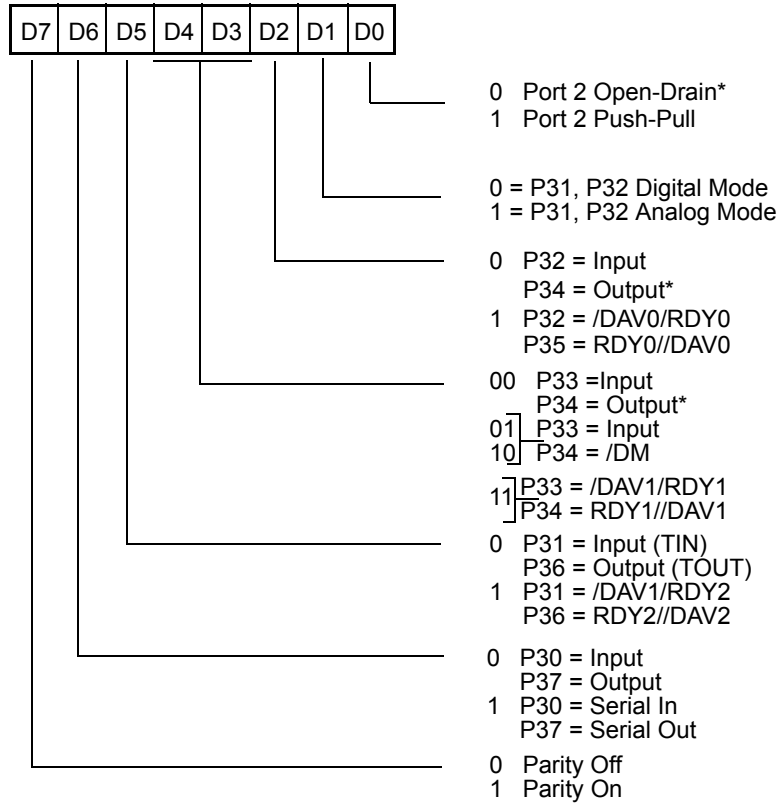


**Figure 57. Port 2 Mode Register—F6H: Write Only**

## Z8 Standard Control Register Diagrams

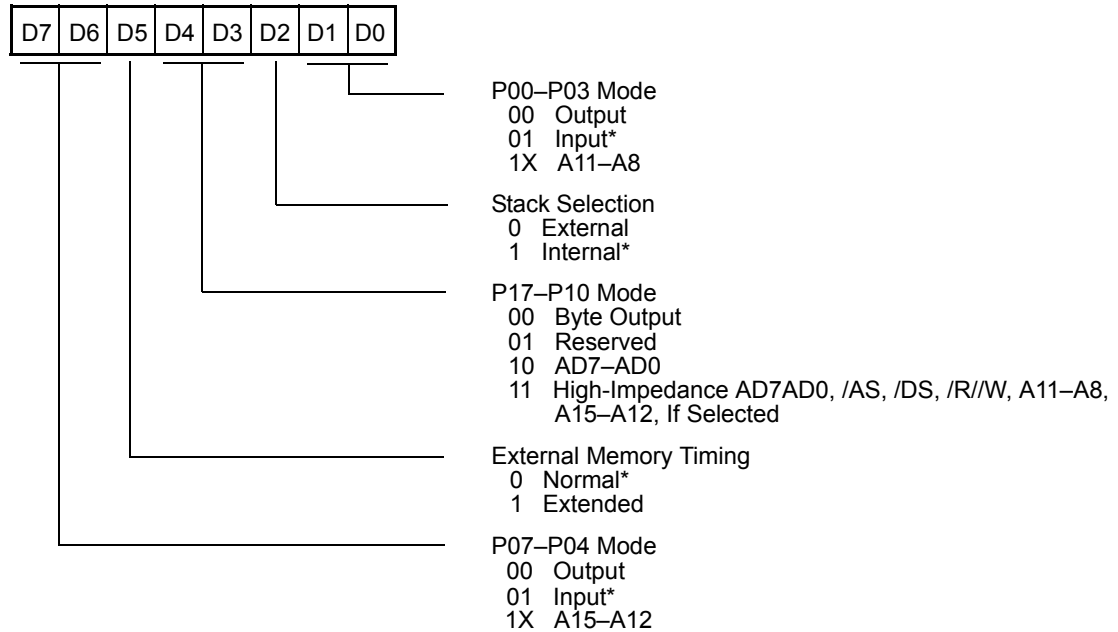
Figure 58 through Figure 66 show the Z8 standard control register diagrams.

R247 P3M

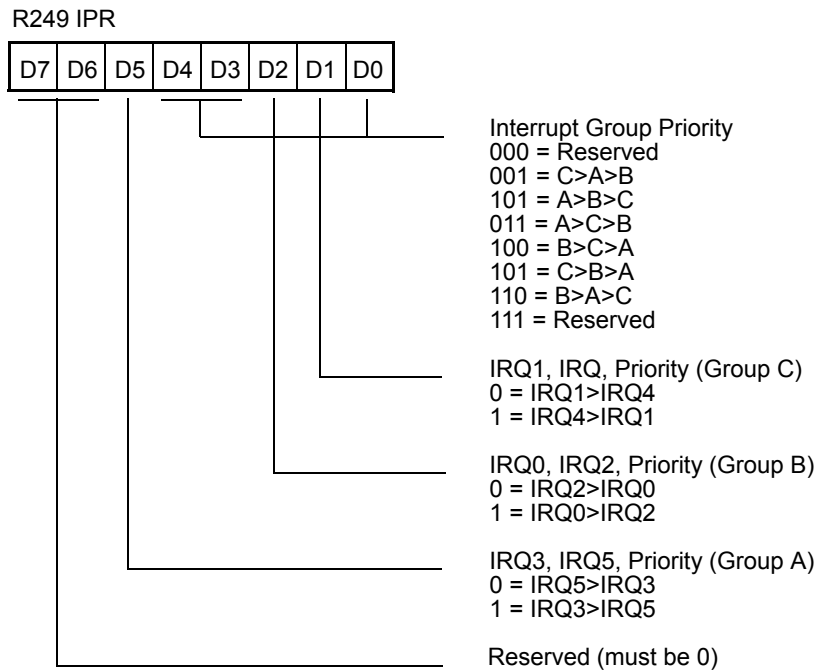


\* Default setting after reset

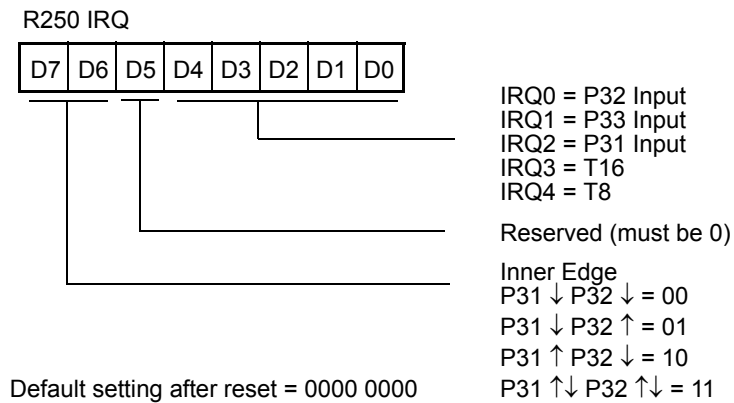
**Figure 58. Port 3 Mode Register—F7H: Write Only**



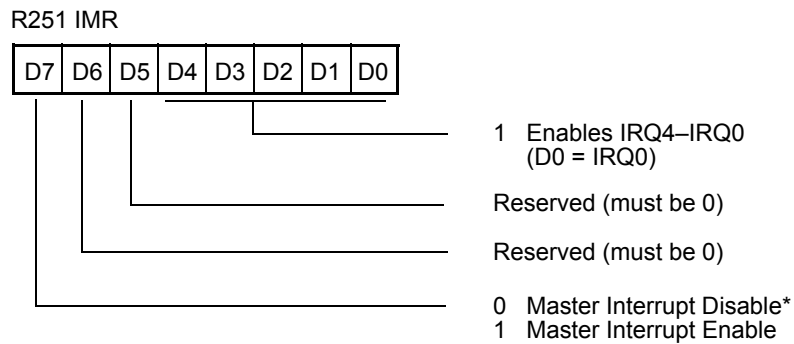
**Figure 59. Port 0 and 1 Mode Register—F8H: Write Only**



**Figure 60. Interrupt Priority Registers—(0) F9H: Write Only**

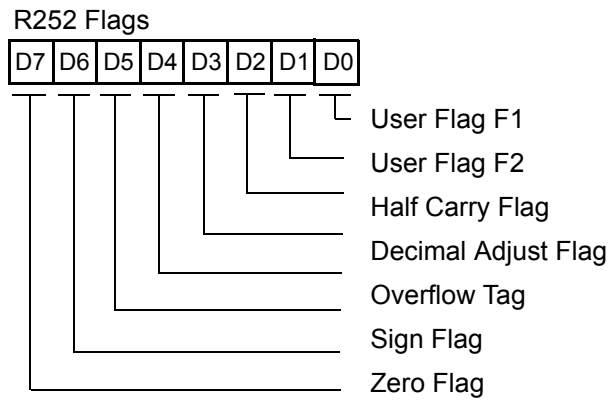


**Figure 61. Interrupt Request Register—(0) FAH: Read/Write**

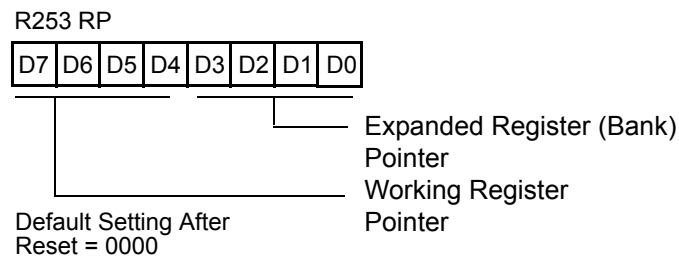


\* Default setting after reset

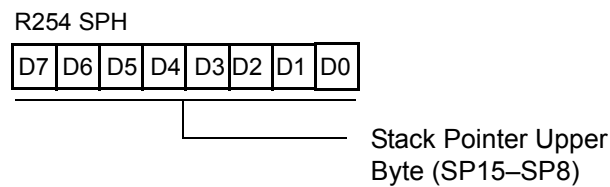
**Figure 62. Interrupt Mask Register—(0) FBH: Read/Write**



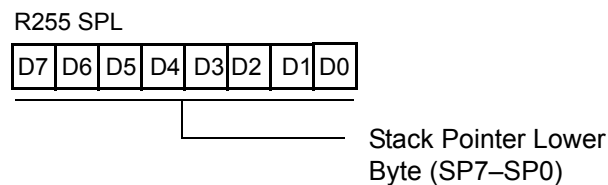
**Figure 63. Flag Register—(0) FCH: Read/Write**



**Figure 64. Register Pointer—(0) FDH: Read/Write**



**Figure 65. Stack Pointer High—(0) FEH: Read/Write**

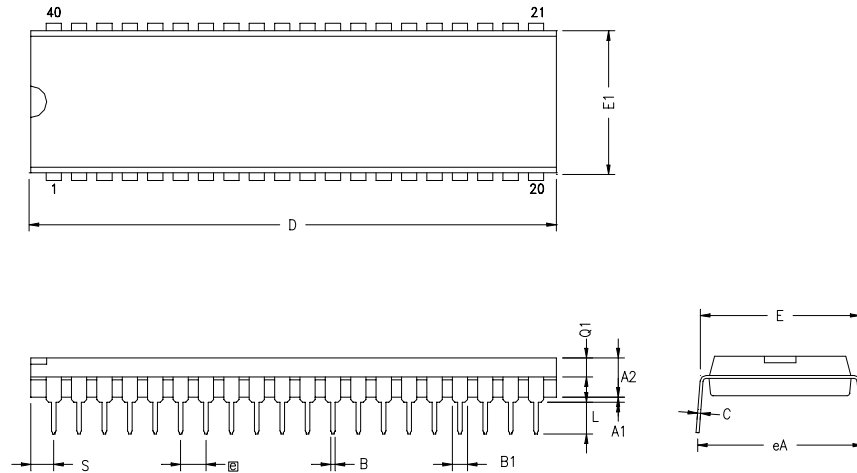




**Figure 66. Stack Pointer Low—(0) FFH: Read/Write**

## Package Information

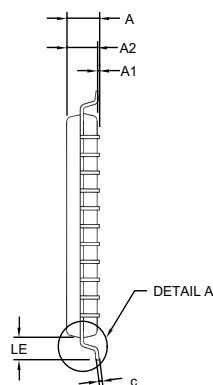
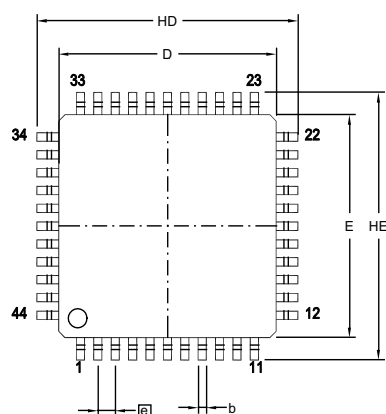
The Z86E72/73 is available in 40-pin DIP (Figure 67), 44-pin LQFP (Figure 68 on page 95), and 44-pin PLCC (Figure 69 on page 96) packages.



| SYMBOL | MILLIMETER |       | INCH     |       |
|--------|------------|-------|----------|-------|
|        | MIN        | MAX   | MIN      | MAX   |
| A1     | 0.51       | 1.02  | .020     | .040  |
| A2     | 3.18       | 3.94  | .125     | .155  |
| B      | 0.38       | 0.53  | .015     | .021  |
| B1     | 1.02       | 1.52  | .040     | .060  |
| C      | 0.23       | 0.38  | .009     | .015  |
| D      | 52.07      | 52.58 | 2.050    | 2.070 |
| E      | 15.24      | 15.75 | .600     | .620  |
| E1     | 13.59      | 14.22 | .535     | .560  |
| Q1     | 2.54 TYP   |       | .100 TYP |       |
| eA     | 15.49      | 16.76 | .610     | .660  |
| L      | 3.05       | 3.81  | .120     | .150  |
| Q1     | 1.40       | 1.91  | .055     | .075  |
| S      | 1.52       | 2.29  | .060     | .090  |

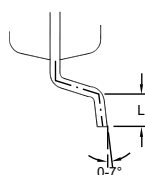
CONTROLLING DIMENSIONS : INCH

**Figure 67. 40-Pin DIP Package Diagram**



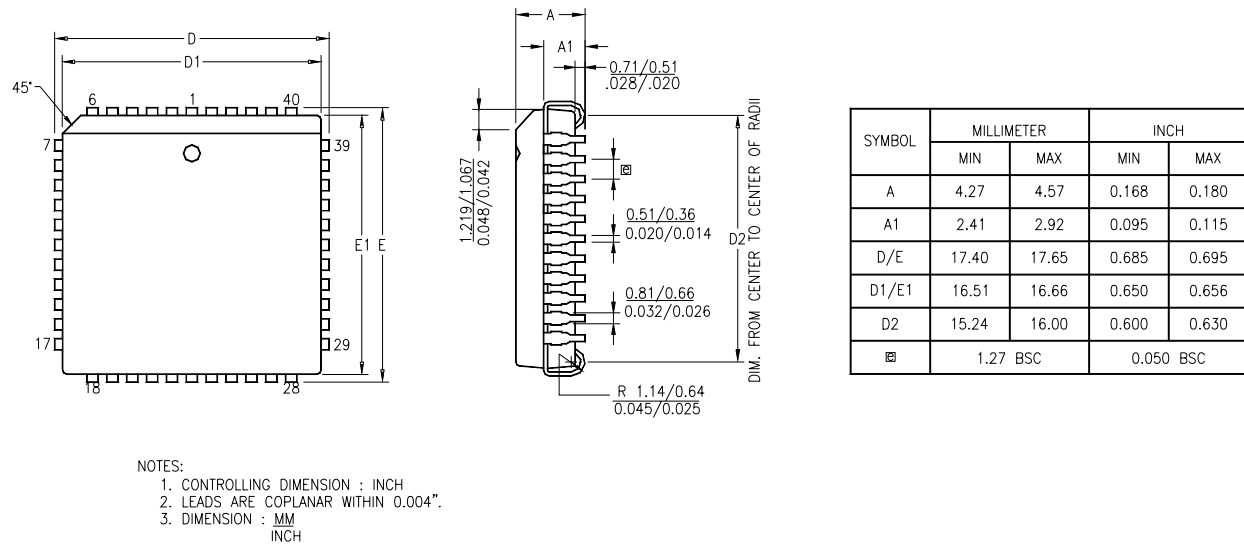
| SYMBOL | MILLIMETER |       | INCH      |       |
|--------|------------|-------|-----------|-------|
|        | MIN        | MAX   | MIN       | MAX   |
| A      | 1.40       | 1.60  | 0.055     | 0.063 |
| A1     | 0.05       | 0.15  | 0.002     | 0.006 |
| A2     | 1.35       | 1.45  | 0.053     | 0.057 |
| b      | 0.30       | 0.45  | 0.012     | 0.018 |
| c      | 0.09       | 0.20  | 0.004     | 0.008 |
| HD     | 11.75      | 12.25 | 0.463     | 0.482 |
| D      | 9.90       | 10.10 | 0.390     | 0.398 |
| HE     | 11.75      | 12.25 | 0.463     | 0.482 |
| E      | 9.90       | 10.10 | 0.390     | 0.398 |
| □      | 0.80 BSC   |       | 0.031 BSC |       |
| L      | 0.45       | 0.75  | 0.018     | 0.030 |
| LE     | 1.00 REF   |       | 0.039 REF |       |

1. CONTROLLING DIMENSIONS : mm  
2. MAX. COPLANARITY : .10mm  
0.004"



DETAIL A

Figure 68. 44-Pin LQFP Package Diagram



**Figure 69. 44-Pin PLCC Package Diagram**

## Ordering Information

Table 33 lists the ordering codes for the 16-MHz Z86E72/73.

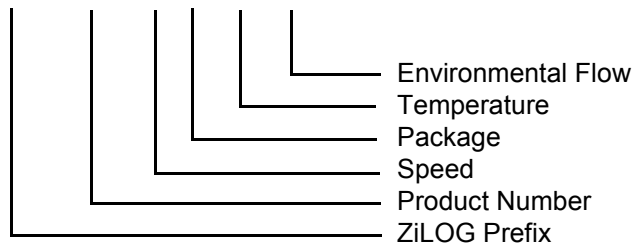
**Table 33. Ordering Codes**

| 40-Pin DIP  | 44-Pin PLCC | 44-Pin LQFP |
|-------------|-------------|-------------|
| Z86E7216PSC | Z86E7216VSC | Z86E7216ASC |
| Z86E7316PSC | Z86E7316VSC | Z86E7316ASC |

Figure 70 shows an example of what the ordering codes represent.

**Example:**

**Z 86E73 16 P S C** is a Z86E73, 16 MHz, DIP, 0 °C to +70 °C, Plastic Standard



**Figure 70. Ordering Codes Example**

For fast results, contact your local ZiLOG sales office for assistance in ordering the part wanted.

**Package**

P = Plastic DIP  
A = Low-profile Quad Flat Pack  
V = Plastic Chip Carrier

**Temperature**

S = 0 °C to +70 °C

**Speed**

16 = 16 MHz

**Environmental**

C = Plastic Standard



## **Customer Support**

For answers to technical questions about the product, documentation, or any other issues with ZiLOG's offerings, please visit ZiLOG's Knowledge Base at <http://www.zilog.com/kb>.

For any comments, detail technical questions, or reporting problems, please visit ZiLOG's Technical Support at <http://support.zilog.com>.