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FAIRCHILD
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March 1995
Revised June 2002

74LCX16500
Low Voltage 18-Bit Universal Bus Transceivers with 5V Tolerant Inputs and Outputs

General Description

These 18-bit universal bus transceivers combine D-type latches and D-type flip-flops to allow data flow in transparent, latched, and clocked modes.

Data flow in each direction is controlled by output-enable (OEAB and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs.

The LCX16500 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with the capability of interfacing to a 5V signal environment.

The LCX16500 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 6.0 ns t_{PD} max (V_{CC} = 3.3V), 20 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA output drive (V_{CC} = 3.0V)
- Uses proprietary noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
  Human body model > 2000V
  Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} and OE tied to GND through a resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

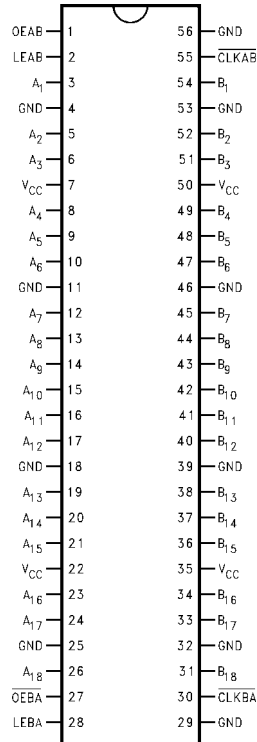| Order Number	Package Number	Package Description
74LCX16500G (Note 2)(Note 3)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LCX16500MEA (Note 3)	MS56A	56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCX16500MTD (Note 3)	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 2: Ordering code "G" indicates Trays.

Note 3: Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.
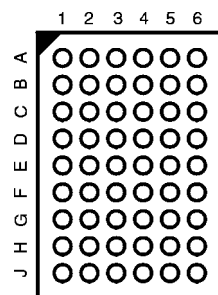
Connection Diagrams

Pin Assignment for SSOP and TSSOP

OEAB	1	56	GND
LEAB	2	55	$\overline{CLKAB}$
A_1	3	54	B_1
GND	4	53	GND
A_2	5	52	B_2
A_3	6	51	B_3
V_{CC}	7	50	V_{CC}
A_4	8	49	B_4
A_5	9	48	B_5
A_6	10	47	B_6
GND	11	46	GND
A_7	12	45	B_7
A_8	13	44	B_8
A_9	14	43	B_9
A_{10}	15	42	B_{10}
A_{11}	16	41	B_{11}
A_{12}	17	40	B_{12}
GND	18	39	GND
A_{13}	19	38	B_{13}
A_{14}	20	37	B_{14}
A_{15}	21	36	B_{15}
V_{CC}	22	35	V_{CC}
A_{16}	23	34	B_{16}
A_{17}	24	33	B_{17}
GND	25	32	GND
A_{18}	26	31	B_{18}
$\overline{OEBA}$	27	30	$\overline{CLKBA}$
LEBA	28	29	GND

Pin Assignment for FBGA

(Top Thru View)

Pin Descriptions

Pin Names	Description
A_1 - A_{18}	Data Register A Inputs/3-STATE Outputs
B_1 - B_{18}	Data Register B Inputs/3-STATE Outputs
$\overline{CLKAB}$, $\overline{CLKBA}$	Clock Pulse Inputs
LEAB, LEBA	Latch Enable Inputs
OEBA, $\overline{OEBA}$	Output Enable Inputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	A_2	A_1	OEAB	GND	B_1	B_2
B	A_4	A_3	LEAB	$\overline{CLKAB}$	B_3	B_4
C	A_6	A_5	V_{CC}	V_{CC}	B_5	B_6
D	A_8	A_7	GND	GND	B_7	B_8
E	A_{10}	A_9	GND	GND	B_9	B_{10}
F	A_{12}	A_{11}	GND	GND	B_{11}	B_{12}
G	A_{14}	A_{13}	V_{CC}	V_{CC}	B_{13}	B_{14}
H	A_{16}	A_{15}	$\overline{OEBA}$	$\overline{CLKBA}$	B_{15}	B_{16}
J	A_{17}	A_{18}	LEBA	GND	B_{18}	B_{17}

Truth Table (Note 4)

Inputs				Output
OEAB	LEAB	$\overline{CLKAB}$	A_n	B_n
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B_0 (Note 5)
H	L	L	X	B_0 (Note 6)

Note 4: A-to-B data flow is shown; B-to-A flow is similar but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$.

Note 5: Output level before the indicated steady-state input conditions were established.

Note 6: Output level before the indicated steady-state input conditions were established, provided that $\overline{CLKAB}$ was LOW before LEAB went LOW.

Functional Description

For A-to-B data flow, the LCX16500 operates in the transparent mode when LEAB is HIGH. When LEAB is LOW, the A data is latched if $\overline{CLKAB}$ is held at a HIGH or LOW logic level. If LEAB is LOW, the A bus data is stored in the latch/flip-flop on the HIGH-to-LOW transition of $\overline{CLKAB}$. Output-enable OEAB is active-HIGH. When OEAB is HIGH, the outputs are active. When OEAB is LOW, the outputs are in the high impedance state.

Data flow for B to A is similar to that of A to B but uses $\overline{OEBA}$, LEBA, and $\overline{CLKBA}$. The output enables are complementary (OEAB is active HIGH and $\overline{OEBA}$ is active LOW).

Logic Diagram

To 17 Other Channels
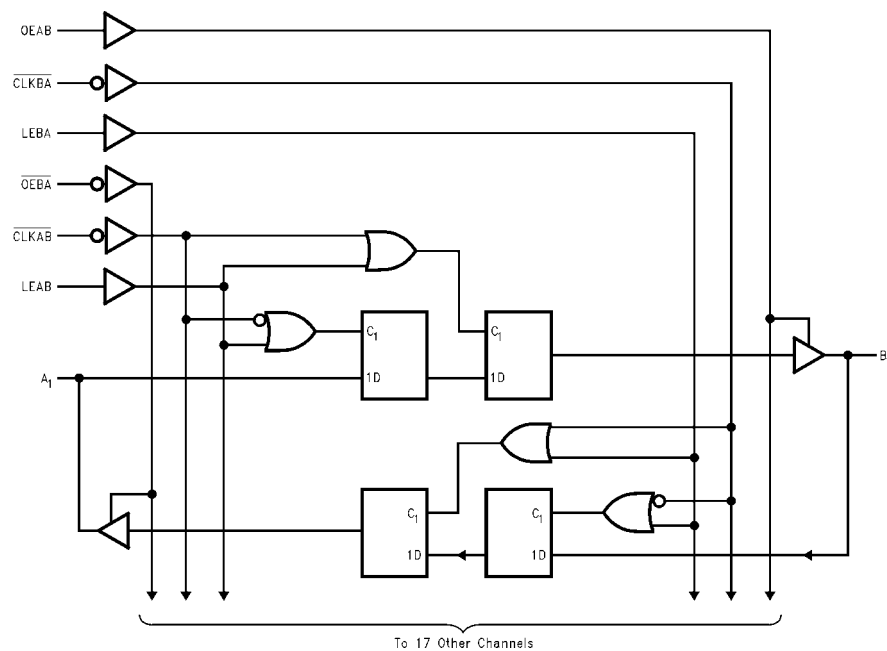
Absolute Maximum Ratings (Note 7)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 8)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions

(Note 9)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V – 3.6V		±24	mA
		V_{CC} = 2.7V – 3.0V		±12	
		V_{CC} = 2.3V – 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
$\Delta t/\Delta V$	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 7: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 8: I_O Absolute Maximum Rating must be observed.

Note 9: Unused (inputs or I/O's) must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100 µA	2.3 – 3.6	V_{CC} − 0.2		V
		I_{OH} = −8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100 µA	2.3 – 3.6		0.2	V
		I_{OL} = 8 mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.3 – 3.6		±5.0	µA
I_{OZ}	3-STATE I/O Leakage	0 ≤ V_O ≤ 5.5V, V_I = V_{IH} or V_{IL}	2.3 – 3.6		±5.0	µA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	µA

DC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V$_{CC}$ (V)	T$_A$ = −40°C to +85°C Min	T$_A$ = −40°C to +85°C Max	Units
I$_{CC}$	Quiescent Supply Current	V$_I$ = V$_{CC}$ or GND	2.3 – 3.6		20	μA
		3.6V ≤ V$_I$, V$_O$ ≤ 5.5V (Note 10)	2.3 – 3.6		±20	
ΔI$_{CC}$	Increase in I$_{CC}$ per Input	V$_{IH}$ = V$_{CC}$ −0.6V	2.3 – 3.6		500	μA

Note 10: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

		T$_A$ = −40°C to +85°C, R$_L$ = 500 Ω						
Symbol	Parameter	V$_{CC}$ = 3.3V ± 0.3V C$_L$ = 50 pF		V$_{CC}$ = 2.7V C$_L$ = 50 pF		V$_{CC}$ = 2.5V ± 0.2V C$_L$ = 30 pF		Units
		Min	Max	Min	Max	Min	Max	
f$_{MAX}$	Maximum Clock Frequency	170						MHz
t$_{PHL}$	Propagation Delay	1.5	6.0	1.5	7.0	1.5	7.2	ns
t$_{PLH}$	Bus to Bus	1.5	6.0	1.5	7.0	1.5	7.2	
t$_{PHL}$	Propagation Delay	1.5	6.7	1.5	8.0	1.5	8.4	ns
t$_{PLH}$	Clock to Bus	1.5	6.7	1.5	8.0	1.5	8.4	
t$_{PHL}$	Propagation Delay	1.5	7.0	1.5	8.0	1.5	8.4	ns
t$_{PLH}$	LE to Bus	1.5	7.0	1.5	8.0	1.5	8.4	
t$_{PZL}$	Output Enable Time	1.5	7.2	1.5	8.2	1.5	9.4	ns
t$_{PZH}$		1.5	7.2	1.5	8.2	1.5	9.4	
t$_{PLZ}$	Output Disable Time	1.5	7.0	1.5	8.0	1.5	8.4	ns
t$_{PHZ}$		1.5	7.0	1.5	8.0	1.5	8.4	
t$_S$	Setup Time	2.5		2.5		3.0		ns
t$_H$	Hold Time	1.5		1.5		2.0		ns
t$_W$	Pulse Width	3.0		3.0		3.5		ns
t$_{OSHL}$	Output to Output Skew		1.0					ns
t$_{OSLH}$	(Note 11)		1.0					

Note 11: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t$_{OSHL}$), or LOW-to-HIGH (t$_{OSLH}$).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V$_{CC}$ (V)	T$_A$ = 25°C Typical	Units
V$_{OLP}$	Quiet Output Dynamic Peak V$_{OL}$	C$_L$ = 50 pF, V$_{IH}$ = 3.3V, V$_{IL}$ = 0V	3.3	0.8	V
		C$_L$ = 30 pF, V$_{IH}$ =2.5V, V$_{IL}$ = 0V	2.5	0.6	
V$_{OLV}$	Quiet Output Dynamic Valley V$_{OL}$	C$_L$ = 50 pF, V$_{IH}$ = 3.3V, V$_{IL}$ = 0V	3.3	−0.8	V
		C$_L$ = 30 pF, V$_{IH}$ =2.5V, V$_{IL}$ = 0V	2.5	−0.6	

Capacitance

Symbol	Parameter	Conditions	Typical	Units
C$_{IN}$	Input Capacitance	V$_{CC}$ = Open, V$_I$ = 0V or V$_{CC}$	7	pF
C$_{I/O}$	Input/Output Capacitance	V$_{CC}$ = 3.3V, V$_I$ = 0V or V$_{CC}$	8	pF
C$_{PD}$	Power Dissipation Capacitance	V$_{CC}$ = 3.3V, V$_I$ = 0V or V$_{CC}$, f = 10 MHz	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

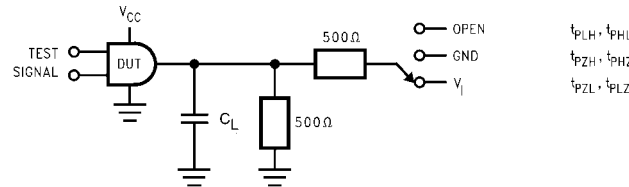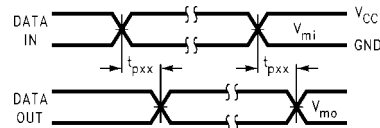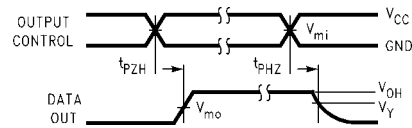| | t_{PLH}, t_{PHL} |
| | t_{PZH}, t_{PHZ} |
| | t_{PZL}, t_{PLZ} |

FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)
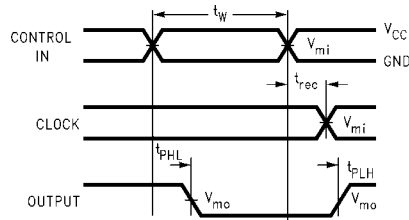
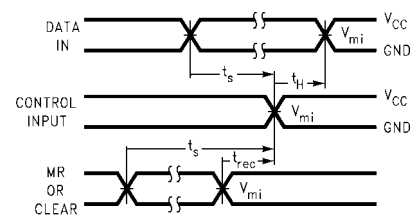| Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$, and 2.7V V_{CC} x 2 at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND

Waveform for Inverting and Non-Inverting Functions
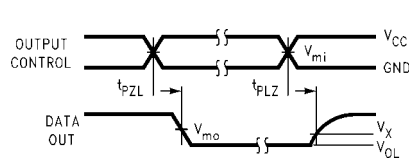

3-STATE Output High Enable and Disable Times for Logic

Propagation Delay. Pulse Width and t_{rec} Waveforms

Setup Time, Hold Time and Recovery Time for Logic
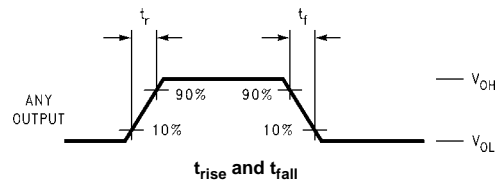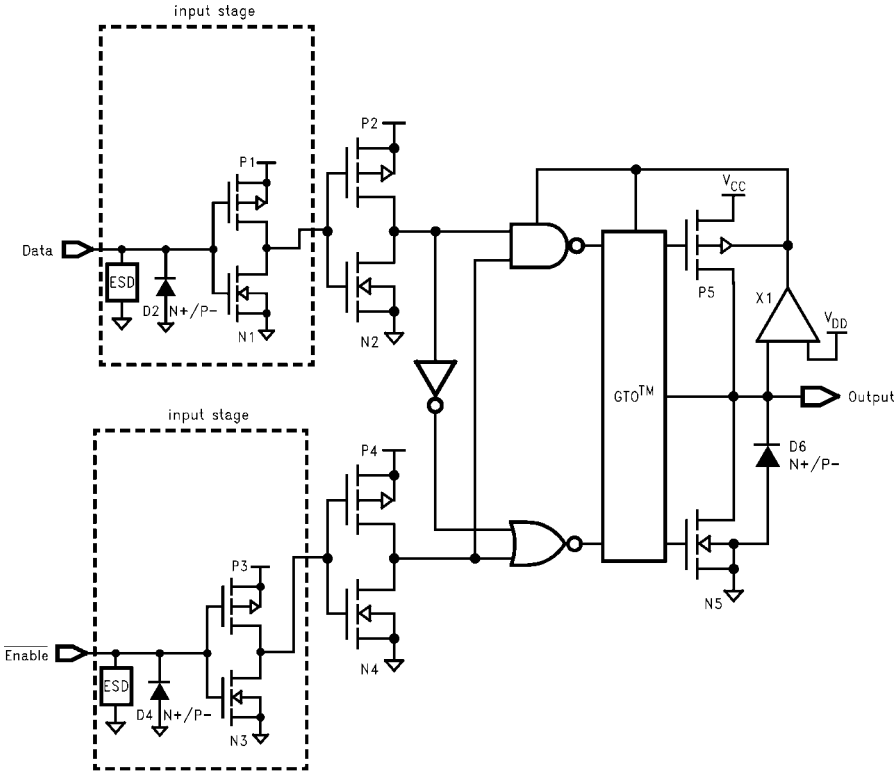

3-STATE Output Low Enable and Disable Times for Logic

t_{rise} and t_{fall}

FIGURE 2. Waveforms
(Input Characteristics; f =1MHz, $t_r = t_f = 3ns$)

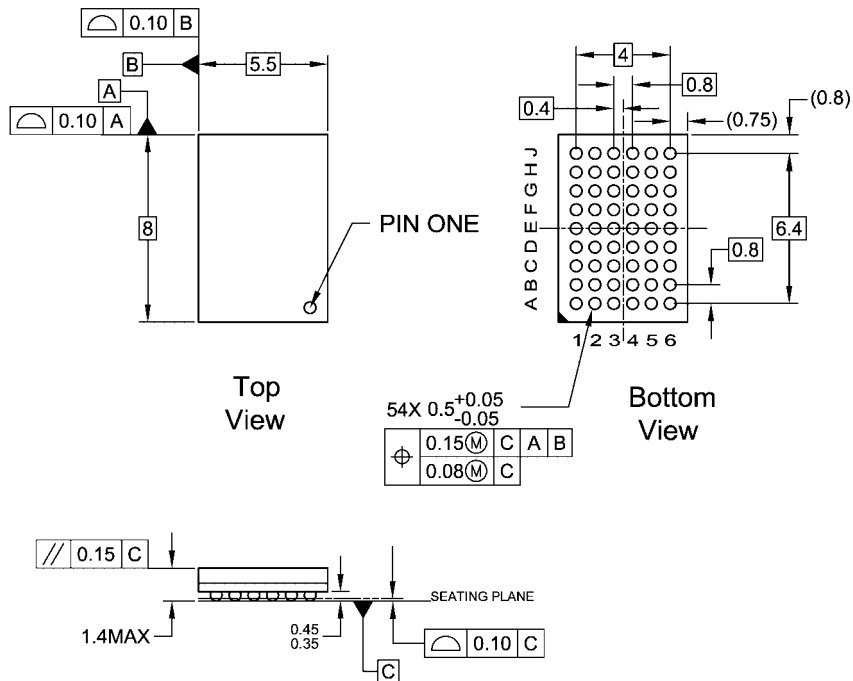| Symbol	V_{CC}		
	3.3V $\pm$ 0.3V	**2.7V**	**2.5V $\pm$ 0.2V**
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family

Physical Dimensions inches (millimeters) unless otherwise noted

⌓ 0.10 B
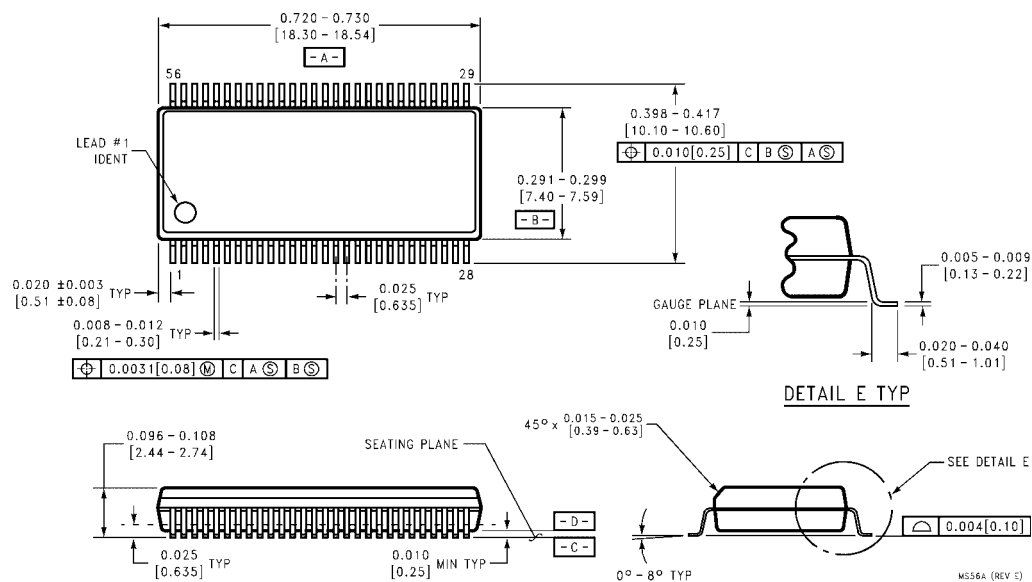
B ◄ 5.5 ►

A

⌓ 0.10 A

8

PIN ONE

Top
View

4

0.8

0.4

(0.8)

(0.75)

A B C D E F G H J

6.4

0.8

1 2 3 4 5 6

Bottom
View

54X 0.5 +0.05 / -0.05

⊕ | 0.15 Ⓜ | C | A | B
| 0.08 Ⓜ | C

∥ | 0.15 | C

SEATING PLANE

1.4MAX

0.45
0.35

⌓ | 0.10 | C

C

NOTES:
A. THIS PACKAGE CONFORMS TO JEDEC M0-205
B. ALL DIMENSIONS IN MILLIMETERS
C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
   .35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA54ArevD

54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA54A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

0.720 – 0.730
[18.30 – 18.54]
– A –

56

29

LEAD #1
IDENT

0.398 – 0.417
[10.10 – 10.60]

⊕ 0.010[0.25] C B Ⓢ A Ⓢ

0.291 – 0.299
[7.40 – 7.59]
– B –

0.020 ±0.003 TYP
[0.51 ±0.08]

1

0.025 TYP
[0.635]

28

0.008 – 0.012 TYP
[0.21 – 0.30]

⊕ 0.0031[0.08] Ⓜ C A Ⓢ B Ⓢ

0.005 – 0.009
[0.13 – 0.22]

GAUGE PLANE

0.010
[0.25]

0.020 – 0.040
[0.51 – 1.01]

DETAIL E TYP

0.096 – 0.108
[2.44 – 2.74]

SEATING PLANE

45° x 0.015 – 0.025
[0.39 – 0.63]

SEE DETAIL E

– D –
– C –

0.025 TYP
[0.635]

0.010 MIN TYP
[0.25]

0° – 8° TYP

⬔ 0.004[0.10]

MS56A (REV E)

**56-Lead Shrink Small Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS56A**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)
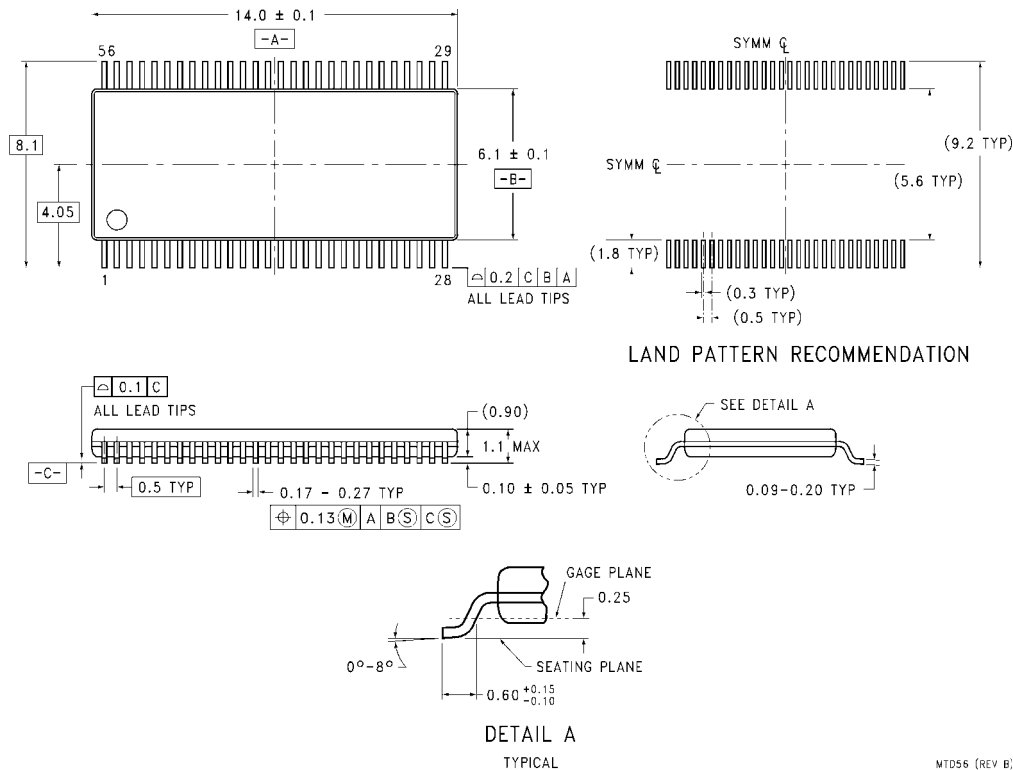
56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD56

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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