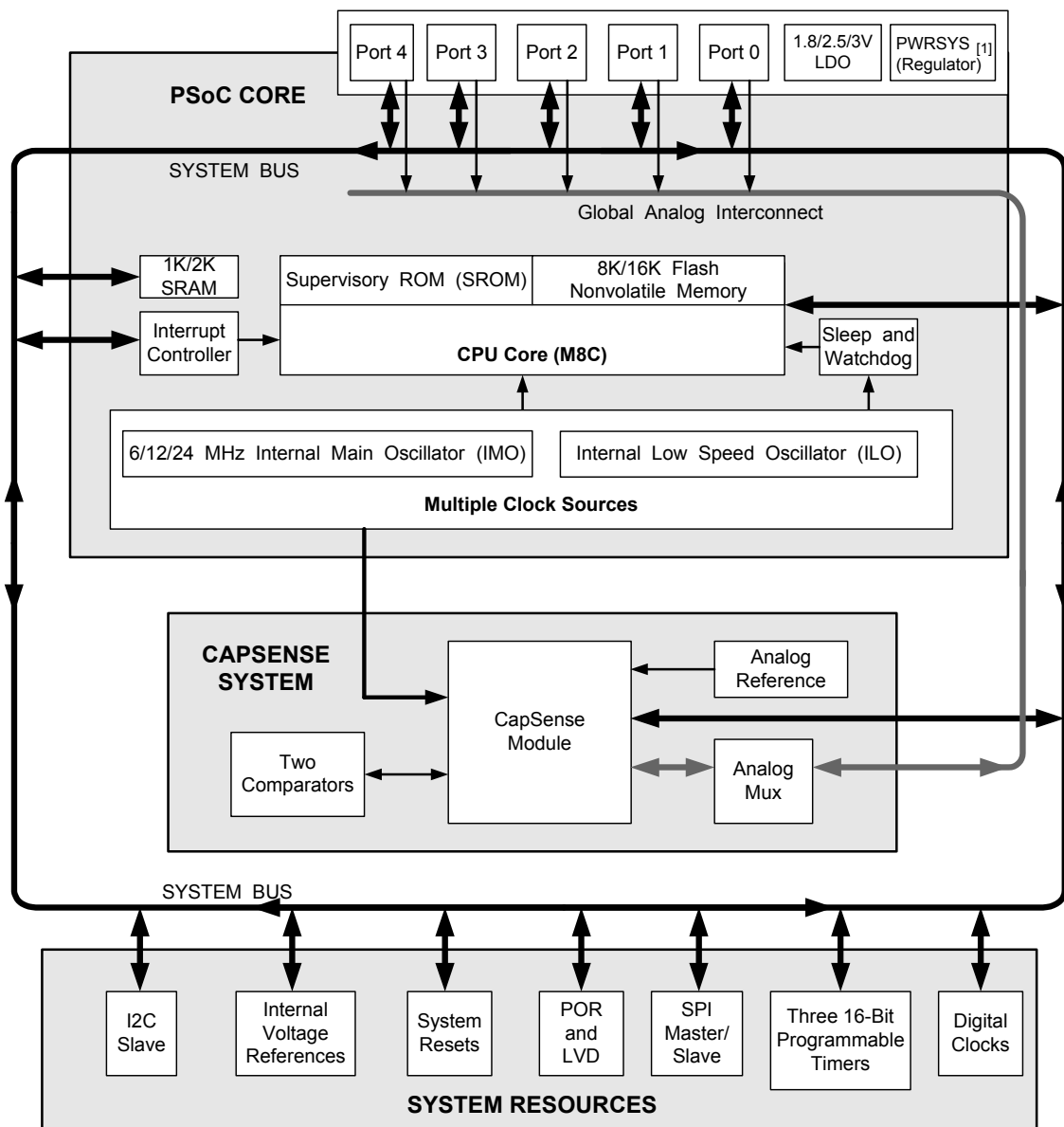


## Features

- 1.71-V to 5.5-V operating range
- Low power CapSense® block
  - Configurable capacitive sensing elements
  - Supports combination of CapSense buttons, sliders, touchpads, touchscreens, and proximity sensors
- Powerful Harvard-architecture processor
  - M8C CPU speed can be up to 24 MHz or sourced by an external crystal, resonator, or clock signal
  - Low power at high speed
  - Interrupt controller
  - Temperature range: -40 °C to +85 °C
- Flexible on-chip memory
  - Two program/data storage size options:
    - CY8C20336H: 8 KB flash / 1 KB SRAM
    - CY8C20446H: 16 KB flash / 2 KB SRAM
  - 50,000 flash erase/write cycles
  - Partial flash updates
  - Flexible protection modes
  - In-System Serial Programming (ISSP)
- Precision, programmable clocking
  - Internal main oscillator (IMO): 6/12/24 MHz ± 5%
  - Internal low-speed oscillator (ILO) at 32 kHz for watchdog and sleep timers
  - Precision 32-kHz oscillator for optional external crystal
- Programmable pin configurations
  - Up to 28 general-purpose I/Os (GPIOs) (depending on the package)
  - Dual-mode GPIO: All GPIOs support digital I/O and analog inputs
  - 25-mA sink current on each GPIO
    - 120-mA total sink current on all GPIOs
  - Pull-up, high Z, open drain modes on all GPIOs
  - CMOS drive mode: 5-mA source current on ports 0 and 1 and 1 mA on ports 2, 3, and 4
    - 20-mA total source current on all GPIOs
  - Selectable, regulated digital I/O on port 1
  - Configurable input threshold on port 1
  - Hot swap capability on all port 1 GPIOs
- Integrates Immersion TS2000 Haptics technology for ERM drive control
- Versatile analog mux
  - Common internal analog bus
  - Simultaneous connection of I/O
  - High [Power supply rejection ratio \(PSRR\)](#) comparator
  - Low dropout voltage regulator for all analog resources
- Additional system resources
  - [I2C](#) slave:
    - Selectable to 50 kHz, 100 kHz, or 400 kHz
    - No clock stretching (under most conditions)
    - Implementation during sleep modes with less than 100 µA
    - Hardware address validation
  - [SPI](#) master and slave: Configurable 46.9 kHz to 12 MHz
  - Three 16-bit timers
  - Watchdog and sleep timers
  - Internal voltage reference
  - Integrated supervisory circuit
  - 8- to 10-bit incremental analog-to-digital converter (ADC)
  - Two general-purpose high-speed, low-power analog comparators
- Complete development tools
  - Free development tool (PSoC Designer™)
  - Full featured, In-Circuit Emulator (ICE) and programmer
  - Full-speed emulation
  - Complex breakpoint structure
  - 128 KB trace memory
- Package options
  - CY8C20336H:
    - 24-pin 4 × 4 × 0.6 mm QFN
  - CY8C20446H:
    - 32-pin 5 × 5 × 0.6 mm QFN

## Logic Block Diagram



### Note

1. Internal voltage regulator for internal circuitry

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## PSoC® Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low-cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the [Logic Block Diagram on page 2](#), consists of three main areas:

- The core
- CapSense analog system
- System resources (including a full-speed USB port).

A common, versatile bus allows connection between the I/O and the analog system.

Each CY8C20336H/446H PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 28 GPIOs are also included. The GPIOs provide access to the MCU and analog mux.

### PSoC Core

The PSoC core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

### CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1-V or 1.2-V analog reference, which together support capacitive sensing of up to 28 inputs<sup>[2]</sup>. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

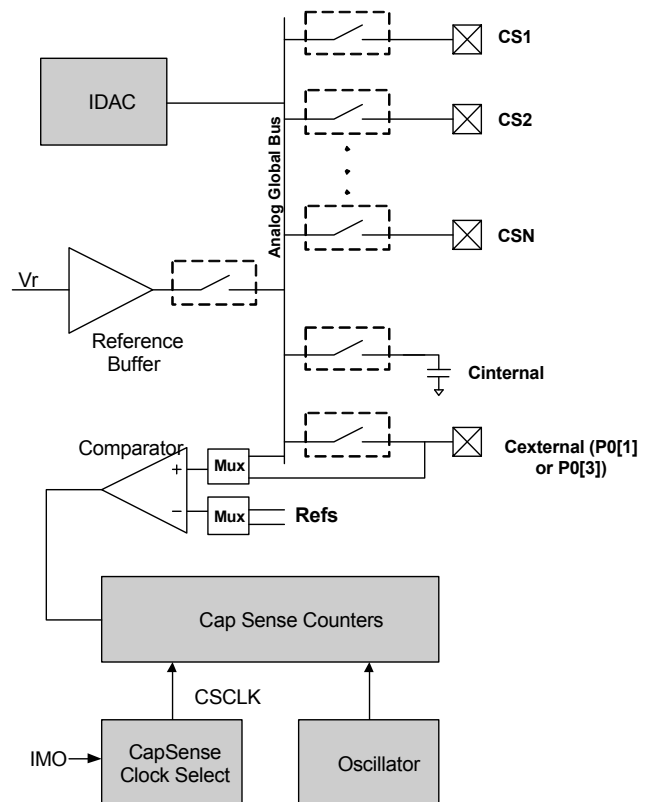
#### SmartSense™

SmartSense is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easy-to-use and provides a robust noise immunity. It is the only auto-tuning solution that establishes, monitors, and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.

#### Note

2. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I<sup>2</sup>C + 1 pin for modulator capacitor.

**Figure 1. CapSense System Block Diagram**



#### Analog Multiplexer System

The analog mux bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch-control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- [Crosspoint connection](#) between any I/O pin combinations.

#### Haptics TS2000 Controller

The CY8C20336H/CY8C20446H family of devices feature an easy-to-use Haptics controller resource with up to 14 different effects. These effects are available for use with three different, selectable ERM modules.

## Additional System Resources

System resources provide additional capability, such as configurable USB and I<sup>2</sup>C slave, SPI master/slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I<sup>2</sup>C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- The I<sup>2</sup>C hardware address recognition feature reduces the already low power consumption by eliminating the need for CPU intervention until a packet addressed to the target device is received.
- The I<sup>2</sup>C enhanced slave interface appears as a 32-byte RAM buffer to the external I<sup>2</sup>C master. Using a simple predefined protocol, the master controls the read and write pointers into the RAM. When this method is enabled, the slave does not stall the bus when receiving data bytes in active mode. For usage details, refer to the application note [I2C Enhanced Slave Operation - AN56007](#).
- Low voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on-reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

## Getting Started

For in depth information, along with detailed programming details, see the PSoC® [Technical Reference Manual](#).

For up-to-date ordering, packaging, and electrical specification information, see the latest [PSoC device datasheets](#) on the web.

## Application Notes

[Cypress application notes](#) are an excellent introduction to the wide variety of possible PSoC designs.

## Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

## Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via [www.cypress.com](http://www.cypress.com), covers a wide variety of topics and skill levels to assist you in your designs.

## CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

## Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

## Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

## Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I<sup>2</sup>C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

### PSoC Designer Software Subsystems

#### *Design Entry*

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

#### *Code Generation Tools*

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

**Assemblers.** The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

**C Language Compilers.** C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

#### *Debugger*

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

#### *Online Help System*

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

#### *In-Circuit Emulator*

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.



## Designing with PSoC Designer

The development process for the PSoC device differs from that of a traditional fixed-function microprocessor. The configurable analog and digital hardware blocks give the PSoC architecture a unique flexibility that pays dividends in managing specification change during development and lowering inventory costs. These configurable resources, called PSoC blocks, have the ability to implement a wide variety of user-selectable functions. The PSoC development process is:

1. Select [user modules](#).
2. Configure user modules.
3. Organize and connect.
4. Generate, verify, and debug.

### Select User Modules

PSoC Designer provides a library of prebuilt, pretested hardware peripheral components called “user modules.” User modules make selecting and implementing peripheral devices, both analog and digital, simple.

### Configure User Modules

Each user module that you select establishes the basic register settings that implement the selected function. They also provide parameters and properties that allow you to tailor their precise configuration to your particular application. For example, a PWM User Module configures one or more digital PSoC blocks, one for each eight bits of resolution. Using these parameters, you can establish the pulse width and duty cycle. Configure the parameters and properties to correspond to your chosen application. Enter values directly or by selecting values from drop-down menus. All of the user modules are documented in datasheets that may be viewed directly in PSoC Designer or on the Cypress website. These [user module datasheets](#) explain the internal operation of the user module and provide performance specifications. Each datasheet describes the use of each user module parameter, and other information that you may need to successfully implement your design.

## Organize and Connect

Build signal chains at the chip level by interconnecting user modules to each other and the I/O pins. Perform the selection, configuration, and routing so that you have complete control over all on-chip resources.

## Generate, Verify, and Debug

When you are ready to test the hardware configuration or move on to developing code for the project, perform the “Generate Configuration Files” step. This causes PSoC Designer to generate source code that automatically configures the device to your specification and provides the software for the system. The generated code provides APIs with high-level functions to control and respond to hardware events at run time, and interrupt service routines that you can adapt as needed.

A complete code development environment lets you to develop and customize your applications in C, assembly language, or both.

The last step in the development process takes place inside PSoC Designer's Debugger (accessed by clicking the Connect icon). PSoC Designer downloads the HEX image to the ICE where it runs at full-speed. PSoC Designer debugging capabilities rival those of systems costing many times more. In addition to traditional single-step, run-to-breakpoint, and watch-variable features, the debug interface provides a large trace buffer. It lets you to define complex breakpoint events that include monitoring address and data bus values, memory locations, and external signals.







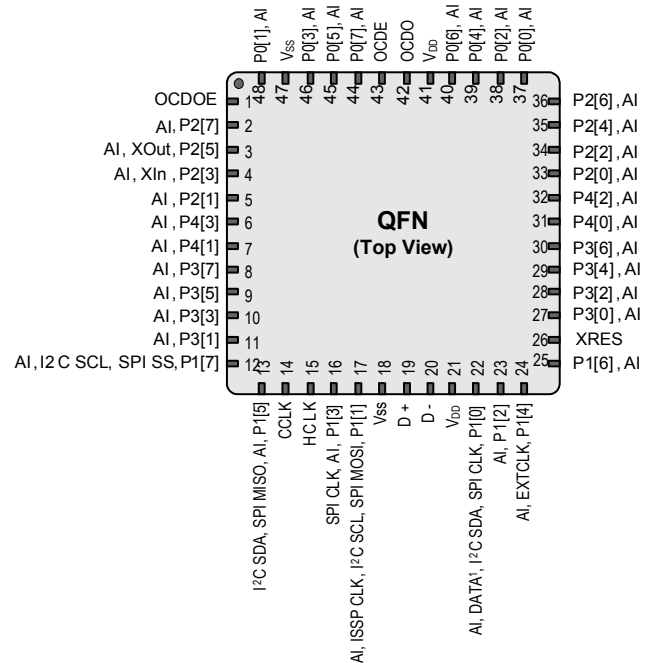
## 48-Pin QFN OCD

The 48-pin QFN part is for the CY8C20066A On-Chip Debug (OCD) PSoC device. Note that this part is only used for in-circuit debugging.<sup>[9]</sup>

**Table 3. Pin Definitions - CY8C20066A PSoC Device** <sup>[10, 11]</sup>

Pin No.	Digital	Analog	Name	Description
1			OCDOE	OCD mode direction pin
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I <sup>2</sup> C SCL, SPI SS
13	IOHR	I	P1[5]	I <sup>2</sup> C SDA, SPI MISO
14			CCLK	OCD CPU clock output
15			HCLK	OCD high speed clock output
16	IOHR	I	P1[3]	SPI CLK.
17	IOHR	I	P1[1]	ISSP CLK <sup>[12]</sup> , I <sup>2</sup> C SCL, SPI MOSI
18	Power		Vss	Ground connection
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		V <sub>DD</sub>	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA <sup>[12]</sup> , I <sup>2</sup> C SDA, SPI CLK
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	

**Figure 4. CY8C20066A PSoC Device**



Pin No.	Digital	Analog	Name	Description
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V <sub>DD</sub>	Supply voltage
42			OCDO	OCD even data I/O
43			OCDE	OCD odd data output
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V <sub>SS</sub>	Ground connection
48	IOH	I	P0[1]	
CP	Power		V <sub>SS</sub>	Center pad must be connected to ground

**LEGEND** A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

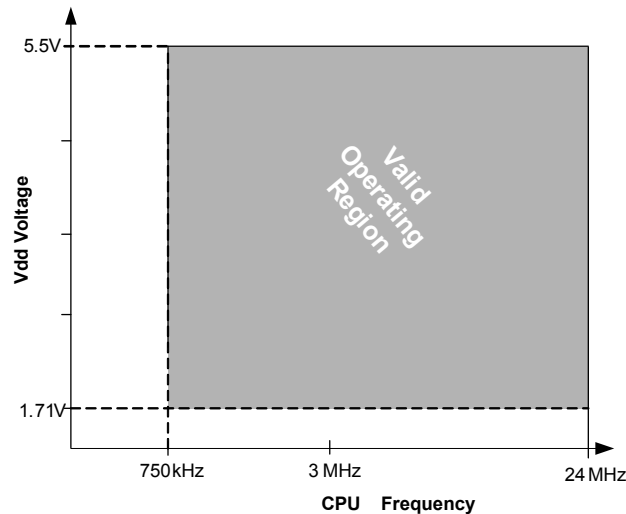
### Notes

9. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.
10. During power-up or reset event, device P1[1] and P1[0] may disturb the I<sup>2</sup>C bus. Use alternate pins if you encounter any issues.
11. The center pad (CP) on the QFN package must be connected to ground (Vss) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
12. These are the ISSP pins, which are not High Z at power on reset (POR).

## Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20x36H/46H PSoC devices. For the latest electrical specifications, confirm that you have the most recent data sheet by visiting the web at <http://www.cypress.com/psoc>.

**Figure 5. Voltage versus CPU Frequency**



## Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

**Table 4. Absolute Maximum Ratings**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>STG</sub>	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	-55	+25	+125	°C
V <sub>DD</sub>	Supply voltage relative to V <sub>SS</sub>		-0.5	–	+6.0	V
V <sub>IO</sub>	DC input voltage		V <sub>SS</sub> – 0.5	–	V <sub>DD</sub> + 0.5	V
V <sub>IOZ</sub>	DC voltage applied to tristate		V <sub>SS</sub> – 0.5	–	V <sub>DD</sub> + 0.5	V
I <sub>MIO</sub>	Maximum current into any port pin		-25	–	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	–	–	V
LU	<a href="#">Latch up current</a>	In accordance with JESD78 standard	–	–	200	mA

## Operating Temperature

**Table 5. Operating Temperature**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>A</sub>	Ambient temperature		-40	–	+85	°C
T <sub>C</sub>	Commercial temperature range		0	–	70	°C
T <sub>J</sub>	Operational die temperature	The temperature rise from ambient to junction is package specific. Refer the table <a href="#">Thermal Impedances per Package on page 28</a> . The user must limit the power consumption to comply with this requirement.	-40	–	+100	°C

## DC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 6. DC Chip-Level Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DD}^{[13]}$	Supply voltage	Refer the table <a href="#">DC POR and LVD Specifications on page 17</a>	1.71	–	5.50	V
$I_{DD24}$	Supply current, IMO = 24 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	3.32	4.00	mA
$I_{DD12}$	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	1.86	2.60	mA
$I_{DD6}$	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	–	1.13	1.80	mA
$I_{SB0}$	Deep sleep current	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	0.50	μA
$I_{SB1}$	Standby current with POR, LVD, and sleep timer	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	μA

### Note

13. When  $V_{DD}$  remains in the range from 1.71 V to 1.9 V for more than 50 μsec, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 μsec to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the  $SR_{POWER\_UP}$  parameter.

### DC General Purpose I/O Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , 2.4 V to 3.0 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , or 1.71 V to 2.4 V and  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ , respectively. Typical parameters apply to 5 V and 3.3 V at  $25^{\circ}\text{C}$  and are for design guidance only.

**Table 7. 3.0 V to 5.5 V DC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$R_{PU}$	Pull-up resistor		4	5.60	8	$k\Omega$
$V_{OH1}$	High output voltage port 2 or 3 pins	$I_{OH} \leq 10\ \mu\text{A}$ , maximum of 10 mA source current in all I/Os	$V_{DD} - 0.20$	–	–	V
$V_{OH2}$	High output voltage port 2 or 3 pins	$I_{OH} = 1\ \text{mA}$ , maximum of 20 mA source current in all I/Os	$V_{DD} - 0.90$	–	–	V
$V_{OH3}$	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	$I_{OH} < 10\ \mu\text{A}$ , maximum of 10 mA source current in all I/Os	$V_{DD} - 0.20$	–	–	V
$V_{OH4}$	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	$I_{OH} = 5\ \text{mA}$ , maximum of 20 mA source current in all I/Os	$V_{DD} - 0.90$	–	–	V
$V_{OH5}$	High output voltage port 1 pins with LDO regulator enabled for 3 V out	$I_{OH} < 10\ \mu\text{A}$ , $V_{DD} > 3.1\ \text{V}$ , maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
$V_{OH6}$	High output voltage port 1 pins with LDO regulator enabled for 3 V out	$I_{OH} = 5\ \text{mA}$ , $V_{DD} > 3.1\ \text{V}$ , maximum of 20 mA source current in all I/Os	2.20	–	–	V
$V_{OH7}$	High output voltage port 1 pins with LDO enabled for 2.5 V out	$I_{OH} < 10\ \mu\text{A}$ , $V_{DD} > 2.7\ \text{V}$ , maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
$V_{OH8}$	High output voltage port 1 pins with LDO enabled for 2.5 V out	$I_{OH} = 2\ \text{mA}$ , $V_{DD} > 2.7\ \text{V}$ , maximum of 20 mA source current in all I/Os	1.90	–	–	V
$V_{OH9}$	High output voltage port 1 pins with LDO enabled for 1.8 V out	$I_{OH} < 10\ \mu\text{A}$ , $V_{DD} > 2.7\ \text{V}$ , maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
$V_{OH10}$	High output voltage port 1 pins with LDO enabled for 1.8 V out	$I_{OH} = 1\ \text{mA}$ , $V_{DD} > 2.7\ \text{V}$ , maximum of 20 mA source current in all I/Os	1.20	–	–	V
$V_{OL}$	Low output voltage	$I_{OL} = 25\ \text{mA}$ , $V_{DD} > 3.3\ \text{V}$ , maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
$V_{IL}$	Input low voltage		–	–	0.80	V
$V_{IH}$	Input high voltage		2.00	–	–	V
$V_H$	Input hysteresis voltage		–	80	–	mV
$I_{IL}$	Input leakage (absolute value)		–	0.001	1	$\mu\text{A}$
$C_{PIN}$	Pin capacitance	Package and pin dependent Temp = $25^{\circ}\text{C}$	0.50	1.70	7	pF

**Table 8. 2.4 V to 3.0 V DC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>PU</sub>	Pull-up resistor		4	5.60	8	kΩ
V <sub>OH1</sub>	High output voltage port 2 or 3 pins	I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH2</sub>	High output voltage port 2 or 3 pins	I <sub>OH</sub> = 0.2 mA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.40	–	–	V
V <sub>OH3</sub>	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I <sub>OH</sub> < 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH4</sub>	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I <sub>OH</sub> = 2 mA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.50	–	–	V
V <sub>OH5A</sub>	High output voltage port 1 pins with LDO enabled for 1.8 V out	I <sub>OH</sub> < 10 μA, V <sub>DD</sub> > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V <sub>OH6A</sub>	High output voltage port 1 pins with LDO enabled for 1.8 V out	I <sub>OH</sub> = 1 mA, V <sub>DD</sub> > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V <sub>OL</sub>	Low output voltage	I <sub>OL</sub> = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V <sub>IL</sub>	Input low voltage		–	–	0.72	V
V <sub>IH</sub>	Input high voltage		1.40	–	–	V
V <sub>H</sub>	Input hysteresis voltage		–	80	–	mV
I <sub>IL</sub>	Input leakage (absolute value)		–	1	1000	nA
C <sub>PIN</sub>	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF

**Table 9. 1.71 V to 2.4 V DC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
R <sub>PU</sub>	Pull-up resistor		4	5.60	8	kΩ
V <sub>OH1</sub>	High output voltage port 2 or 3 pins	I <sub>OH</sub> = 10 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH2</sub>	High output voltage port 2 or 3 pins	I <sub>OH</sub> = 0.5 mA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.50	–	–	V
V <sub>OH3</sub>	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I <sub>OH</sub> = 100 μA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.20	–	–	V
V <sub>OH4</sub>	High output voltage port 0 or 1 pins with LDO regulator disabled for port 1	I <sub>OH</sub> = 2 mA, maximum of 10 mA source current in all I/Os	V <sub>DD</sub> – 0.50	–	–	V
V <sub>OL</sub>	Low output voltage	I <sub>OL</sub> = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V
V <sub>IL</sub>	Input low voltage		–	–	0.30 × V <sub>DD</sub>	V
V <sub>IH</sub>	Input high voltage		0.65 × V <sub>DD</sub>	–	–	V



**Table 9. 1.71 V to 2.4 V DC GPIO Specifications (continued)**

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_H$	Input hysteresis voltage		–	80	–	mV
$I_{IL}$	Input leakage (absolute value)		–	1	1000	nA
$C_{PIN}$	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF

**Table 10. DC Characteristics – USB Interface**

Symbol	Description	Conditions	Min	Typ	Max	Units
Rusbi	USB D+ pull-up resistance	With idle bus	900	–	1575	$\Omega$
Rusba	USB D+ pull-up resistance	While receiving traffic	1425	–	3090	$\Omega$
Vohusb	Static output high		2.8	–	3.6	V
Volusb	Static output low		–	–	0.3	V
Vdi	Differential input sensitivity		0.2	–	–	V
Vcm	Differential input common mode range		0.8	–	2.5	V
Vse	Single-ended receiver threshold		0.8	–	2.0	V
Cin	Transceiver capacitance		–	–	50	pF
Iio	High-Z state data line leakage	On D+ or D- line	–10	–	+10	$\mu$ A
Rps2	PS/2 pull-up resistance		3000	5000	7000	$\Omega$
Rext	External USB series resistor	In series with each USB pin	21.78	22.0	22.22	$\Omega$

### DC Analog Mux Bus Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 11. DC Analog Mux Bus Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$R_{SW}$	Switch resistance to common analog bus		–	–	800	$\Omega$
$R_{GND}$	Resistance of initialization switch to $V_{SS}$		–	–	800	$\Omega$

The maximum pin voltage for measuring  $R_{SW}$  and  $R_{GND}$  is 1.8 V

### DC Low Power Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 12. DC Comparator Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{LPC}$	Low power comparator (LPC) common mode	Maximum voltage limited to $V_{DD}$	0.0	–	1.8	V
$I_{LPC}$	LPC supply current		–	10	40	$\mu$ A
$V_{OSLPC}$	LPC voltage offset		–	2.5	30	mV

### Comparator User Module Electrical Specifications

The following table lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range:  $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$ ,  $1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ .

**Table 13. Comparator User Module Electrical Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$T_{\text{COMP}}$	Comparator response time	50-mV overdrive	–	70	100	ns
Offset		Valid from 0.2 V to $V_{DD} - 0.2\text{ V}$	–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	$\mu\text{A}$
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input Range			0	–	1.5	V

### ADC Electrical Specifications

**Table 14. ADC User Module Electrical Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
<b>Input</b>						
$V_{\text{IN}}$	Input voltage range		0	–	$V_{\text{REFADC}}$	V
$C_{\text{IIN}}$	Input capacitance		–	–	5	pF
$R_{\text{IN}}$	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	$1/(500\text{fF} \times \text{data clock})$	$1/(400\text{fF} \times \text{data clock})$	$1/(300\text{fF} \times \text{data clock})$	$\Omega$
<b>Reference</b>						
$V_{\text{REFADC}}$	ADC reference voltage		1.14	–	1.26	V
<b>Conversion Rate</b>						
$F_{\text{CLK}}$	Data clock	Source is chip's internal main oscillator. See <a href="#">AC Chip-Level Specifications on page 18</a> for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. Sample Rate = $0.001/(2^{\text{Resolution}}/\text{Data clock})$	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. Sample Rate = $0.001/(2^{\text{Resolution}}/\text{Data clock})$	–	5.85	–	ksps
<b>DC Accuracy</b>						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity		–1	–	+2	LSB
INL	<a href="#">Integral nonlinearity</a>		–2	–	+2	LSB
$E_{\text{OFFSET}}$	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
$E_{\text{GAIN}}$	Gain error	For any resolution	–5	–	+5	%FSR
<b>Power</b>						
$I_{\text{ADC}}$	Operating current		–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR ( $V_{DD} > 3.0\text{ V}$ )	–	24	–	dB
		PSRR ( $V_{DD} < 3.0\text{ V}$ )	–	30	–	dB

## DC POR and LVD Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 15. DC POR and LVD Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>POR0</sub>	1.66 V selected in PSoC Designer	V <sub>DD</sub> must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V <sub>POR1</sub>	2.36 V selected in PSoC Designer		–	2.36	2.41	
V <sub>POR2</sub>	2.60 V selected in PSoC Designer		–	2.60	2.66	
V <sub>POR3</sub>	2.82 V selected in PSoC Designer		–	2.82	2.95	
V <sub>LVD0</sub>	2.45 V selected in PSoC Designer		2.40	2.45	2.51	V
V <sub>LVD1</sub>	2.71 V selected in PSoC Designer		2.64 <sup>[14]</sup>	2.71	2.78	
V <sub>LVD2</sub>	2.92 V selected in PSoC Designer		2.85 <sup>[15]</sup>	2.92	2.99	
V <sub>LVD3</sub>	3.02 V selected in PSoC Designer		2.95 <sup>[16]</sup>	3.02	3.09	
V <sub>LVD4</sub>	3.13 V selected in PSoC Designer		3.06	3.13	3.20	
V <sub>LVD5</sub>	1.90 V selected in PSoC Designer		1.84	1.90	2.32	
V <sub>LVD6</sub>	1.80 V selected in PSoC Designer		1.75 <sup>[17]</sup>	1.80	1.84	
V <sub>LVD7</sub>	4.73 V selected in PSoC Designer		4.62	4.73	4.83	

## DC Programming Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 16. DC Programming Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
V <sub>DDIWRITE</sub>	Supply voltage for flash write operations		1.71	–	5.25	V
I <sub>DDP</sub>	Supply current during programming or verify		–	5	25	mA
V <sub>ILP</sub>	Input low voltage during programming or verify	See the appropriate <a href="#">DC General Purpose I/O Specifications on page 13</a>	–	–	V <sub>IL</sub>	V
V <sub>IHP</sub>	Input high voltage during programming or verify	See appropriate <a href="#">DC General Purpose I/O Specifications on page 13</a> table on pages 15 or 16	V <sub>IH</sub>	–	–	V
I <sub>ILP</sub>	Input current when applying V <sub>ILP</sub> to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I <sub>IHP</sub>	Input current when applying V <sub>IHP</sub> to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V <sub>OLP</sub>	Output low voltage during programming or verify		–	–	V <sub>SS</sub> + 0.75	V
V <sub>OHP</sub>	Output high voltage during programming or verify	See appropriate <a href="#">DC General Purpose I/O Specifications on page 13</a> table on page 16. For V <sub>DD</sub> > 3 V use V <sub>OH4</sub> in <a href="#">Table 5 on page 11</a> .	V <sub>OH</sub>	–	V <sub>DD</sub>	V
Flash <sub>ENPB</sub>	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
Flash <sub>DR</sub>	Flash data retention	Following maximum flash write cycles; ambient temperature of 55 °C	10	20	–	Years

### Notes

14. Always greater than 50 mV above V<sub>PPOR1</sub> voltage for falling supply.
15. Always greater than 50 mV above V<sub>PPOR2</sub> voltage for falling supply.
16. Always greater than 50 mV above V<sub>PPOR3</sub> voltage for falling supply.
17. Always greater than 50 mV above V<sub>PPOR0</sub> voltage for falling supply.

## AC Chip-Level Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 17. AC Chip-Level Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>IMO24</sub>	IMO frequency at 24-MHz setting		22.8	24	25.2	MHz
F <sub>IMO12</sub>	IMO frequency at 12-MHz setting		11.4	12	12.6	MHz
F <sub>IMO6</sub>	IMO frequency at 6-MHz setting		5.7	6.0	6.3	MHz
F <sub>CPU</sub>	CPU frequency		0.75	–	25.20	MHz
F <sub>32K1</sub>	ILO frequency		19	32	50	kHz
F <sub>32K_U</sub>	ILO untrimmed frequency		13	32	82	kHz
DC <sub>IMO</sub>	Duty cycle of IMO		40	50	60	%
DC <sub>ILO</sub>	ILO duty cycle		40	50	60	%
SR <sub>POWER_UP</sub>	Power supply slew rate	V <sub>DD</sub> slew rate during power-up	–	–	250	V/ms
T <sub>XRST</sub>	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
T <sub>XRST2</sub>	External reset pulse width after power-up <sup>[18]</sup>	Applies after part has booted	10	–	–	μs

### Note

18. The minimum required XRES pulse length is longer when programming the device (see [Table 23 on page 21](#)).

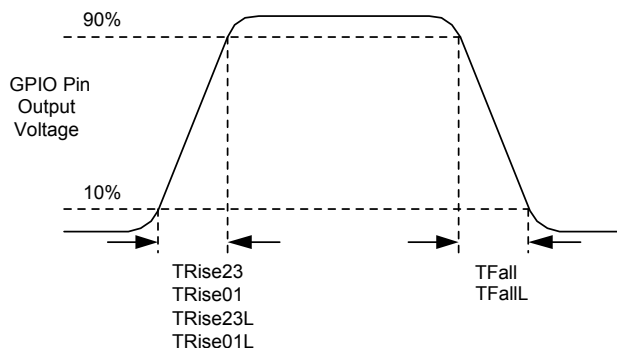
## AC General Purpose I/O Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 18. AC GPIO Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{GPIO}$	GPIO operating frequency	Normal strong mode port 0, 1	0	–	6 MHz for 1.71 V < $V_{DD}$ < 2.40 V 12 MHz for 2.40 V < $V_{DD}$ < 5.50 V	MHz
$T_{RISE23}$	Rise time, strong mode, Cload = 50 pF ports 2 or 3	$V_{DD}$ = 3.0 to 3.6 V, 10% – 90%	15	–	80	ns
$T_{RISE23L}$	Rise time, strong mode low supply, Cload = 50 pF, ports 2 or 3	$V_{DD}$ = 1.71 to 3.0 V, 10% – 90%	15	–	80	ns
$T_{RISE01}$	Rise time, strong mode, Cload = 50 pF ports 0 or 1	$V_{DD}$ = 3.0 to 3.6 V, 10% – 90% LDO enabled or disabled	10	–	50	ns
$T_{RISE01L}$	Rise time, strong mode low supply, Cload = 50 pF, ports 0 or 1	$V_{DD}$ = 1.71 to 3.0 V, 10% – 90% LDO enabled or disabled	10	–	80	ns
$T_{FALL}$	Fall time, strong mode, Cload = 50 pF all ports	$V_{DD}$ = 3.0 to 3.6 V, 10% – 90%	10	–	50	ns
$T_{FALLL}$	Fall time, strong mode low supply, Cload = 50 pF, all ports	$V_{DD}$ = 1.71 to 3.0 V, 10% – 90%	10	–	70	ns

**Figure 6. GPIO Timing Diagram**



**Table 19. AC Characteristics – USB Data Timings**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>DRATE</sub>	Full-speed data rate	Average bit rate	12 – 0.25%	12	12 + 0.25%	MHz
T <sub>JR1</sub>	Receiver jitter tolerance	To next transition	–18.5	–	18.5	ns
T <sub>JR2</sub>	Receiver jitter tolerance	To pair transition	–9	–	9	ns
T <sub>DJ1</sub>	FS driver jitter	To next transition	–3.5	–	3.5	ns
T <sub>DJ2</sub>	FS driver jitter	To pair transition	–4.0	–	4.0	ns
T <sub>FDEOP</sub>	Source jitter for differential transition	To SE0 transition	–2	–	5	ns
T <sub>FEOPT</sub>	Source SE0 interval of EOP		160	–	175	ns
T <sub>FEOPR</sub>	Receiver SE0 interval of EOP		82	–		ns
T <sub>FST</sub>	Width of SE0 interval during differential transition		–	–	14	ns

**Table 20. AC Characteristics – USB Driver**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>FR</sub>	Transition rise time	50 pF	4	–	20	ns
T <sub>FF</sub>	Transition fall time	50 pF	4	–	20	ns
T <sub>FRFM</sub> <sup>[19]</sup>	Rise/fall time matching		90	–	111	%
V <sub>crs</sub>	Output signal crossover voltage		1.30	–	2.00	V

### AC Comparator Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 21. AC Low Power Comparator Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
T <sub>LPC</sub>	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage.	–	–	100	ns

### AC External Clock Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 22. AC External Clock Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
F <sub>OSCEXT</sub>	Frequency (external oscillator frequency)		0.75	–	25.20	MHz
	High period		20.60	–	5300	ns
	Low period		20.60	–	–	ns
	Power-up IMO to switch		150	–	–	μs

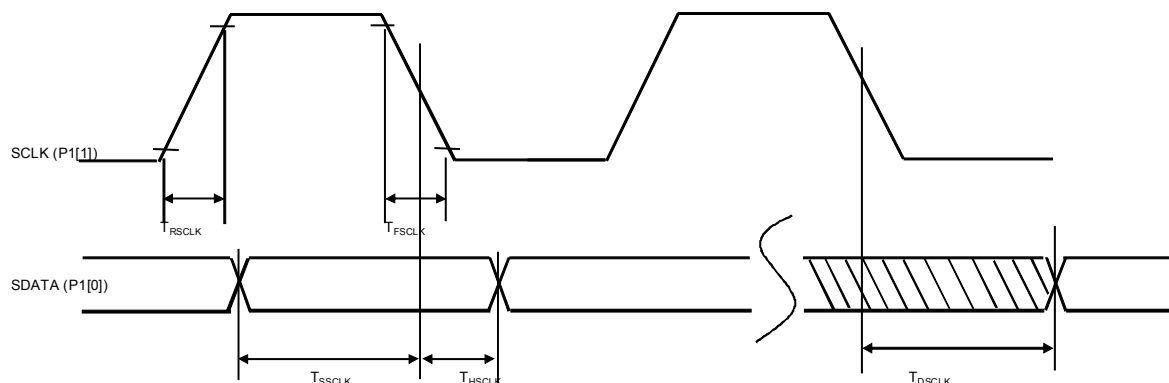
**Note**

19. T<sub>FRFM</sub> is not met under all conditions. There is a corner case at lower supply voltages, such as those under 3.3 V. This condition does not affect USB communications. Signal integrity tests show an excellent eye diagram at 3.15 V.



## AC Programming Specifications

Figure 7. AC Waveform



The following table lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 23. AC Programming Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$T_{RCLK}$	Rise time of SCLK		1	–	20	ns
$T_{FCLK}$	Fall time of SCLK		1	–	20	ns
$T_{SSCLK}$	Data Setup time to falling edge of SCLK		40	–	–	ns
$T_{HSCLK}$	Data Hold time from falling edge of SCLK		40	–	–	ns
$F_{SCLK}$	Frequency of SCLK		0	–	8	MHz
$T_{ERASEB}$	Flash erase time (Block)		–	–	18	ms
$T_{WRITE}$	Flash block write time		–	–	25	ms
$T_{DSCLK}$	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	–	–	60	ns
$T_{DSCLK3}$	Data out delay from falling edge of SCLK	$3.0 \leq V_{DD} \leq 3.6$	–	–	85	ns
$T_{DSCLK2}$	Data out delay from falling edge of SCLK	$1.71 \leq V_{DD} \leq 3.0$	–	–	130	ns
$T_{XRST3}$	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	–	–	$\mu$ s
$T_{XRES}$	XRES Pulse Length		300	–	–	$\mu$ s
$T_{VDDWAIT}$	$V_{DD}$ stable to wait-and-poll hold off		0.1	–	1	ms
$T_{VDDXRES}$	$V_{DD}$ stable to XRES assertion delay		14.27	–	–	ms
$T_{POLL}$	SDATA high pulse time		0.01	–	200	ms
$T_{ACQ}$	“Key window” time after a $V_{DD}$ ramp acquire event, based on 256 ILO clocks.		3.20	–	19.60	ms
$T_{XRESINI}$	“Key window” time after an XRES event, based on eight ILO clocks		98	–	615	$\mu$ s

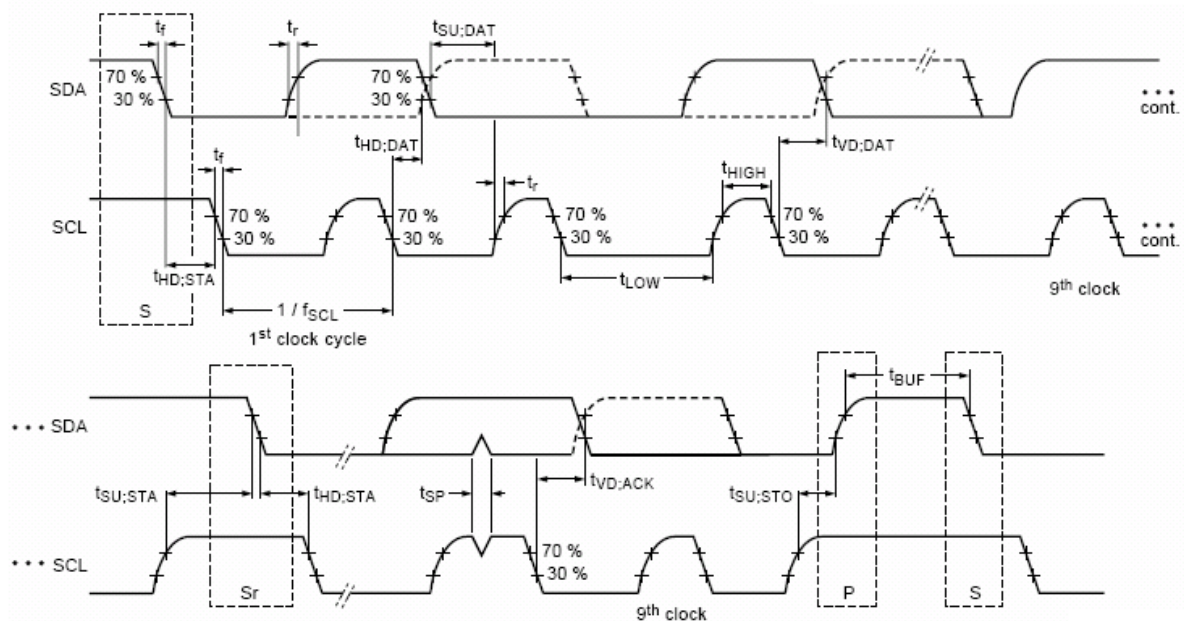
## AC I<sup>2</sup>C Specifications

The following table lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

**Table 24. AC Characteristics of the I<sup>2</sup>C SDA and SCL Pins**

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
$f_{SCL}$	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	—	0.6	—	$\mu$ s
$t_{LOW}$	LOW period of the SCL clock	4.7	—	1.3	—	$\mu$ s
$t_{HIGH}$	HIGH period of the SCL clock	4.0	—	0.6	—	$\mu$ s
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	—	0.6	—	$\mu$ s
$t_{HD;DAT}$	Data hold time	0	3.45	0	0.9	$\mu$ s
$t_{SU;DAT}$	Data setup time	250	—	100 <sup>[20]</sup>	—	ns
$t_{SU;STO}$	Setup time for STOP condition	4.0	—	0.6	—	$\mu$ s
$t_{BUF}$	Bus-free time between a STOP and START condition	4.7	—	1.3	—	$\mu$ s
$t_{SP}$	Pulse width of spikes are suppressed by the input filter.	—	—	0	50	ns

**Figure 8. Definition for Timing for Fast/Standard Mode on the I<sup>2</sup>C Bus**

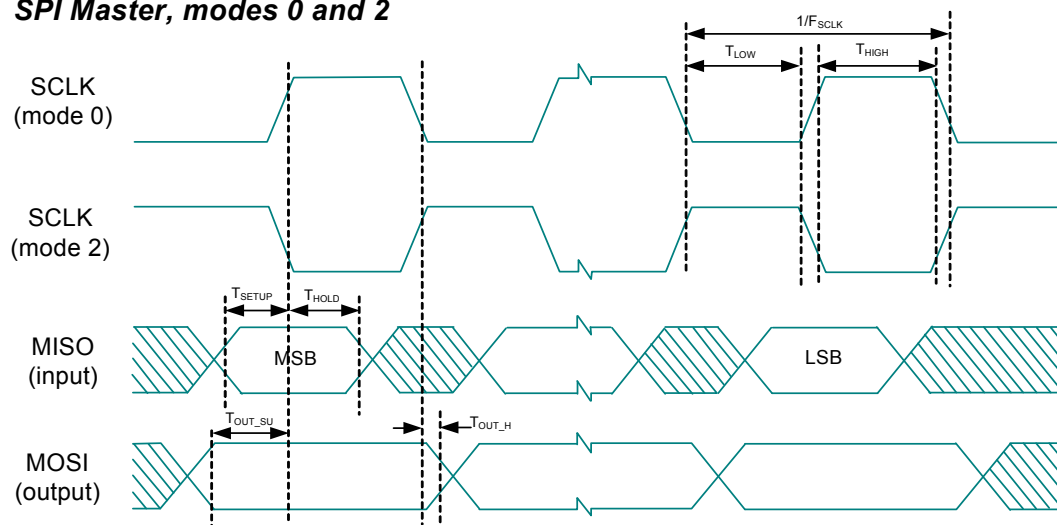


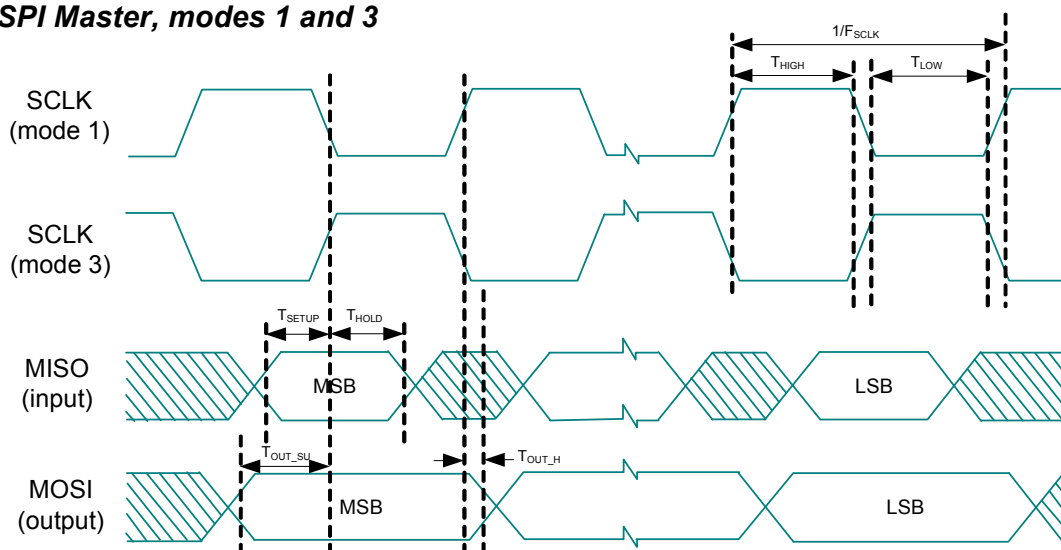
### Note

20. A Fast-Mode I<sup>2</sup>C-bus device can be used in a Standard Mode I<sup>2</sup>C-bus system, but the requirement  $t_{SU;DAT} \geq 250$  ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line  $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$  ns (according to the Standard-Mode I<sup>2</sup>C-bus specification) before the SCL line is released.

**Table 25. SPI Master AC Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{SCLK}$	SCLK clock frequency	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$	— —	— —	6 3	MHz
DC	SCLK duty cycle		—	50	—	%
$T_{SETUP}$	MISO to SCLK setup time	$V_{DD} \geq 2.4\text{ V}$ $V_{DD} < 2.4\text{ V}$	60 100	— —	— —	ns
$T_{HOLD}$	SCLK to MISO hold time		40	—	—	ns
$T_{OUT\_VAL}$	SCLK to MOSI valid time		—	—	40	ns
$T_{OUT\_H}$	MOSI high time		40	—	—	ns

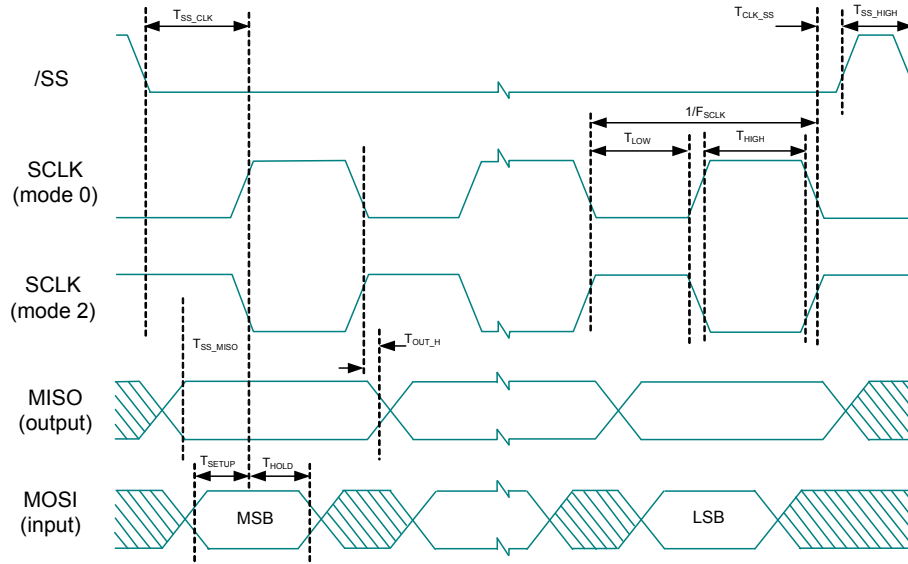
**Figure 9. SPI Master Mode 0 and 2**
**SPI Master, modes 0 and 2**


**Figure 10. SPI Master Mode 1 and 3**
**SPI Master, modes 1 and 3**

**Table 26. SPI Slave AC Specifications**

Symbol	Description	Conditions	Min	Typ	Max	Units
$F_{SCLK}$	SCLK clock frequency	—	—	—	4	MHz
$T_{LOW}$	SCLK low time	—	42	—	—	ns
$T_{HIGH}$	SCLK high time	—	42	—	—	ns
$T_{SETUP}$	MOSI to SCLK setup time	—	30	—	—	ns
$T_{HOLD}$	SCLK to MOSI hold time	—	50	—	—	ns
$T_{SS\_MISO}$	SS high to MISO valid	—	—	—	153	ns
$T_{SCLK\_MISO}$	SCLK to MISO valid	—	—	—	125	ns
$T_{SS\_HIGH}$	SS high time	—	50	—	—	ns
$T_{SS\_CLK}$	Time from SS low to first SCLK	—	$2/SCLK$	—	—	ns
$T_{CLK\_SS}$	Time from last SCLK to SS high	—	$2/SCLK$	—	—	ns

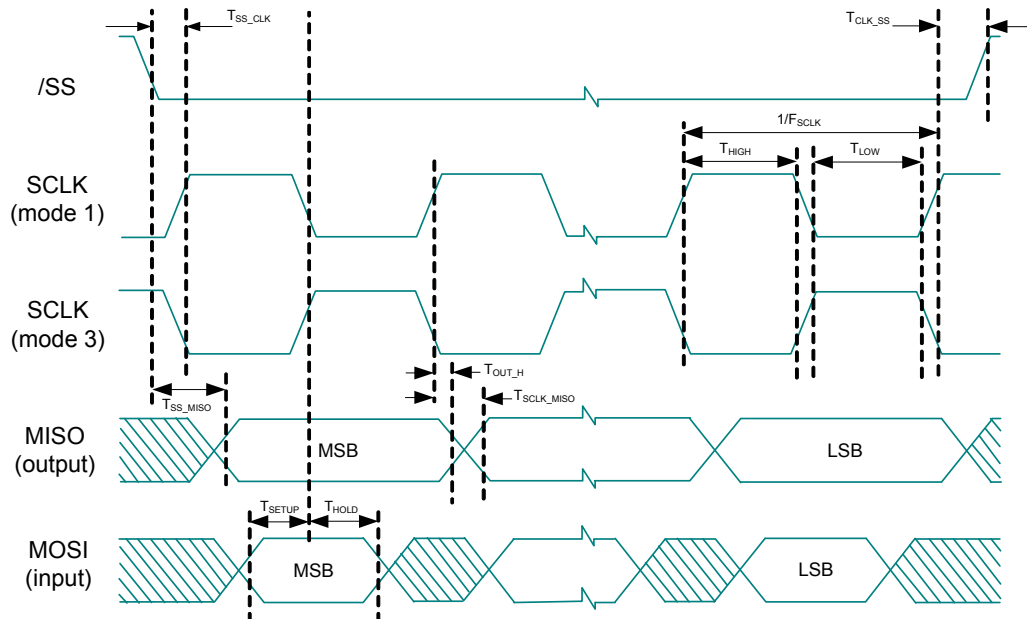
**Figure 11. SPI Slave Mode 0 and 2**

***SPI Slave, modes 0 and 2***



**Figure 12. SPI Slave Mode 1 and 3**

***SPI Slave, modes 1 and 3***

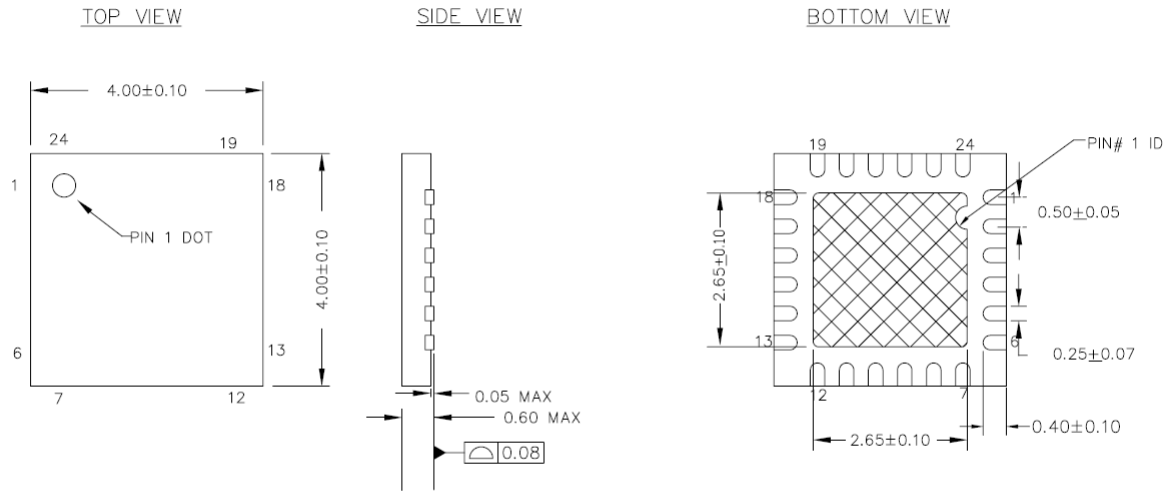


## Packaging Information


This section illustrates the packaging specifications for the CY8C20336H/CY8C20446H PSoC device, along with the thermal impedances for each package.

**Important Note** Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the document titled *PSoC Emulator Pod Dimensions* at <http://www.cypress.com/design/MR10161>.

**Figure 13. 24-Pin ( $4 \times 4 \times 0.55$  mm) QFN**



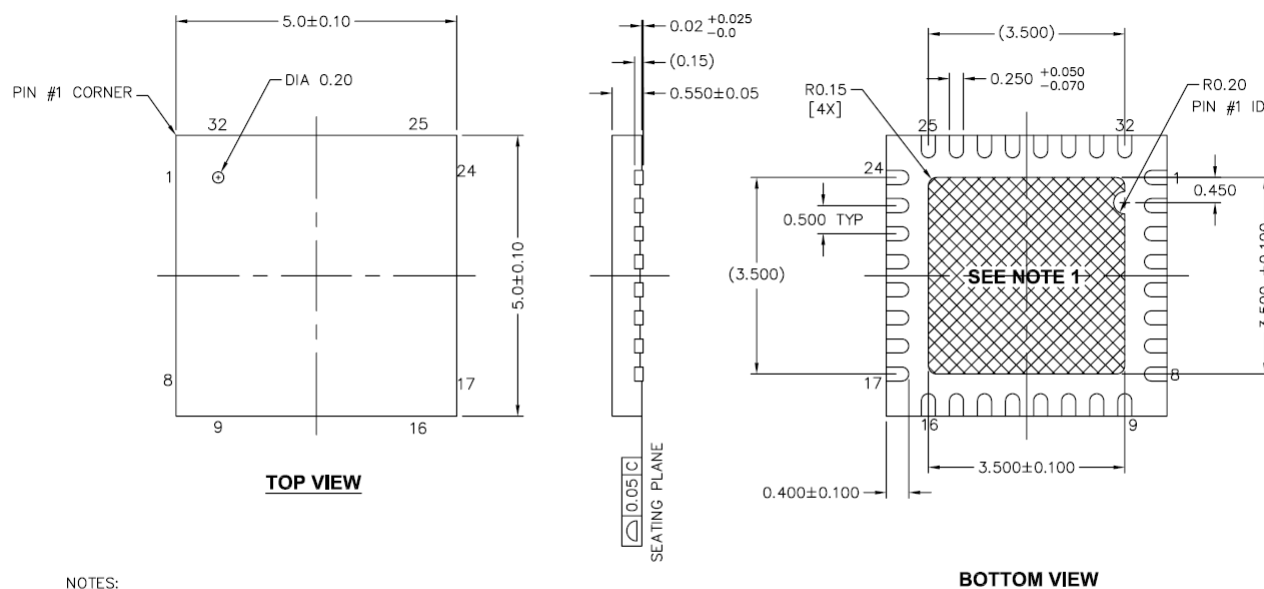
### NOTES :

1.  HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT :  $29 \pm 3$  mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13937 \*E



Figure 14. 32-Pin ( $5 \times 5 \times 0.55$  mm) QFN

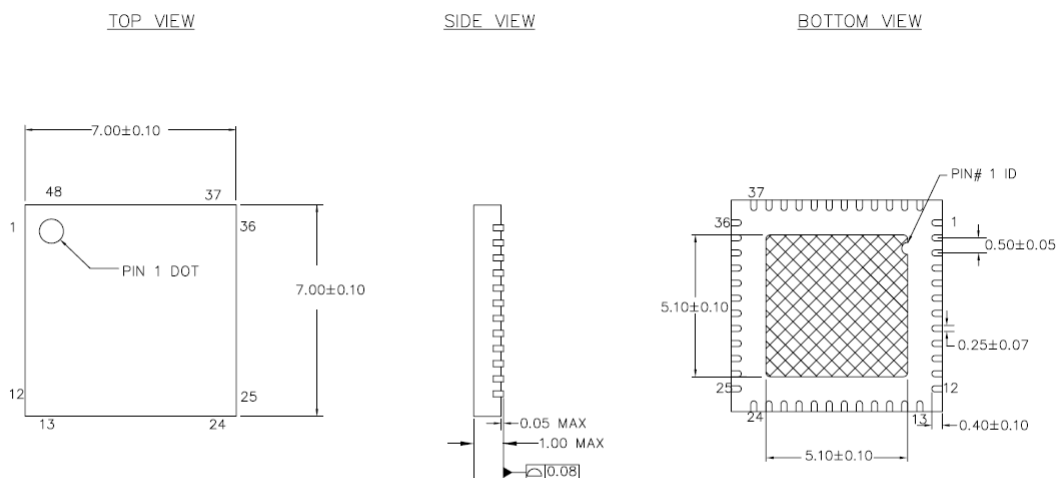


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-248
3. PACKAGE WEIGHT: 0.0388g
4. DIMENSIONS ARE IN MILLIMETERS

001-42168 \*E

Figure 15. 48-Pin ( $7 \times 7 \times 1.0$  mm) QFN



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT:  $13 \pm 1$  mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 \*G

**Important Notes**

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at [http://www.amkor.com/products/notes\\_papers/MLFAppNote.pdf](http://www.amkor.com/products/notes_papers/MLFAppNote.pdf).
- Pinned vias for thermal conduction are not required for the low power PSoC device.

## Thermal Impedances

**Table 27. Thermal Impedances per Package**

Package	Typical $\theta_{JA}$ <sup>[21]</sup>
24-QFN <sup>[22]</sup>	20.90 °C/W
32-QFN <sup>[22]</sup>	19.51 °C/W
48-QFN <sup>[22]</sup>	17.68 °C/W

## Capacitance on Crystal Pins

**Table 28. Typical Package Capacitance on Crystal Pins**

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

## Solder Reflow Peak Temperature

This table lists the minimum solder reflow peak temperature to achieve good solderability.

**Table 29. Solder Reflow Peak Temperature**

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
24-pin QFN	260 °C	30 s
32-pin QFN	260 °C	30 s
48-pin QFN	260 °C	30 s

### Notes

21.  $T_J = T_A + \text{Power} \times \theta_{JA}$ .

22. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

23. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are  $220 \pm 5$  °C with Sn-Pb or  $245 \pm 5$  °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications.

## Development Tool Selection

### Software

#### *PSoC Designer*

At the core of the PSoC development software suite is PSoC Designer. Utilized by thousands of PSoC developers, this robust software has been facilitating PSoC designs for over half a decade. PSoC Designer is available free of charge at <http://www.cypress.com>.

#### *PSoC Programmer*

Flexible enough to be used on the bench in development, yet suitable for factory programming, PSoC Programmer works either as a standalone programming application or it can operate directly from PSoC Designer. PSoC Programmer software is compatible with both PSoC ICE-Cube In-Circuit Emulator and PSoC MiniProg. PSoC Programmer is available free of charge at <http://www.cypress.com>.

### Development Kits

All development kits are sold at the Cypress Online Store.

#### *CY3215-DK Basic Development Kit*

The **CY3215-DK** is for prototyping and development with PSoC Designer. This kit supports in-circuit emulation and the software interface enables users to run, halt, and single step the processor and view the content of specific memory locations. PSoC Designer supports the advance emulation features also. The kit includes:

- PSoC Designer software CD
- ICE-Cube In-Circuit Emulator
- ICE Flex-Pod for CY8C29x66A family
- Cat-5 adapter
- Mini-Eval programming board
- 110 ~ 240-V power supply, Euro-Plug adapter
- iMAGEcraft C Compiler (Registration required)
- ISSP cable
- USB 2.0 cable and Blue Cat-5 cable
- Two CY8C29466A-24PXI 28-PDIP chip samples

### Evaluation Tools

All evaluation tools are sold at the Cypress Online Store.

#### *CY3210-MiniProg1*

The **CY3210-MiniProg1** kit enables the user to program PSoC devices via the MiniProg1 programming unit. The MiniProg is a small, compact prototyping programmer that connects to the PC via a provided USB 2.0 cable. The kit includes:

- MiniProg Programming Unit
- MiniEval Socket Programming and Evaluation Board
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample
- 28-pin CY8C27443A-24PXI PDIP PSoC Device Sample
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

#### *CY3210-PSoCEval1*

The **CY3210-PSoCEval1** kit features an evaluation board and the MiniProg1 programming unit. The evaluation board includes an LCD module, potentiometer, LEDs, and plenty of bread-boarding space to meet all of your evaluation needs. The kit includes:

- Evaluation Board with LCD Module
- MiniProg Programming Unit
- 28-pin CY8C29466A-24PXI PDIP PSoC Device Sample (2)
- PSoC Designer Software CD
- Getting Started Guide
- USB 2.0 Cable

#### *CY3280-20x66 Universal CapSense Controller*

The **CY3280-20X66 CapSense Controller Kit** is designed for easy prototyping and debug of CY8C20xx6A CapSense Family designs with pre-defined control circuitry and plug-in hardware. Programming hardware and an I2C-to-USB bridge are included for tuning and data acquisition.

The kit includes:

- CY3280-20x66 CapSense Controller board
- CY3240-I2USB bridge
- CY3210 MiniProg1 Programmer
- USB 2.0 retractable cable
- CY3280-20x66 Kit CD

## Device Programmers

All device programmers are purchased from the Cypress Online Store.

### CY3216 Modular Programmer

The **CY3216 Modular Programmer kit** features a modular programmer and the MiniProg1 programming unit. The modular programmer includes three programming module cards and supports multiple Cypress products. The kit includes:

- Modular Programmer Base
- Three Programming Module Cards
- MiniProg Programming Unit
- PSoC Designer Software CD

- Getting Started Guide

- USB 2.0 Cable

### CY3207ISSP In-System Serial Programmer (ISSP)

The **CY3207ISSP** is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment. Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

## Accessories (Emulation and Programming)

**Table 30. Emulation and Programming Accessories**

Part Number	Pin Package	Flex-Pod Kit <sup>[24]</sup>	Foot Kit <sup>[25]</sup>	Adapter <sup>[26]</sup>
CY8C20336H-24LQXI	24-pin QFN	CY3250-20366QFN	CY3250-24QFN-FK	See note 24
CY8C20446H-24LQXI	32-pin QFN	CY3250-20466QFN	CY3250-32QFN-FK	See note 26

## Third Party Tools

Several tools have been specially designed by the following third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at <http://www.cypress.com> under Documentation > Evaluation Boards.

## Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note "Debugging - Build a PSoC Emulator into Your Board - AN2323" at <http://www.cypress.com/?rID2748>.

## Notes

24. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.

25. Foot kit includes surface mount feet that can be soldered to the target PCB.

26. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at <http://www.emulation.com>.

27. Dual-function digital I/O pins also connect to the common analog mux.

28. This part is available in limited quantities for in-circuit debugging during prototype development. It is not available in production volumes.

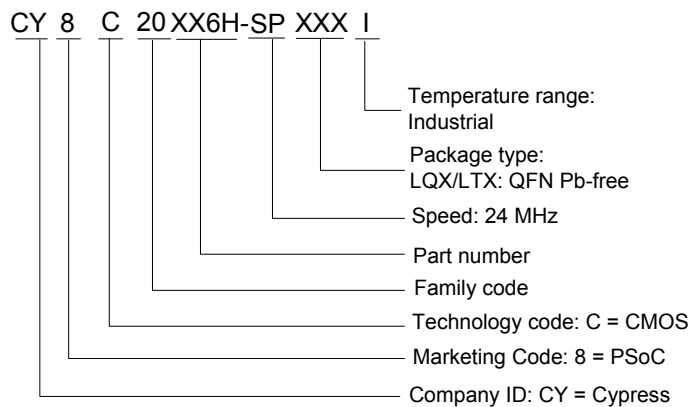
## Ordering Information

The following table lists the CY8C20336H/CY8C20446H PSoC devices' key package features and ordering codes.

**Table 31. PSoC Device Key Features and Ordering Information**

Package	Ordering Code	Flash (KB)	SRAM (KB)	CapSense Blocks	Digital I/O Pins	Analog Inputs <sup>[27]</sup>	XRES Pin	USB
24-pin (4 × 4 × 0.6mm) QFN	CY8C20336H-24LQXI	8	1	1	20	20	Yes	No
32 pin (5 × 5 × 0.6 mm) QFN	CY8C20446H-24LQXI	16	2	1	28	28	Yes	No
48 pin (7 × 7 mm) QFN (OCD) <sup>[28]</sup>	CY8C20066A-24LTXI	32	2	1	36	36	Yes	Yes

## Ordering Code Definitions



## Document Conventions

### Acronyms Used

The following table lists the acronyms that are used in this document.

Acronym	Description
AC	alternating current
ADC	analog-to-digital converter
API	application programming interface
CMOS	complementary metal oxide semiconductor
CPU	central processing unit
DAC	digital-to-analog converter
DC	direct current
EOP	end of packet
FSR	full scale range
GPIO	general purpose input/output
GUI	graphical user interface
I <sup>2</sup> C	inter-integrated circuit
ICE	in-circuit emulator
IDAC	digital analog converter current
ILO	internal low speed oscillator
IMO	internal main oscillator
I/O	input/output
ISSP	in-system serial programming
LCD	liquid crystal display
LDO	low dropout (regulator)
LSB	least-significant bit
LVD	low voltage detect
MCU	micro-controller unit
MIPS	mega instructions per second
MISO	master in slave out
MOSI	master out slave in
MSB	most-significant bit
OCD	on-chip debugger
POR	power on reset
PPOR	precision power on reset
PSRR	power supply rejection ratio
PWRSYS	power system
PSoC®	Programmable System-on-Chip
SLIMO	slow internal main oscillator
SRAM	static random access memory
SNR	signal to noise ratio
QFN	quad flat no-lead
SCL	serial I <sup>2</sup> C clock
SDA	serial I <sup>2</sup> C data
SDATA	serial ISSP data
SPI	serial peripheral interface
SS	slave select
SSOP	shrink small outline package
TC	test controller
USB	universal serial bus
USB D+	USB Data +
USB D-	USB Data-
WLCSP	wafer level chip scale package
XTAL	crystal

### Units of Measure

Table 32 lists all the abbreviations used to measure the PSoC devices.

### Numeric Naming

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase 'h' (for example, '14h' or '3Ah'). Hexadecimal numbers may also be represented by a '0x' prefix, the C coding convention. Binary numbers have an appended lowercase 'b' (for example, '01010100b' or '01000011b'). Numbers not indicated by an 'h', 'b', or 0x are decimal.

**Table 32. Units of Measure**

Symbol	Unit of Measure
°C	degree Celsius
dB	decibels
fF	femto farad
g	gram
Hz	hertz
KB	1024 bytes
Kbit	1024 bits
KHz	kilohertz
Ksps	kilo samples per second
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
μA	microampere
μF	microfarad
μH	microhenry
μs	microsecond
μW	microwatts
mA	milli-ampere
ms	milli-second
mV	milli-volts
nA	nanoampere
ns	nanosecond
nV	nanovolts
Ω	ohm
pA	picoampere
pF	picofarad
pp	peak-to-peak
ppm	parts per million
ps	picosecond
sps	samples per second
σ	sigma: one standard deviation
V	volts
W	watt



## Glossary

<b>Crosspoint connection</b>	Connection between any GPIO combination via analog multiplexer bus.
<b>Differential non-linearity</b>	Ideally, any two adjacent digital codes correspond to output analog voltages that are exactly one LSB apart. Differential non-linearity is a measure of the worst case deviation from the ideal 1 LSB step.
<b>Hold time</b>	Hold time is the time following a clock event during which the data input to a latch or flip-flop must remain stable in order to guarantee that the latched data is correct.
<b>I<sup>2</sup>C</b>	It is a serial multi-master bus used to connect low speed peripherals to MCU.
<b>Integral nonlinearity</b>	It is a term describing the maximum deviation between the ideal output of a DAC/ADC and the actual output level.
<b>Latch up current</b>	Current at which the latch up test is conducted according to JESD78 standard (at 125 °C)
<b>Power supply rejection ratio (PSRR)</b>	The PSRR is defined as the ratio of the change in supply voltage to the corresponding change in output voltage of the device.
<b>Scan</b>	The conversion of all sensor capacitances to digital values.
<b>Setup time</b>	Period required to prepare a device, machine, process, or system for it to be ready to function.
<b>Signal-to-noise ratio</b>	The ratio between a capacitive finger signal and system noise.
<b>SPI</b>	Serial peripheral interface is a synchronous serial data link standard.

## Reference Documents

- Technical reference manual for [CY8C20xx6](#) devices
- In-system Serial Programming (ISSP) protocol for 20xx6 – [AN2026C](#)
- Host Sourced Serial Programming for 20xx6 devices – [AN59389](#)

## Document History Page

Document Title: CY8C20336H/CY8C20446H Haptics Enabled CapSense® Controller Document Number: 001-56223				
Revision	ECN	Origin of Change	Submission Date	Description of Change
**	2787411	VZD/AESA	10/15/2009	New datasheet.
*A	3016550	KEJO/KPOL	08/26/2010	Added CY8C20346H part. Updated 24-pin QFN and 32-pin QFN package diagrams. Content and format updated to match latest template.
*B	3089844	JPM	11/18/10	In <a href="#">Table 26</a> , modified $T_{LOW}$ and $T_{HIGH}$ min values to 42. Updated $T_{SS\_HIGH}$ min value to 50; removed max value.
*C	3180479	YVA	02/23/11	Removed CY8C20346H part Changed title from CapSense Applications to Haptics Enabled CapSense Controller Updated <a href="#">Table 29</a> with Time at Maximum Temperature information
*D	3638625	YLIU/BVI	06/06/2012	Updated $F_{SCLK}$ parameter in the <a href="#">SPI Slave AC Specifications</a> table Updated <a href="#">Getting Started</a> and <a href="#">Designing with PSoC Designer</a> sections. Included <a href="#">Development Tools</a> . Updated <a href="#">Software</a> under <a href="#">Development Tool Selection</a> section. Updated $F_{SCLK}$ parameter in the <a href="#">Table 26</a> , "SPI Slave AC Specifications," on page 24. Changed $t_{OUT\_HIGH}$ to $t_{OUT\_H}$ in <a href="#">Table 25</a> , "SPI Master AC Specifications," on page 23 Updated package diagrams: 001-13937 to *D 001-13191 to *F
*E	3822568	DST	11/27/2012	Updated package diagrams: 001-13937 to *E 001-42168 to *E 001-13191 to *G

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