

## 27 - Line SCSI Terminator With Split Disconnect

### FEATURES

- Complies with SCSI, SCSI-2, SCSI-3, SPI and FAST-20 (Ultra) Standards
- 2.5pF Channel Capacitance During Disconnect
- $100\mu\text{A}$  Supply Current in Disconnect Mode
- 4V To 7V Operation
- $110\Omega$  Termination
- Completely Meets SCSI Hot Plugging
- $-900\text{mA}$  Sourcing Current for Termination
- $+500\text{mA}$  Sinking Current for Active Negation
- Logic Command Disconnects all Termination Lines
- Split Disconnect Controls Lines 1 to 9 and 10 to 27 Separately
- Trimmed Impedance to 5%
- Current Limit and Thermal Shutdown Protection

### DESCRIPTION

The UCC5622 provides 27 lines of active termination for a SCSI (Small Computer Systems Interface) parallel bus. The SCSI standard recommends active termination at both ends of the cable.

The UCC5622 is ideal for high performance 5V SCSI systems. During disconnect the supply current is typically only  $100\mu\text{A}$ , which makes the IC attractive for lower powered systems.

The UCC5622 features a split disconnect allowing the user to control termination lines 10 to 27 with disconnect one, DISC1, and control termination lines 1 to 9 with disconnect two, DISC2.

The UCC5622 is designed with a low channel capacitance of 2.5pF, which eliminates effects on signal integrity from disconnected terminators at interim points on the bus.

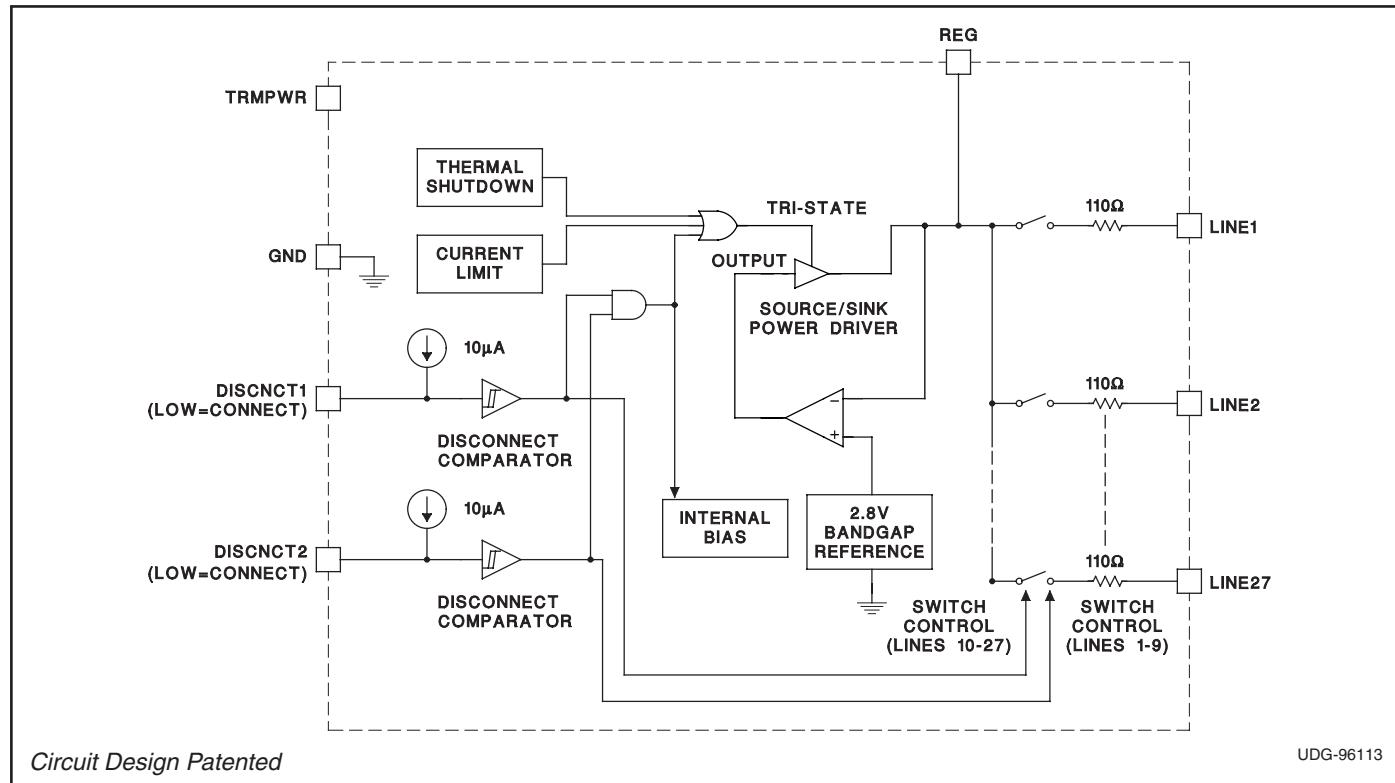
The power amplifier output stage allows the UCC5622 to source full termination current and sink active negation current when all termination lines are actively negated.

The UCC5622, as with all Unitrode terminators, is completely hot pluggable and appears as high impedance at the terminating channels with  $V_{TRMPWR} = 0\text{V}$  or open.

Internal circuit trimming is utilized, first to trim the  $110\Omega$  impedance, and then most importantly, to trim the output current as close to the maximum SCSI-3 specification as possible, which maximizes noise margin in FAST-20 SCSI operation.

**(continued)**

### BLOCK DIAGRAM



*Circuit Design Patented*

UDG-96113

**DESCRIPTION (cont.)**

Other features include thermal shutdown and current limit. This device is offered in low thermal resistance versions of the industry standard 44 pin wide body QSOP (MWP). Consult QSOP-44 Packaging Diagram for exact dimensions.

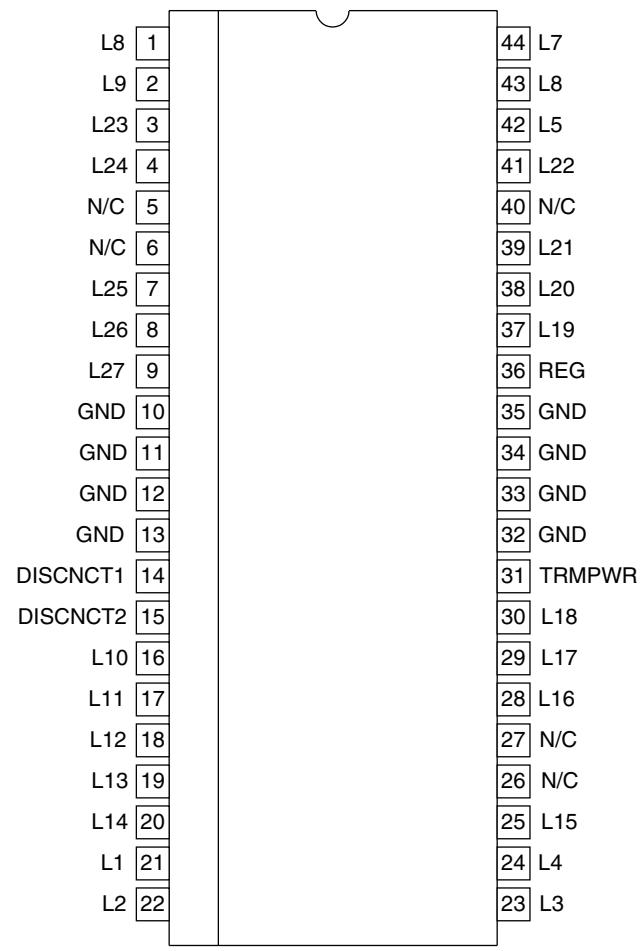
**ABSOLUTE MAXIMUM RATINGS**

TRMPWR Voltage .....	+7V
Signal Line Voltage .....	0V to +7V
Regulator Output Current .....	1.5A
Storage Temperature .....	-65°C to +150°C
Junction Temperature .....	-55°C to +150°C
Lead Temperature (Soldering, 10 Sec.) .....	+300°C

*Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.*

**CONNECTION DIAGRAM**

**QSOP-44 (Top View)**  
**MWP Package**



**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply for  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  
 $\text{TRMPWR} = 4.75\text{V}$ ,  $\text{DISCNCT1} = \text{DISCNCT2} = 0\text{V}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Supply Current Section</b>					
TRMPWR Supply Current	All Termination Lines = Open		1	2	mA
	All Termination Lines = 0.2V		630	650	mA
Power Down Mode	$\text{DISCNCT1} = \text{DISCNCT2} = \text{TRMPWR}$		100	200	$\mu\text{A}$
<b>Output Section (Termination Lines)</b>					
Termination Impedance	(Note 3)	104.5	110	115.5	$\Omega$
Output High Voltage	(Note 1)	2.6	2.8	3.0	V
Max Output Current	$V_{\text{LINE}} = 0.2\text{V}$ , $T_J = 25^\circ\text{C}$	-22.1	-23.3	-24	mA
	$V_{\text{LINE}} = 0.2\text{V}$	-20.7	-23.3	-24	mA
	$V_{\text{LINE}} = 0.2\text{V}$ , $\text{TRMPWR} = 4\text{V}$ , $T_J = 25^\circ\text{C}$ (Note 1)	-21	-23	-24	mA
	$V_{\text{LINE}} = 0.2\text{V}$ , $\text{TRMPWR} = 4\text{V}$ (Note 1)	-20	-23	-24	mA
	$V_{\text{LINE}} = 0.5\text{V}$			-22.4	mA
Output Leakage	$\text{DISCNCT1} = \text{DISCNCT2} = 2.4\text{V}$ , $\text{TRMPWR} = 0\text{V}$ to $5.25\text{V}$		10	400	nA
Output Capacitance	$\text{DISCNCT1} = \text{DISCNCT2} = 2.4\text{V}$ (Note 2)		2.5	4	pF

**ELECTRICAL CHARACTERISTICS** Unless otherwise stated, these specifications apply for  $T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $\text{TRMPWR} = 4.75\text{V}$ ,  $\text{DISCNCT1} = \text{DISCNCT2} = 0\text{V}$ ,  $T_A = T_J$ .

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
<b>Regulator Section</b>					
Regulator Output Voltage		2.6	2.8	3.0	V
Drop Out Voltage	All Termination Lines = 0.2V		0.4	0.8	V
Short Circuit Current	$V_{\text{REG}} = 0\text{V}$	-650	-900	-1300	mA
Sinking Current Capability	$V_{\text{REG}} = 3.5\text{V}$	300	500	900	mA
Thermal Shutdown			170		$^\circ\text{C}$
Thermal Shutdown Hysteresis			10		$^\circ\text{C}$
<b>Disconnect Section</b>					
Disconnect Threshold DISCNCT1	Controls Lines 10 to 27	0.8	1.5	2.0	V
Input Current DISCNCT1	$\text{DISCNCT1} = 0\text{V}$		-10	-30	$\mu\text{A}$
Disconnect Threshold DISCNCT2	Controls Lines 1 to 9	0.8	1.5	2	V
Input Current DISCNCT2	$\text{DISCNCT2} = 0\text{V}$		-10	-30	$\mu\text{A}$

Note 1: Measuring each termination line while other 26 are low (0.2V).

Note 2: Ensured by design. Not 100% tested in production.

Note 3: Tested by measuring  $I_{\text{OUT}}$  with  $V_{\text{OUT}} = 0.2\text{V}$  and  $V_{\text{OUT}}$  with no load, then calculate:

$$Z = \frac{V_{\text{OUT}} \text{ N.L.} - 0.2\text{V}}{I_{\text{OUT}} \text{ at } 2.0\text{V}}$$

## PIN DESCRIPTIONS

**DISCNCT1:** Disconnect one controls termination lines 10 – 27. Taking this pin high or leaving it open causes termination lines 10 - 27 to become high impedance, taking this pin low allows the channels to provide normal termination.

**DISCNCT2:** Disconnect two controls termination lines 1 – 9. Taking this pin high or leaving it open causes termination lines 1 - 9 to become high impedance. Taking this pin low allows the channels to provide normal termination. Taking both disconnect pins high or leaving

them open will put the chip in to sleep mode where it will be in low-power mode.

**GND:** Ground reference for the IC.

**L1 – L27:**  $110\Omega$  termination channels.

**REG:** Output of the internal 2.7V regulator.

**TRMPWR:** Power for the IC.

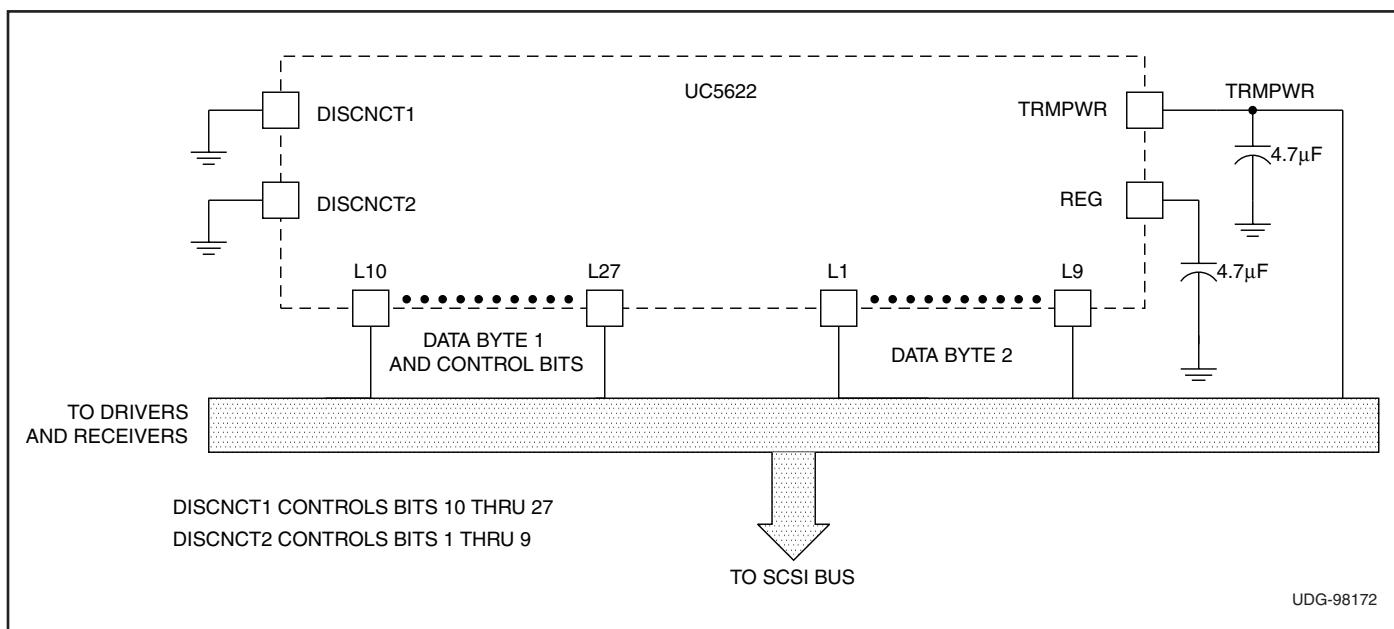


Figure 1. Typical Wide SCSI Bus Configuration Using the UCC5622

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC5622FQP	OBsolete	LQFP	PT	48		TBD	Call TI	Call TI	0 to 70		
UCC5622FQPTR	OBsolete	LQFP	PT	48		TBD	Call TI	Call TI	0 to 70		
UCC5622MWP	LIFEBUY	SSOP	DCE	44	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5622MWP	
UCC5622MWP4	LIFEBUY	SSOP	DCE	44	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC5622MWP	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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## PACKAGE OPTION ADDENDUM

7-Oct-2013

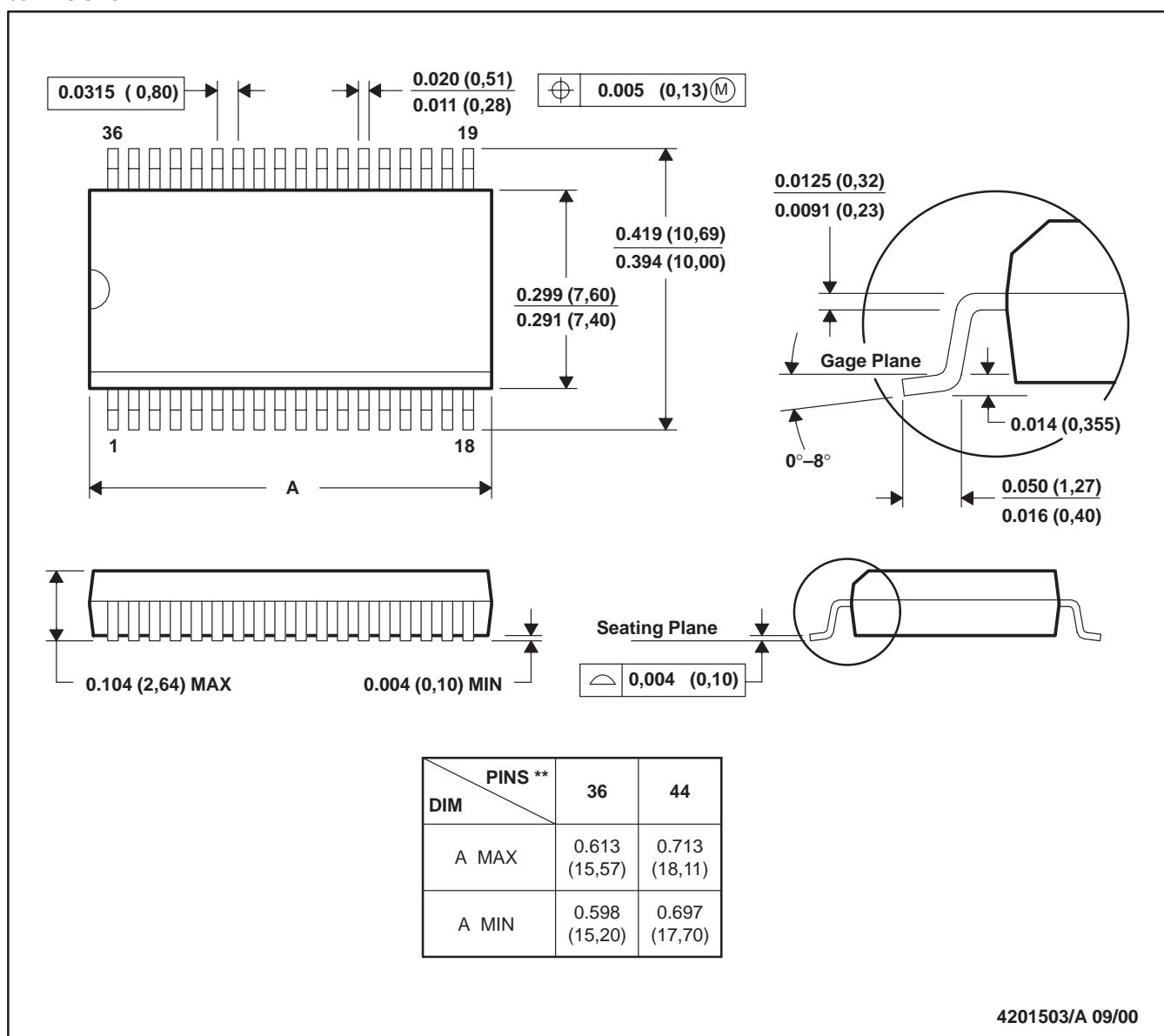
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## DCE (R-PDSO-G\*\*)

36 PINS SHOWN

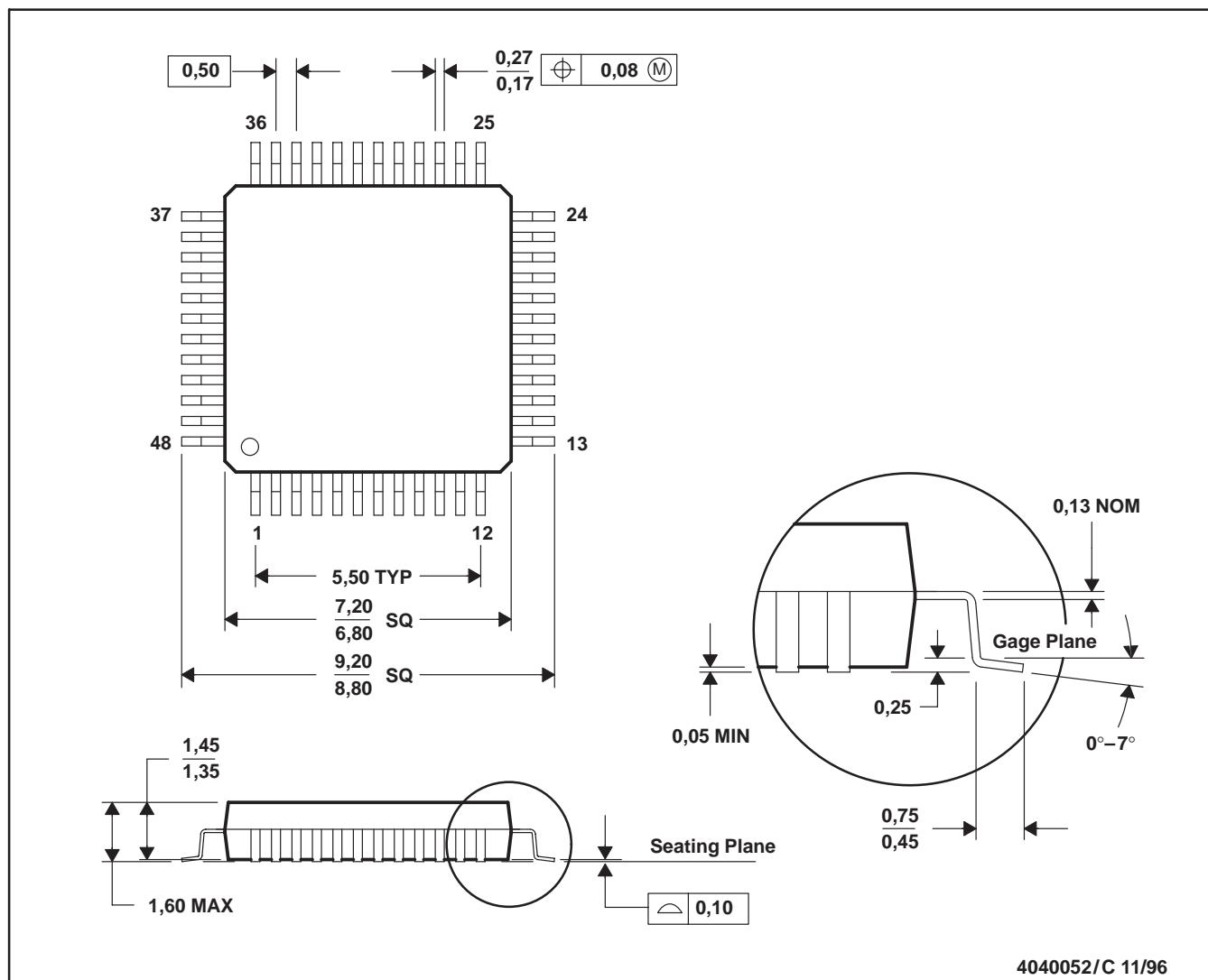
## PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).

## PT (S-PQFP-G48)

## PLASTIC QUAD FLATPACK



NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Falls within JEDEC MS-026
- This may also be a thermally enhanced plastic package with leads connected to the die pads.

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