

FEATURES

Low V_{OS} (V_{BE} Match): 40 μV typ, 100 μV max

Low TCV_{OS} : 0.5 $\mu\text{V}/^\circ\text{C}$ max

High h_{FE} : 500 min

Excellent h_{FE} Linearity from 10 nA to 10 mA

Low Noise Voltage: 0.23 μV p-p—0.1 Hz to 10 Hz

High Breakdown: 45 V min

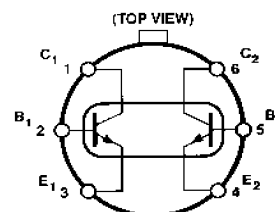
Available in Die Form

PRODUCT DESCRIPTION

The MAT01 is a monolithic dual NPN transistor. An exclusive Silicon Nitride "Triple-Passivation" process provides excellent stability of critical parameters over both temperature and time. Matching characteristics include offset voltage of 40 μV , temperature drift of 0.15 $\mu\text{V}/^\circ\text{C}$, and h_{FE} matching of 0.7%. Very high h_{FE} is provided over a six decade range of collector current, including an exceptional h_{FE} of 590 at a collector current of only 10 nA. The high gain at low collector current makes the MAT01 ideal for use in low power, low level input stages.

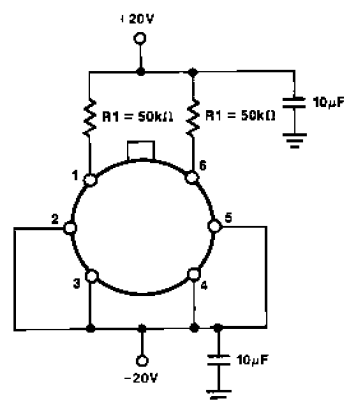
PIN CONNECTION

TO-78
(H Suffix)



NOTE: Substrate is connected to case.

BURN-IN CIRCUIT



REV. A

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MAT01—SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ $V_{CB} = 15\text{ V}$, $I_C = 10\text{ }\mu\text{A}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT01AH			MAT01GH			Units
			Min	Typ	Max	Min	Typ	Min	
Breakdown Voltage	BV_{CEO}	$I_C = 100\text{ }\mu\text{A}$	45			45			V
Offset Voltage	V_{OS}			0.04	0.1		0.10	0.5	mV
Offset Voltage Stability									
First Month	V_{OS}/Time	(Note 1)		2.0			2.0		$\mu\text{V}/\text{Mo}$
Long Term		(Note 2)		0.2			0.2		$\mu\text{V}/\text{Mo}$
Offset Current	I_{OS}			0.1	0.6		0.2	3.2	nA
Bias Current	I_B			13	20		18	40	nA
Current Gain	h_{FE}	$I_C = 10\text{ nA}$		590			430		
		$I_C = 10\text{ }\mu\text{A}$	500	770		250	560		
		$I_C = 10\text{ mA}$		840			610		
Current Gain Match	Δh_{FE}	$I_C = 10\text{ }\mu\text{A}$		0.7	3.0		1.0	8.0	%
		$100\text{ nA} \leq I_C \leq 10\text{ mA}$		0.8			1.2		%
Low Frequency Noise									
Voltage	$e_n\text{ p-p}$	$0.1\text{ Hz to }10\text{ Hz}^3$		0.23	0.4		0.23	0.4	$\mu\text{V p-p}$
Broadband Noise									
Voltage	$e_n\text{ rms}$	$1\text{ Hz to }10\text{ kHz}$		0.60			0.60		$\mu\text{V rms}$
Noise Voltage									
Density	e_n	$f_O = 10\text{ Hz}^3$		7.0	9.0		7.0	9.0	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 100\text{ Hz}^3$		6.1	7.6		6.1	7.6	$\text{nV}/\sqrt{\text{Hz}}$
		$f_O = 1000\text{ Hz}^3$		6.0	7.5		6.0	7.5	$\text{nV}/\sqrt{\text{Hz}}$
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30\text{ V}$		0.5	3.0		0.8	8.0	$\mu\text{V}/\text{V}$
Offset Current Change	$\Delta I_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30\text{ V}$		2	15		3	70	pA/V
Collector-Base									
Leakage Current	I_{CBO}	$V_{CB} = 30\text{ V}$, $I_E = 0^4$		15	50		25	200	pA
Collector-Emitter									
Leakage Current	I_{CES}	$V_{CE} = 30\text{ V}$, $V_{BE} = 0^{4,5}$		50	200		90	400	pA
Collector-Collector									
Leakage Current	I_{CC}	$V_{CC} = 30\text{ V}^5$		20	200		30	400	pA
Collector Saturation	$V_{CE(\text{SAT})}$	$I_B = 0.1\text{ mA}$, $I_C = 1\text{ mA}$		0.12	0.20		0.12	0.25	V
Voltage		$I_B = 1\text{ mA}$, $I_C = 10\text{ mA}$		0.8			0.8		V
Gain-Bandwidth Product	f_T	$V_{CE} = 10\text{ V}$, $I_C = 10\text{ mA}$		450			450		MHz
Output Capacitance	C_{OB}	$V_{CB} = 15\text{ V}$, $I_E = 0$		2.8			2.8		pF
Collector-Collector									
Capacitance	C_{CC}	$V_{CC} = 0$		8.5			8.5		pF

ELECTRICAL CHARACTERISTICS (@ $V_{CB} = 15\text{ V}$, $I_C = 10\text{ }\mu\text{A}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT01AH			MAT01GH			Units
			Min	Typ	Max	Min	Typ	Min	
Offset Voltage	V_{OS}			0.06	0.15		0.14	0.70	mV
Average Offset									
Voltage Drift	TCV_{OS}	(Note 6)		0.15	0.50		0.35	1.8	$\mu\text{V}/^\circ\text{C}$
Offset Current	I_{OS}			0.9	8.0		1.5	15.0	nA
Average Offset									
Current Drift	TCI_{OS}	(Note 7)		10	90		15	150	$\text{pA}/^\circ\text{C}$
Bias Current	I_B			28	60		36	130	nA
Current Gain	h_{FE}		167	400		77	300		
Collector-Base	I_{CBO}	$T_A = 125^\circ\text{C}$, $V_{CB} = 30\text{ V}$, $I_E = 0^4$		15	80		25	200	nA
Collector-Emitter	I_{CES}	$T_A = 125^\circ\text{C}$, $V_{CE} = 30\text{ V}$, $V_{BE} = 0^{4,6}$		50	300		90	400	nA
Collector-Collector	I_{CC}	$T_A = 125^\circ\text{C}$, $V_{CC} = 30\text{ V}$, (Note 6)		30	200		50	400	nA
Leakage Current									

TYPICAL ELECTRICAL CHARACTERISTICS (@ $V_{CB} = 15\text{ V}$ and $I_C = 10\text{ }\mu\text{A}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT01N Typical	Units
Average Offset Voltage Drift	TCV_{OS}		0.35	$\mu\text{V}/^\circ\text{C}$
Average Offset Current Drift	TCI_{OS}		15	$\text{pA}/^\circ\text{C}$
Collector-Emitter-Leakage Current	I_{CES}	$V_{CE} = 30\text{ V}$, $V_{BE} = 0$	90	pA
Collector-Base-Leakage Current	I_{CBO}	$V_{CB} = 30\text{ V}$, $I_E = 0$	25	pA
Gain Bandwidth Product	f_T	$V_{CE} = 10\text{ V}$, $I_C = 10\text{ mA}$	450	MHz
Offset Voltage Stability	$\Delta V_{OS}/T$	First Month (Note 1)	2.0	$\mu\text{V}/\text{Mo}$
		Long-Term (Note 2)	0.2	$\mu\text{V}/\text{Mo}$

NOTES

¹Exclude first hour of operation to allow for stabilization.²Parameter describes long-term average drift after first month of operation.³Sample tested.⁴The collector-base (I_{CBO}) and collector-emitter (I_{CES}) leakage currents may be reduced by a factor of two to ten times by connecting the substrate (package) to a potential which is lower than either collector voltage.⁵ I_{CC} and I_{CES} are guaranteed by measurement of I_{CBO} .⁶Guaranteed by V_{OS} test ($TCV_{OS} \equiv \frac{V_{OS}}{T}$ for $V_{OS} \ll V_{BE}$) $T = 298^\circ\text{K}$ for $T_A = 25^\circ\text{C}$.⁷Guaranteed by I_{OS} test limits over temperature.

Specifications subject to change without notice.

WAFER TEST LIMITS (@ $V_{CB} = 15\text{ V}$, $I_C = 10\text{ }\mu\text{A}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.)

Parameter	Symbol	Conditions	MAT01N Limits	Units
Breakdown Voltage	BV_{CEO}	$I_C = 100\text{ }\mu\text{A}$	45	V min
Offset Voltage	V_{OS}		0.5	mV max
Offset Current	I_{OS}		3.2	nA max
Bias Current	I_B		40	nA max
Current Gain	h_{FE}		250	min
Current Gain Match	Δh_{FE}		8.0	$\% \text{ max}$
Offset Voltage Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30\text{ V}$	8.0	$\mu\text{V}/\text{V max}$
Offset Current Change	$\Delta V_{OS}/\Delta V_{CB}$	$0 \leq V_{CB} \leq 30\text{ V}$	70	$\text{pA}/\text{V max}$
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_B = 0.1\text{ mA}$, $I_C = 1\text{ mA}$	0.25	V max

NOTE

Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

MAT01

ABSOLUTE MAXIMUM RATINGS¹

Collector-Base Voltage (BV _{CBO})	
MAT01AH, GH, N	45 V
Collector-Emitter Voltage (BV _{CBO})	
MAT01AH, GH, N	45 V
Collector-Collector Voltage (BV _{CC})	
MAT01AH, GH, N	45 V
Emitter-Emitter Voltage (BV _{EE})	
MAT01AH, GH, N	45 V
Emitter-Base Voltage (BV _{EBO}) ²	5 V
Collector Current (I _C)	25 mA
Emitter Current (I _E)	25 mA
Total Power Dissipation	
Case Temperature ≤ 40°C ³	1.8 W
Ambient Temperature ≤ 70°C ⁴	500 mW
Operating Ambient Temperature	–55°C to +125°C
Operating Junction Temperature	–55°C to +150°C

Storage Temperature	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	+300°C
DICE Junction Temperature	–65°C to +150°C

NOTES

¹Absolute maximum ratings apply to both DICE and packaged devices.

²Application of reverse bias voltages in excess of rating shown can result in degradation of h_{FE} and h_{FE} matching characteristics. Do not attempt to measure BV_{EBO} greater than the 5 V rating shown.

³Rating applies to applications using heat sinking to control case temperature. Derate linearity at 16.4 mW/°C for case temperatures above 40°C.

⁴Rating applies to applications not using heat sinking; device in free air only. Derate linearity at 6.3 mW/°C for ambient temperatures above 70°C.

ORDERING GUIDE¹

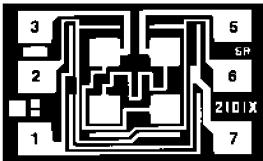
Model	V _{OS} max (T _A = +25°C)	Temperature Range	Package Option
MAT01AH ²	0.1 mV	–55°C to +125°C	TO-78
MAT01GH	0.5 mV	–55°C to +125°C	TO-78

NOTES

¹Burn-in is available on commercial and industrial temperature range parts in TO-can packages.

²For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.

DICE CHARACTERISTICS



- 1. COLLECTOR (1)
- 2. BASE (1)
- 3. EMITTER (1)
- 5. EMITTER (2)
- 6. BASE (2)
- 7. COLLECTOR (2)

DIE SIZE 0.035 × 0.025 inch, 875 sq. mils
(0.89 × 0.64 mm, 0.58 sq. mm)

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the MAT01 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



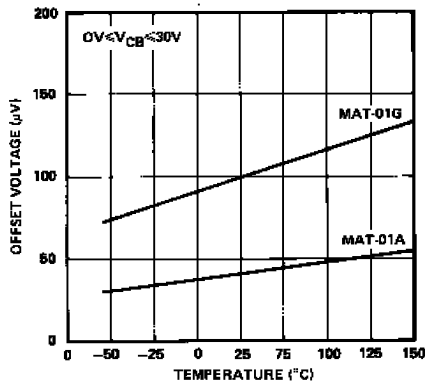


Figure 1. Offset Voltage vs. Temperature

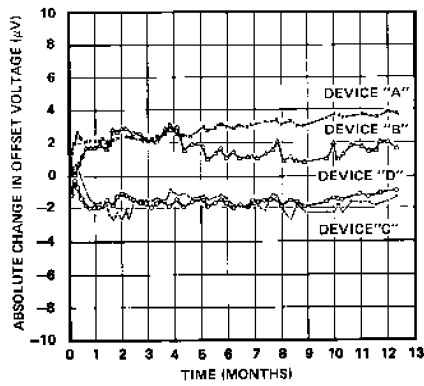


Figure 4. Offset Voltage vs. Time

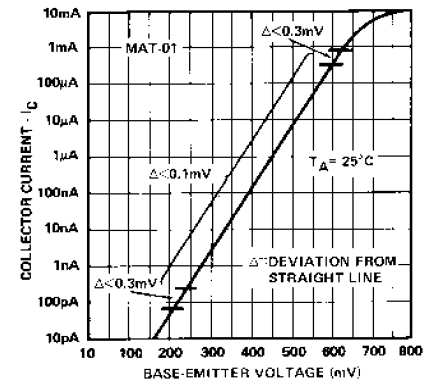


Figure 7. Base-Emitter Voltage vs. Collector Current

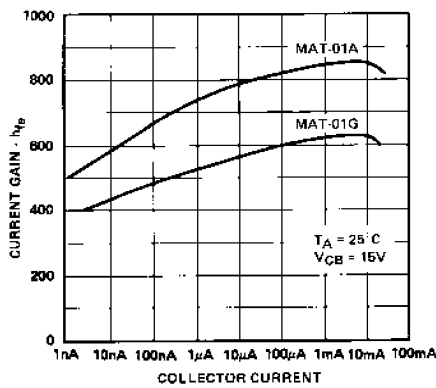


Figure 2. Current Gain vs. Collector Current

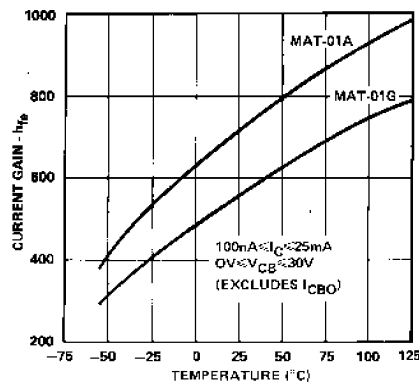


Figure 5. Current Gain vs. Temperature

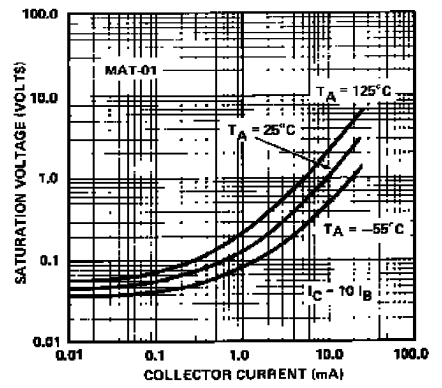


Figure 8. Saturation Voltage vs. Collector Current

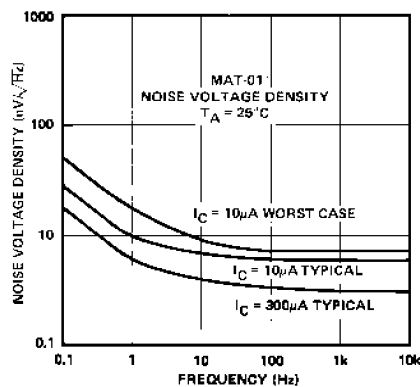


Figure 3. Noise Voltage

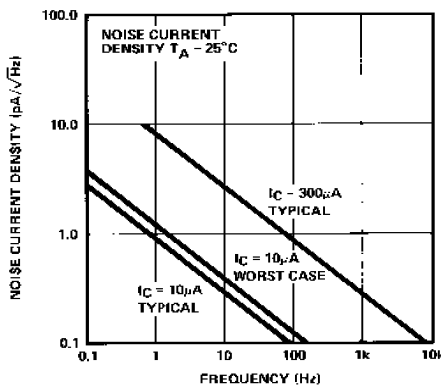


Figure 6. Noise Current Density

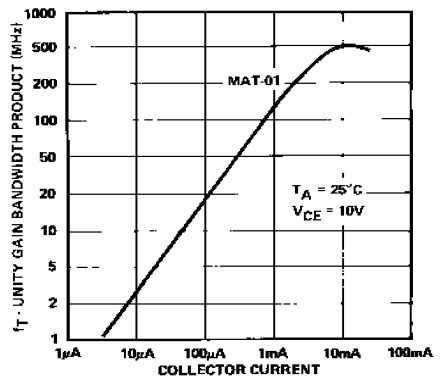
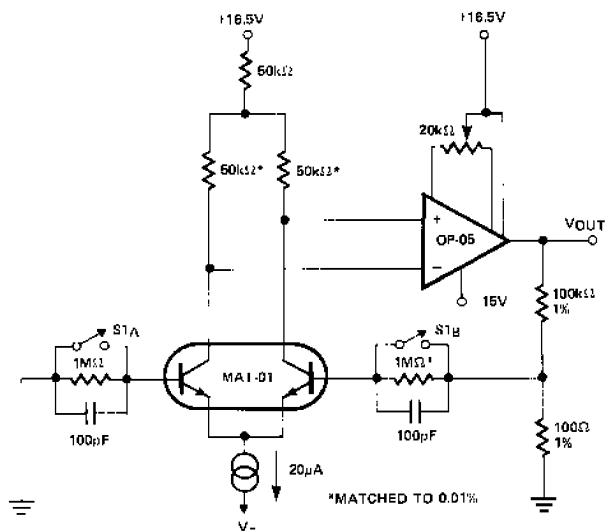


Figure 9. Gain-Bandwidth vs. Collector Current

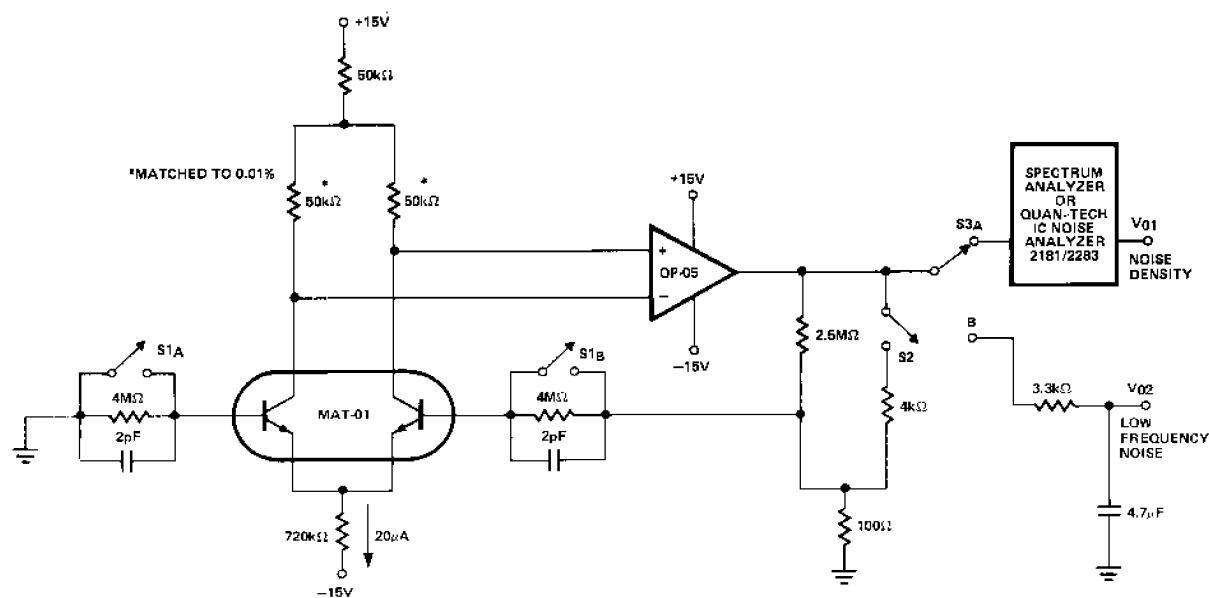
MAT01

MAT01 TEST CIRCUITS



TEST	SI _A	SI _B	UNITS
V _{OS}	X	X	V _{OUT1} 1 volt per mV
I _{OS}	O	O	V _{OUT2} - V _{OUT1} 1 volt per nA

Figure 10. MAT01 Matching Measurement Circuit



TEST	SI _A	SI _B	S ₂	S ₃	READING
Noise Voltage Density (Per Transistor)	X	X	X	A	$V_{01}/\sqrt{2}$
Noise Current Density (Per Transistor)	O	O	X	A	$V_{01}/(\sqrt{2} \times 4M\Omega)$
Low Frequency Noise (Referred to Input)	X	X	O	B	$\frac{V_{02} \text{ PEAK-TO-PEAK}}{25,000}$

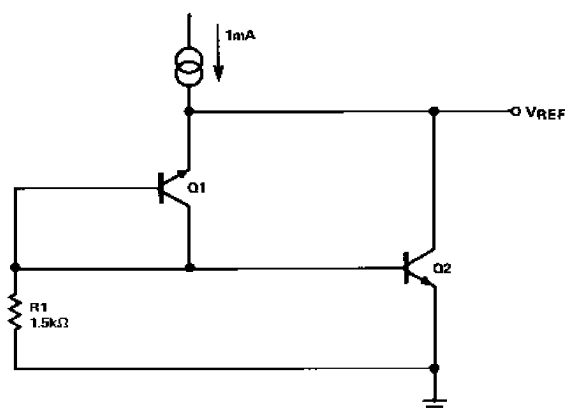
Figure 11. MAT01 Noise Measurement Circuit

APPLICATION NOTES

Application of reverse bias voltages to the emitter-base junctions in excess of ratings (5 V) may result in degradation of h_{FE} and h_{FE} matching characteristics. Circuit designs should be checked to ensure that reverse bias voltages above 5 V cannot be applied during such transient conditions as at circuit turn-on and turn-off.

Stray thermoelectric voltages generated by dissimilar metals at the contacts to the input terminals can prevent realization of the predicted drift performance. Both input terminals should be maintained at the same temperature, preferably close to the temperature of the device's package.

TYPICAL APPLICATIONS



$V_{REF} \sim 7.0V$
 $TCV_{REF} \sim 10ppm/^{\circ}C$
 $R_O \sim 40\Omega$
 R_1 MAY BE ADJUSTED TO MINIMIZE TCV_{REF} . INCREASING R_1 WILL CAUSE A POSITIVE CHANGE IN TCV_{REF} .
 NOTE: h_{FE} OF Q1 WILL BE REDUCED BY OPERATION OF BREAKDOWN MODE.

Figure 12. Precision Reference

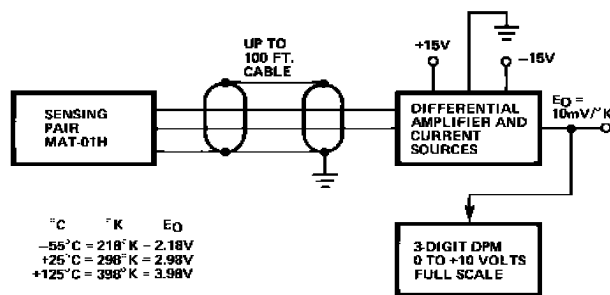
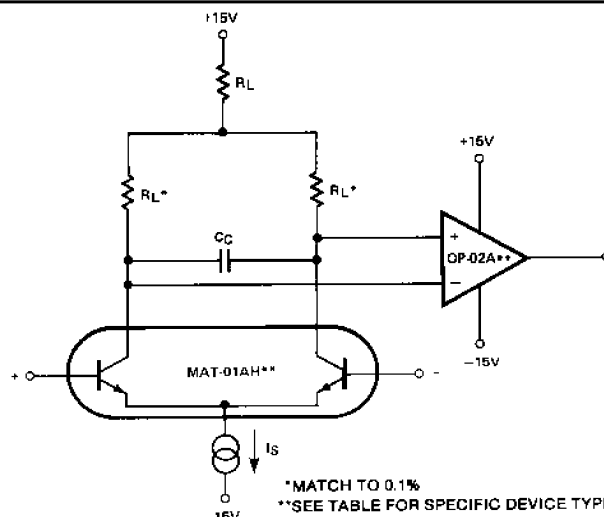


Figure 13. Basic Digital Thermometer Readout in Degrees Kelvin ($^{\circ}K$)



THIS CONFIGURATION CAN ALSO BE USED WITH THE LOW POWER OP-21 OR MICROPOWER OP-22 TO ACHIEVE A LOW NOISE AND LOW POWER PRECISION OP-AMP.

	MAT-01AH OP-02A	MAT-01AH OP-02A	MAT-01GH OP-02	MAT-01GH OP-02
V_{OS} Maximum	0.15mV	0.27mV	0.65mV	1.2mV
TCV_{OS} Maximum	$0.6\mu V/^{\circ}C$	$1\mu V/^{\circ}C$	$2\mu V/^{\circ}C$	$4\mu V/^{\circ}C$
I_{OS} Maximum	0.8nA	0.1nA	3.2nA	0.32nA
I_B Maximum	20nA	2nA	40nA	4nA
Gain Minimum	2,000,000	2,000,000	800,000	800,000
I_S	20 μA	2 μA	20 μA	2 μA
R_L	100k Ω	1M Ω	100k Ω	1M Ω

Figure 14. Precision Operational Amplifiers

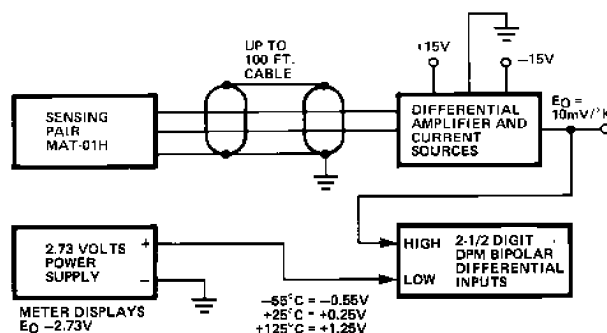
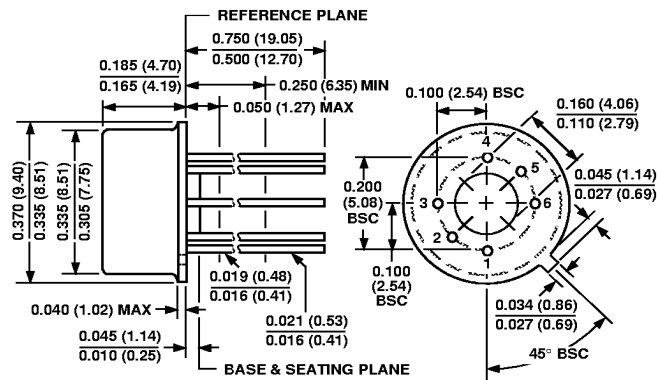


Figure 15. Digital Thermometer with Readout in $^{\circ}C$

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

H-06A
6-Lead Metal Can (TO-78)



3127-0-6/97

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