

OptiMOS[®] -T PN Half Bridge



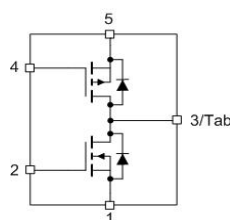
Features

- Dual p- and n-channel MOSFET
- Automotive AEC Q101 qualified
- Green package (RoHS compliant)
- Ultra low $R_{DS(on)}$
- 150 °C operating temperature

Product Summary

	P	N	
V_{DS}	-30	55	V
$R_{DS(on),max}$	13	12	mΩ
I_D	-40	40	A

PG-TO220-5-13



Type	Package	Marking
BTS7904S	PG-TO220-5-13	7904S

Maximum ratings, at $T_J=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value		Unit
			P	N	
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$	-40	40	A
		$T_C=100\text{ °C}$	-40	40	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	-160	160	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=\pm 20\text{ A}$	350	200	mJ
Avalanche current, single pulse	I_{AS}		-40	40	A
Gate source voltage	V_{GS}		-16 / +5	+16 / -16 ³⁾	V
Power dissipation ²⁾	P_{tot}	$T_C=25\text{ °C}$	96	69	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150		°C
IEC climatic category; DIN IEC 68-1			55/150/56		

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Thermal characteristics

Thermal resistance, junction - case	P	R_{thJC}		-	-	1.3	K/W
	N			-	-	1.8	
SMD version, device on PCB ⁵⁾		R_{thJA}	minimal footprint	-	-	62	
			6 cm ² cooling area ⁴⁾	-	-	45	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	P	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=-1\text{ mA}$	-30	-	-	V
	N		$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	55	-	-	
Gate threshold voltage	P	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=-70\text{ }\mu\text{A}$	-1	-1.5	-2.1	
	N		$V_{DS}=V_{GS}, I_D=40\text{ }\mu\text{A}$	1.2	1.7	2.2	
Zero gate voltage drain current	P	I_{DSS}	$V_{DS}=-18\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	-0.01	-1	μA
			$V_{DS}=-18\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	-1	-100	
	N		$V_{DS}=18\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	
			$V_{DS}=18\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}$	-	1	100	
Gate-source leakage current	P	I_{GSS}	$V_{GS}=-16\text{ V}, V_{DS}=0\text{ V}$	-	-10	-100	nA
	N		$V_{GS}=16\text{ V}, V_{DS}=0\text{ V}$	-	1	100	
Drain-source on-state resistance	P	$R_{DS(on)}$	$V_{GS}=-10\text{ V}, I_D=-20\text{ A}$	-	7.2	13	m Ω
	N		$V_{GS}=10\text{ V}, I_D=20\text{ A}$	-	9.7	12	
	P		$V_{GS}=-4.5\text{ V}, I_D=-12.5\text{ A}$	-	17.5	21	
	N		$V_{GS}=4.5\text{ V}, I_D=20\text{ A}$	-	16.8	20.5	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics

Input capacitance	P	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=\pm 25\text{ V},$ $f=1\text{ MHz}$	-	3900	5200	pF
	N			-	4600	6100	
Output capacitance	P	C_{oss}		-	1000	1300	
	N			-	570	760	
Reverse transfer capacitance	P	C_{rss}		-	850	1300	
	N			-	550	820	
Turn-on delay time	P	$t_{d(on)}$		-	22	-	ns
	N			-	15	-	
Rise time	P	t_r		-	94	-	
	N			-	77	-	
Turn-off delay time	P	$t_{d(off)}$		-	104	-	
	N			-	31	-	
Fall time	P	t_f		-	150	-	
	N			-	8	-	

Gate Charge Characteristics²⁾

Gate to source charge	P	Q_{gs}	$V_{DD}=-24\text{ V}, I_D=-40\text{ A},$ $V_{GS}=0\text{ to }-10\text{ V}$	-	-12	-16	nC
Gate to drain charge		Q_{gd}		-	-30	-45	
Switching charge		Q_g		-	-80	-121	
Gate plateau voltage		$V_{plateau}$		-	-3.0	-	
Gate to source charge	N	Q_{gs}	$V_{DD}=44\text{ V}, I_D=40\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	20	27	
Gate to drain charge		Q_{gd}		-	32	48	
Gate charge		Q_g		-	82	123	
Gate plateau voltage		$V_{plateau}$			4.2		

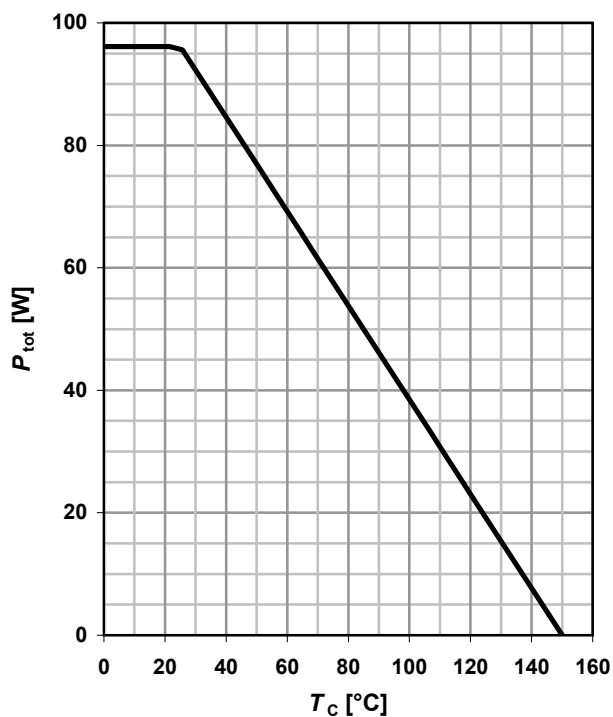
Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Reverse Diode

Diode continuous forward current ²⁾	P	I_S	$T_C=25\text{ °C}$	-	-	-40	A
	N					40	
Diode pulse current	P	$I_{S,pulse}$		-	-	-160	
	N					160	
Diode forward voltage	P	V_{SD}	$V_{GS}=0\text{ V}, I_F=-40\text{ A}, T_j=25\text{ °C}$	-	-1.00	-1.2	V
	N		$V_{GS}=0\text{ V}, I_F=40\text{ A}, T_j=25\text{ °C}$	-	0.90	1.2	
Reverse recovery time ²⁾	P	t_{rr}	$V_R=15\text{ V}, I_F=I_S, di_F/dt=400\text{ A/}\mu\text{s}$	-	41	-	ns
	N			-	47	-	
Reverse recovery charge ²⁾	P	Q_{rr}		-	-40	-	nC
	N			-	50	-	

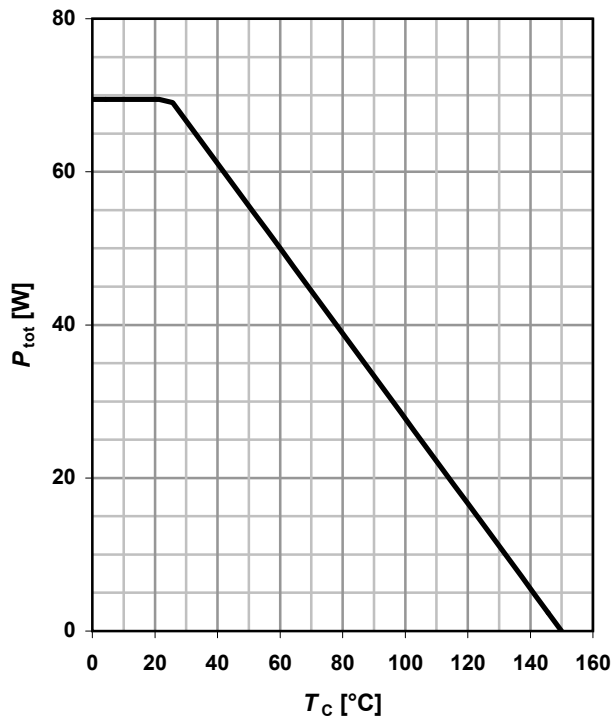
1 Power dissipation (P)

$$P_{\text{tot}} = f(T_C), V_{\text{GS}} \geq 6 \text{ V}$$



2 Power dissipation (N)

$$P_{\text{tot}} = f(T_C), V_{\text{GS}} \geq 6 \text{ V}$$



3 Drain current (P)

$$I_D = f(T_C)$$

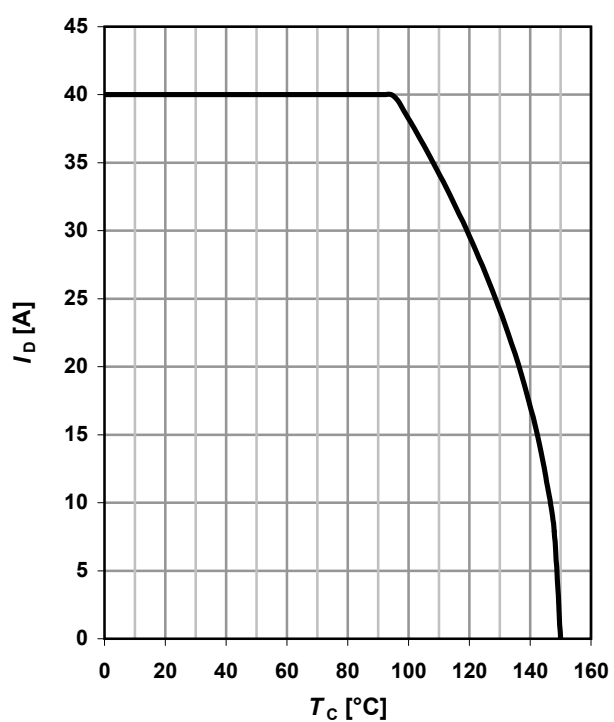
parameter: $V_{\text{GS}} \geq 6 \text{ V}$



4 Drain current (N)

$$I_D = f(T_C)$$

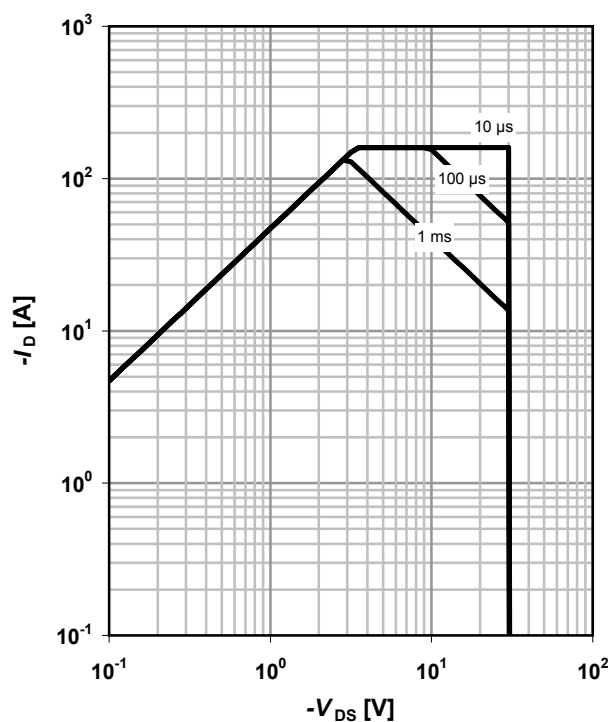
parameter: $V_{\text{GS}} \geq 6 \text{ V}$



5 Safe operating area (P)

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

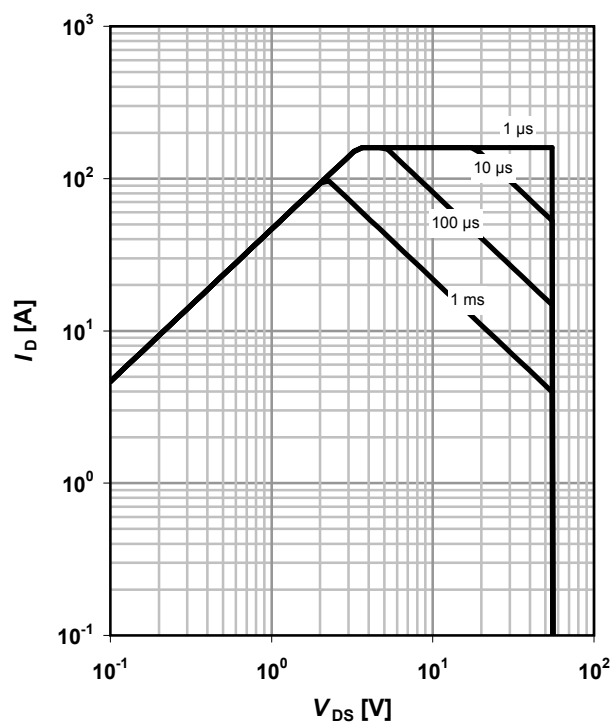
parameter: t_p



6 Safe operating area (N)

$$I_D = f(V_{DS}); T_C = 25^\circ\text{C}; D = 0$$

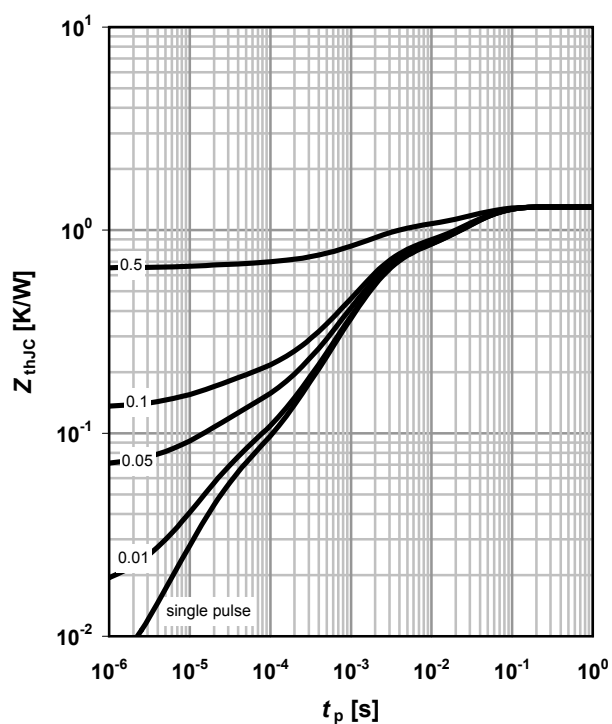
parameter: t_p



7 Max. transient thermal impedance (P)

$$Z_{thJC} = f(t_p)$$

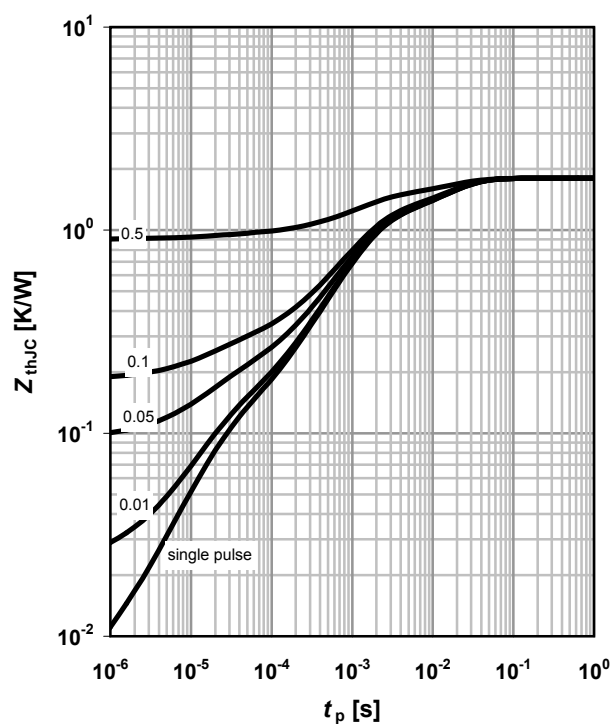
parameter: $D = t_p/T$



8 Max. transient thermal impedance (N)

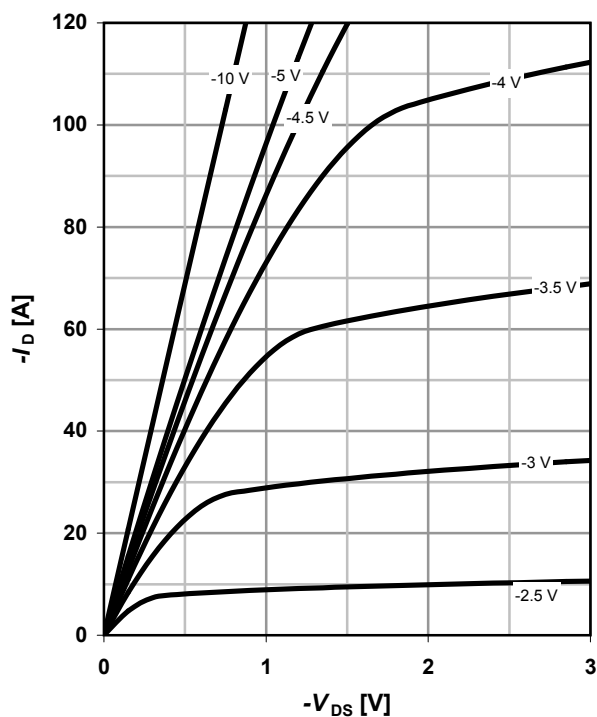
$$Z_{thJC} = f(t_p)$$

parameter: $D = t_p/T$



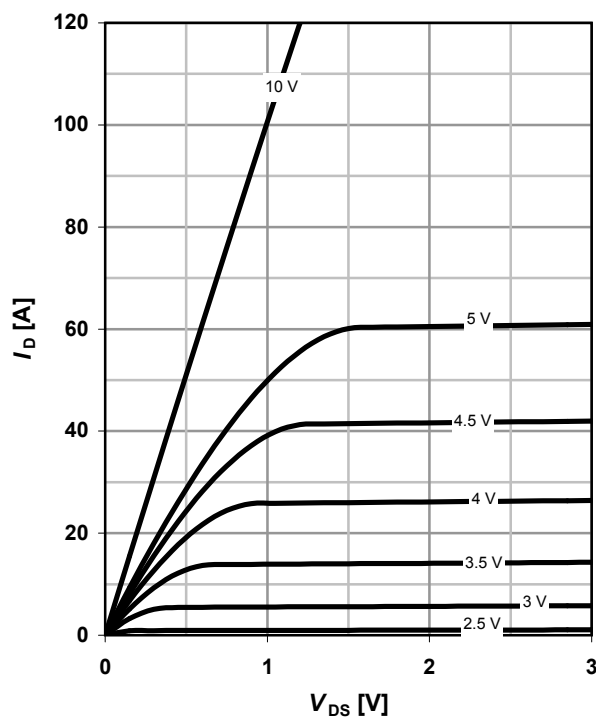
9 Typ. output characteristics (P)

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


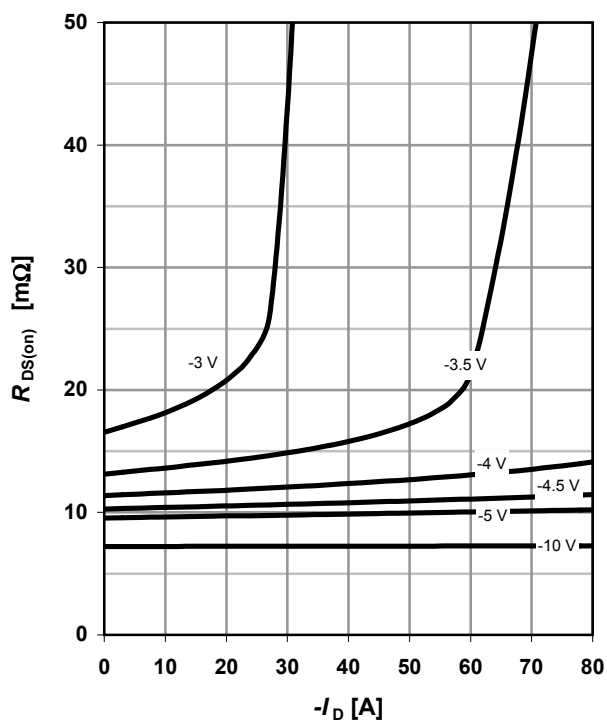
10 Typ. output characteristics (N)

 $I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

parameter: V_{GS}


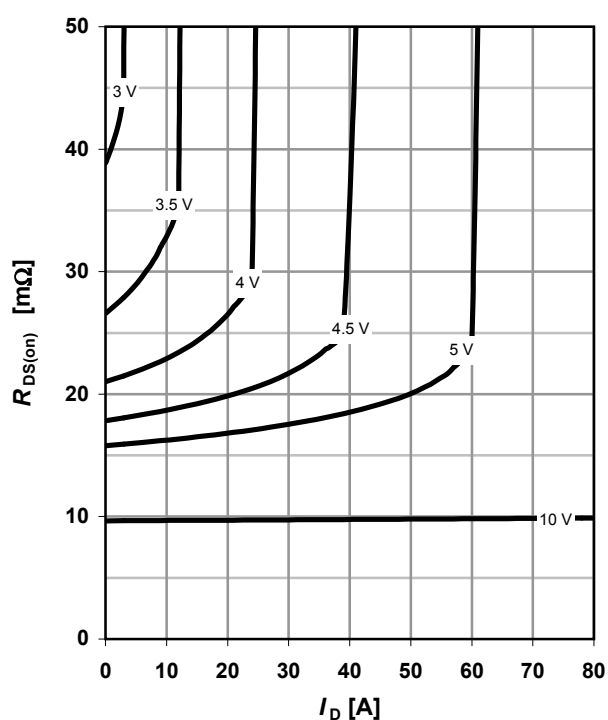
11 Typ. drain-source on resistance (P)

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

parameter: V_{GS}


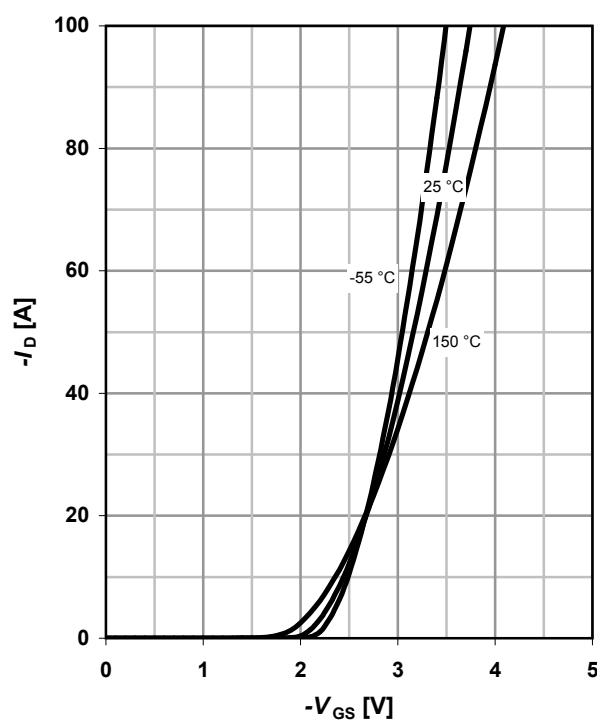
12 Typ. drain-source on resistance (N)

 $R_{DS(on)} = f(I_D); T_j = 25^\circ\text{C}$

parameter: V_{GS}


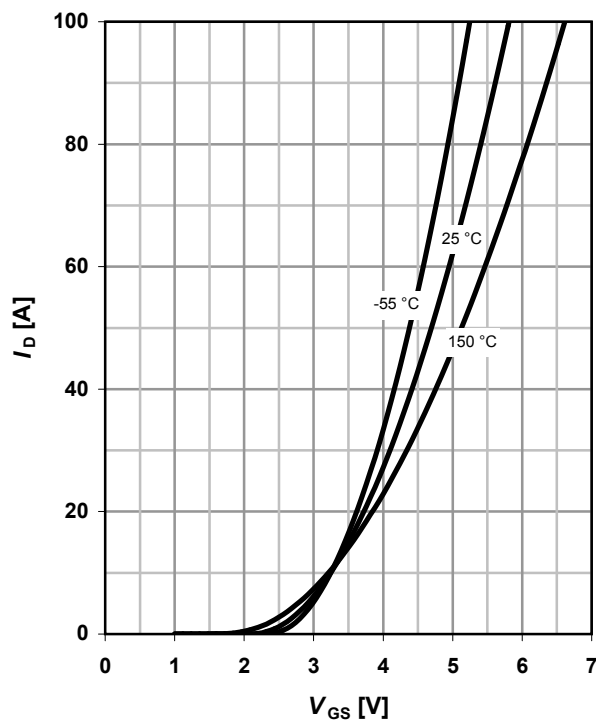
13 Typ. transfer characteristics (P)

 $I_D = f(V_{GS}); V_{DS} = -6 \text{ V}$

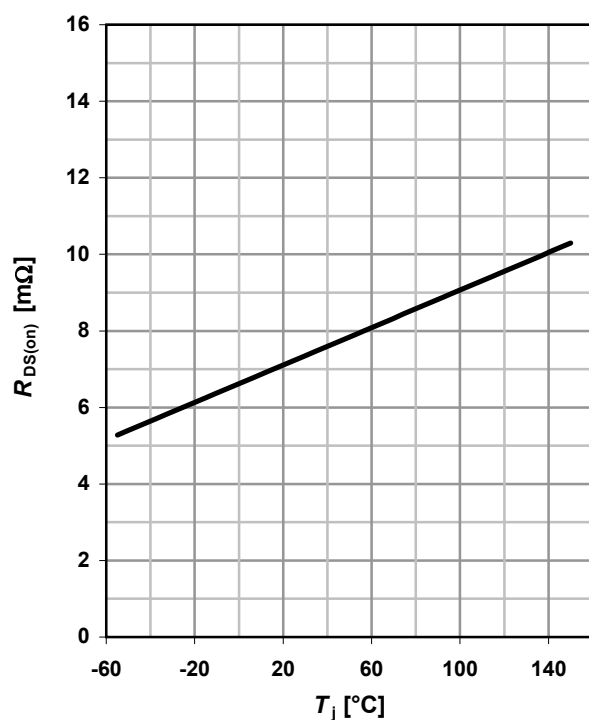
parameter: T_j


14 Typ. transfer characteristics (N)

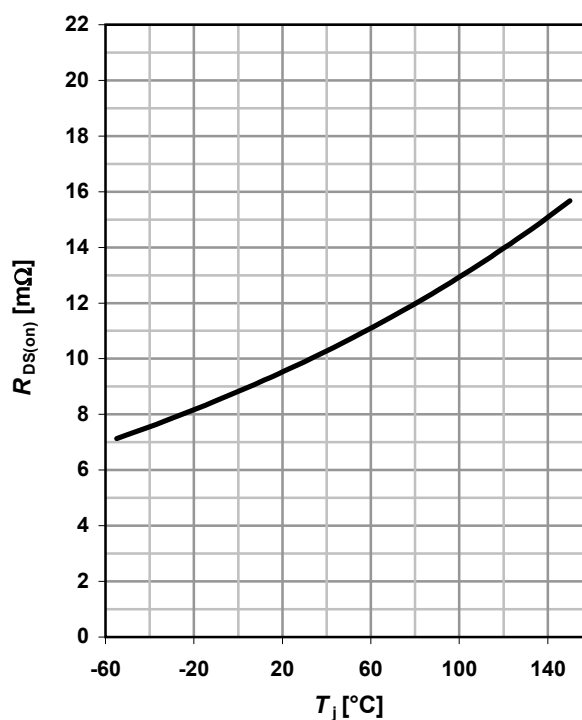
 $I_D = f(V_{GS}); V_{DS} = 6 \text{ V}$

parameter: T_j


15 Drain-source on-state resistance (P)

 $R_{DS(on)} = f(T_j); I_D = -20 \text{ A}; V_{GS} = -10 \text{ V}$


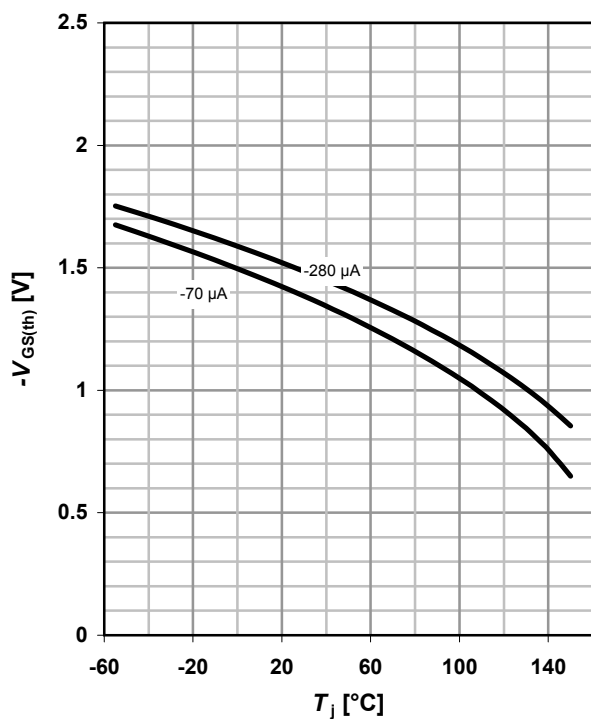
16 Drain-source on-state resistance (N)

 $R_{DS(on)} = f(T_j); I_D = 20 \text{ A}; V_{GS} = 10 \text{ V}$


17 Typ. gate threshold voltage (P)

$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

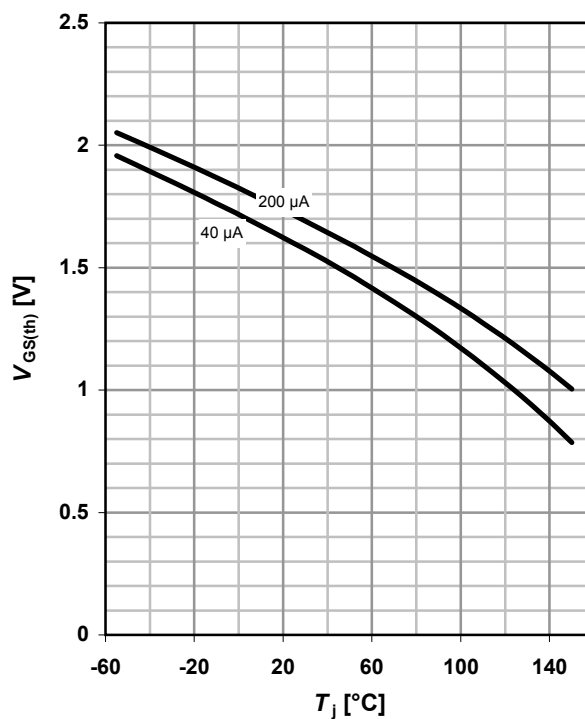
parameter: I_D



18 Typ. gate threshold voltage (N)

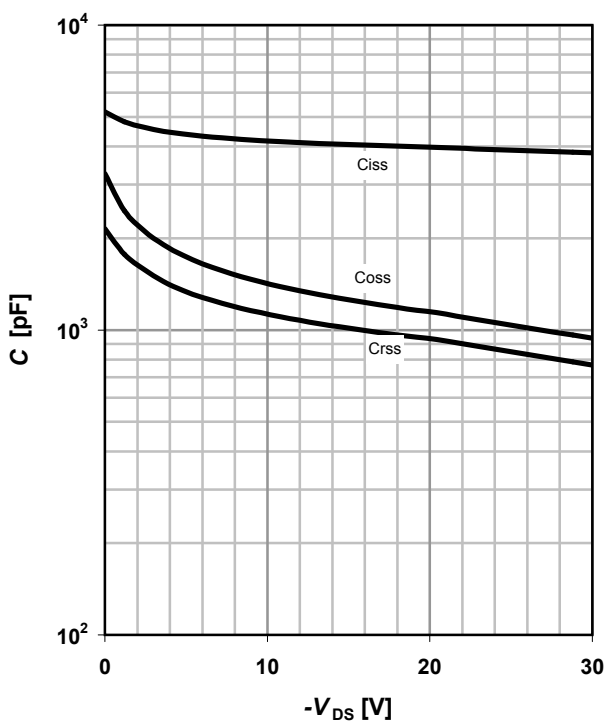
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



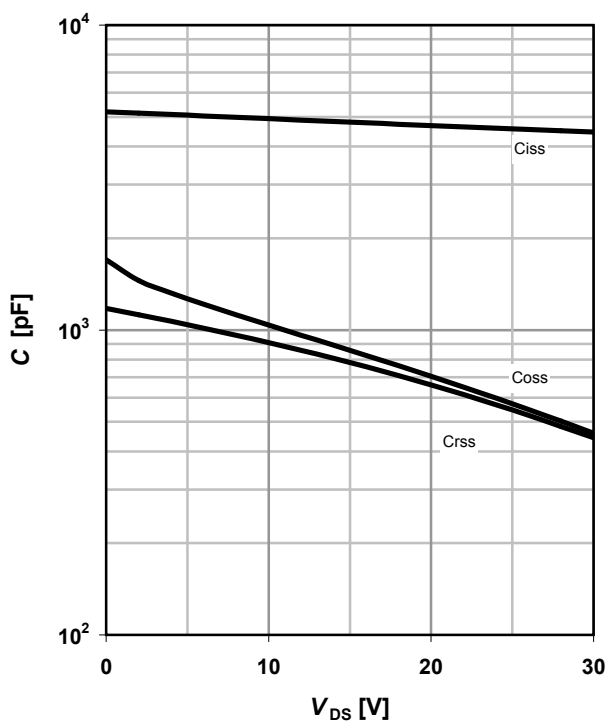
19 Typ. capacitances (P)

$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



20 Typ. capacitances (N)

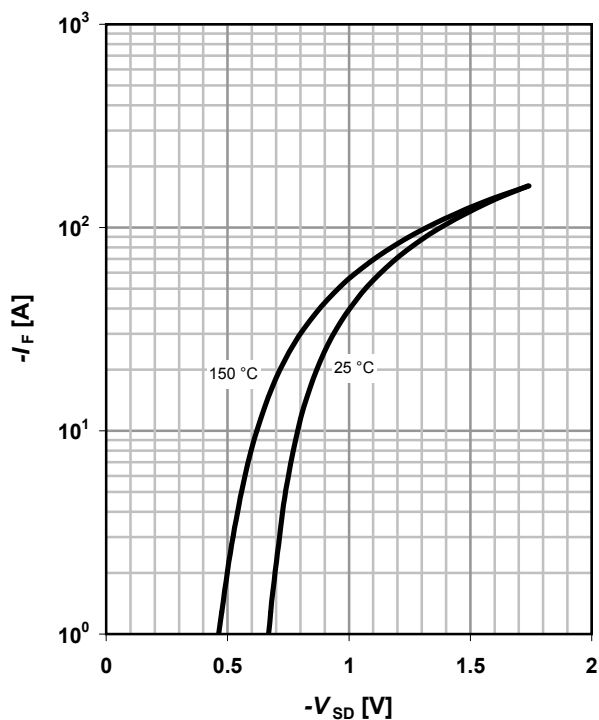
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$



21 Forward characteristics of reverse diode (P)

$$I_F = f(V_{SD})$$

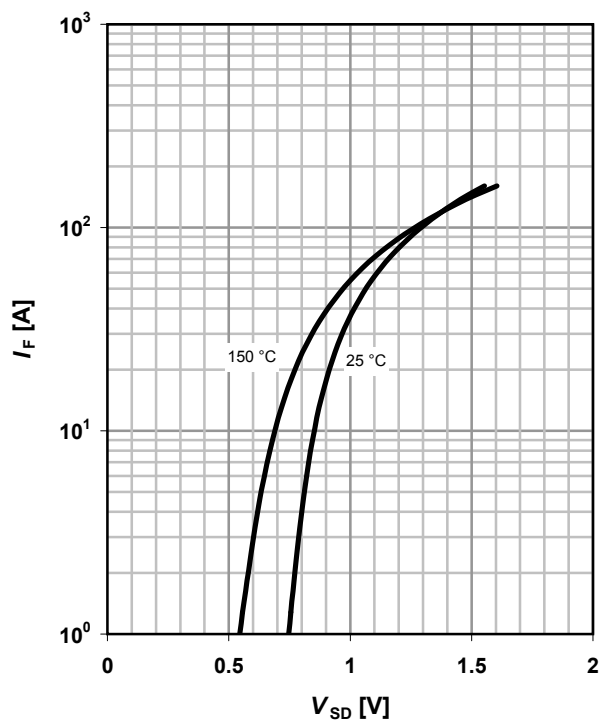
parameter: T_j



22 Forward characteristics of reverse diode (N)

$$I_F = f(V_{SD})$$

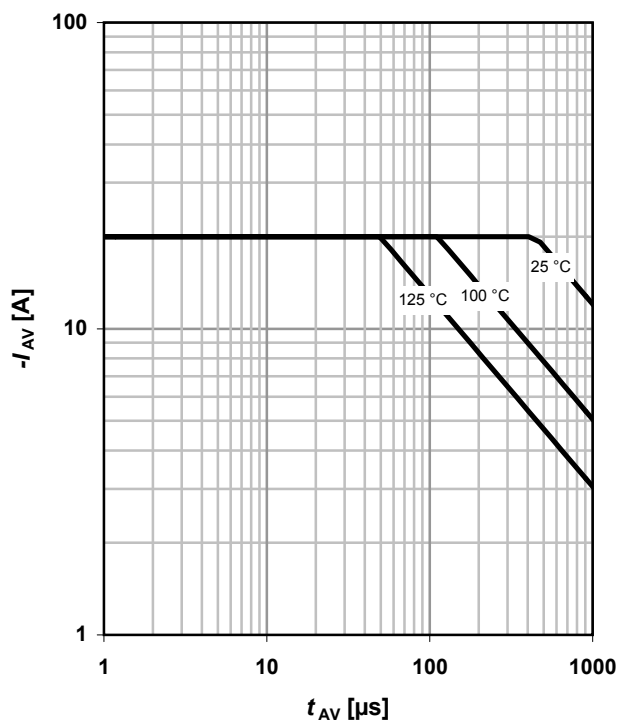
parameter: T_j



23 Avalanche characteristics (P)

$$I_{AS} = f(t_{AV}); R_{GS} = 25 \Omega$$

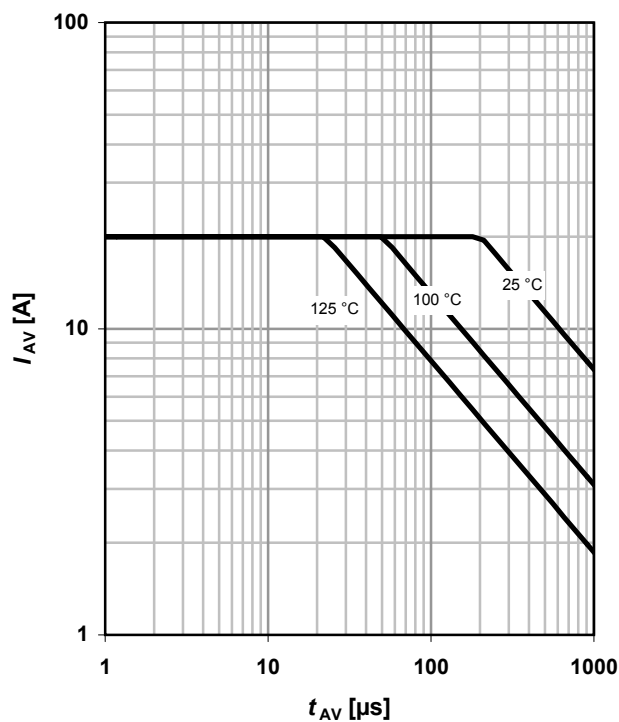
parameter: $T_{j(start)}$



24 Avalanche characteristics (N)

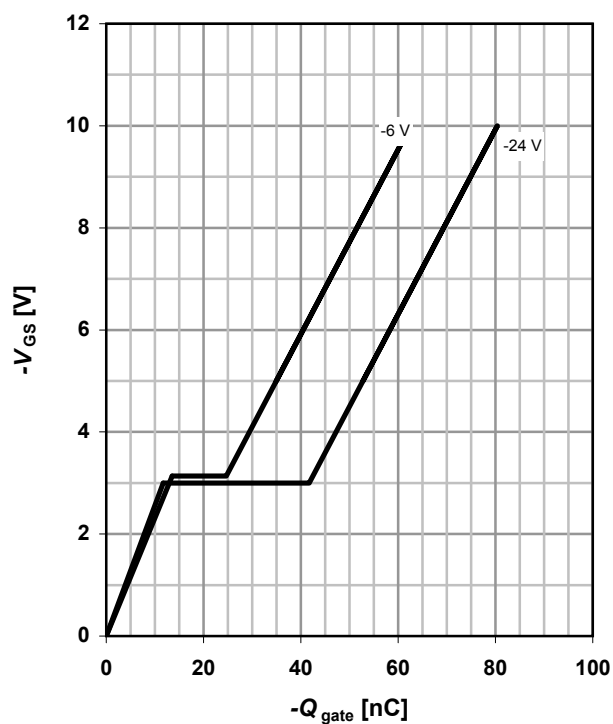
$$I_{AS} = f(t_{AV}); R_{GS} = 25 \Omega$$

parameter: $T_{j(start)}$



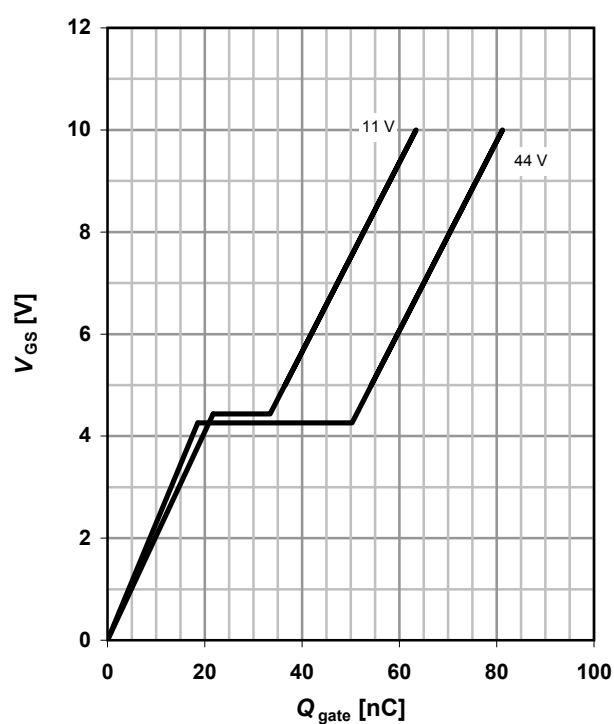
25 Typ. gate charge (P)

 $V_{GS}=f(Q_{gate}); I_D=-40\text{ A pulsed}$

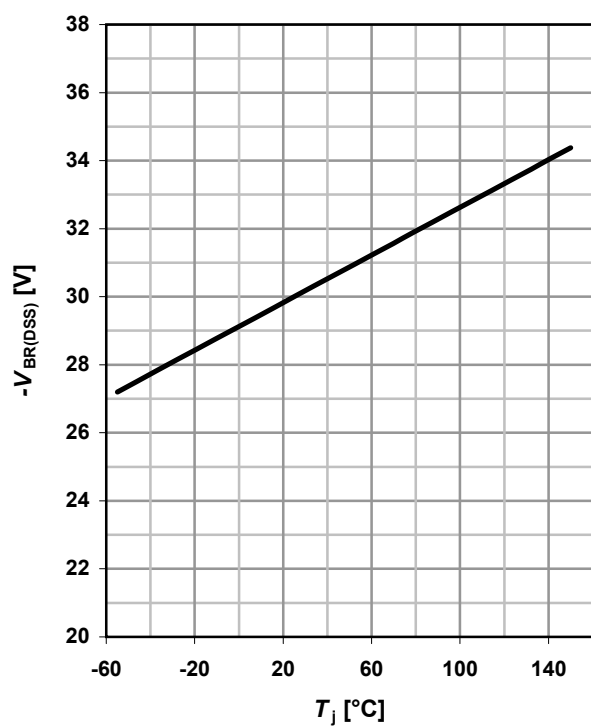
parameter: V_{DD}


26 Typ. gate charge (N)

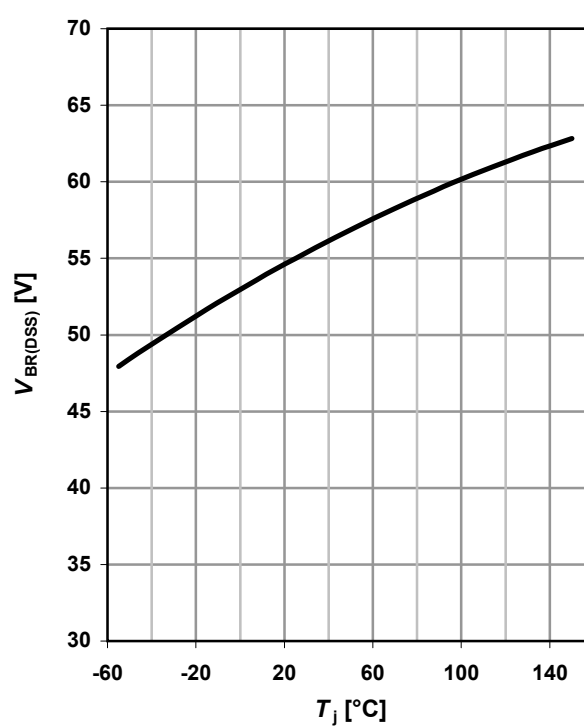
 $V_{GS}=f(Q_{gate}); I_D=40\text{ A pulsed}$

parameter: V_{DD}


27 Drain-source breakdown voltage (P)

 $V_{BR(DSS)}=f(T_j); I_D=-1\text{ mA}$


28 Drain-source breakdown voltage (N)

 $V_{BR(DSS)}=f(T_j); I_D=1\text{ mA}$


Published by
Infineon Technologies AG
81726 Munich, Germany

© Infineon Technologies AG 2008
All Rights Reserved.

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.
Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life.

Revision History

Version	Date	Changes

¹⁾ Current is limited by bondwire.

With an $R_{thJC}(HS)=1.3K/W$ the HS chip is able to carry $I_D=80A$ at $25^{\circ}C$.

With an $R_{thJC}(LS)=1.8K/W$ the LS chip is able to carry $I_D=63A$ at $25^{\circ}C$.

For detailed information see Application Note ANPS071E at www.infineon.com/optimos

²⁾ Defined by design, not subject to production tests

³⁾ Qualified at -5V and +16V.

⁴⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm^2 (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.