

NOT RECOMMENDED FOR NEW DESIGN USE DMP3068L



DMP3130L

P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary

BV _{DSS}	RDS(ON) Max	I _D T _A = +25°C
-30V	$77m\Omega@V_{GS} = -10V$	-3.5A
	$95m\Omega@V_{GS} = -4.5V$	-3.0A
	150mΩ@ V _{GS} = -2.5V	-2.4A

Features and Benefits

- Low On-Resistance
- Low Gate Threshold Voltage
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)
- Qualified to AEC-Q101 Standards for High Reliability
- An Automotive-Compliant Part is Available Under Separate Datasheet (DMP3130LQ)

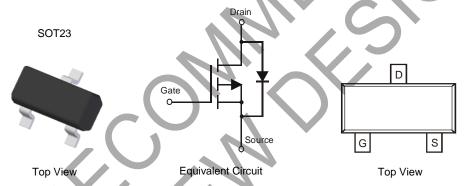
Description and Applications

This new generation MOSFET has been designed to minimize the on-state resistance ($R_{DS(ON)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- DC-DC Converters
- Power Management Functions
- Analog Switch

Mechanical Data

- Case: SOT23
- Case Material: Molded Plastic, "Green" Molding Compound.
 UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 @3
- Terminal Connections: See Diagram
- Weight: 0.008 grams (Approximate)



Ordering Information (Note 4)

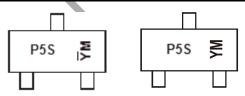
Part Number	Case	Packaging
DMP3130L-7	SOT23	3000/Tape & Reel

Notes:

- 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Shanghai A/T Site

Marking Information



Chengdu A/T Site

P5S = Product Type Marking Code

YM = Date Code Marking for SAT (Shanghai Assembly/ Test Site)

YM = Date Code Marking for CAT (Chengdu Assembly/ Test Site)

Y or \overline{Y} = Year (ex: E = 2017)

M = Month (ex: 9 = September)

Date Code Key

Year	2008	2009	2010	2011	2012	20	13	2014	201	15	2016	2017	2018
Code	V	W	Х	Υ	Z	1	4	В	С	;	D	Е	F
Month	Jan	Feb	Mar	Apr	May	Jun	Ju	ıl Au	g	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8		9	0	N	D



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DMP3130L

Maximum Ratings ($@T_A = +25^{\circ}C$, unless otherwise specified.)

Characteristic		Symbol	Value	Unit	
Drain-Source Voltage		V_{DSS}	-30	V	
Gate-Source Voltage		V _{GSS}	±12	V	
Continuous Drain Current (Note 5) V _{GS} = -4.5V	$T_A = +25$ °C $T_A = +70$ °C	I _D	-3.0 -2.6	А	
Continuous Diam Curient (Note 5) VGS = -4.5V	t<10s	$T_A = +25^{\circ}C$ $T_A = +70^{\circ}C$	I _D	-4.1 -3.2	А
Maximum Continuous Body Diode Forward Current	(Note 5)	Is	-1.6	А	
Pulsed Drain Current (10µs Pulse, Duty Cycle = 1%	<u>(</u>	I _{DM}	-20	Α	

Thermal Characteristics

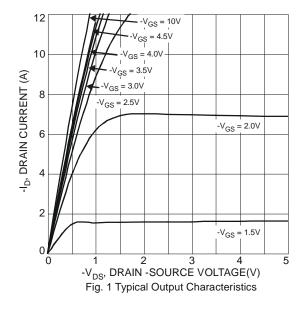
Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	$T_A = +25$ °C	P _D	0.7	W
Total Fower Dissipation (Note 3)	$T_A = +70^{\circ}C$	ı D	0.4	VV
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	$R_{\theta JA}$	184	°C/W
Thermal Resistance, Junction to Ambient (Note 3)	t<10s	$\kappa_{ heta}$ JA	115	C/VV
Total Power Dissipation (Note 6)	$T_A = +25^{\circ}C$	Pn	1.3	W
Total Fower Dissipation (Note o)	T _A = +70°C	PD	0.8	VV
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	D	94	
Thermal Resistance, Junction to Ambient (Note o)	t<10s	$R_{\theta JA}$	61	°C/W
Thermal Resistance, Junction to Case		$R_{ heta JC}$	25	
Operating and Storage Temperature Range		T _J , T _{STG}	-55 to +150	°C

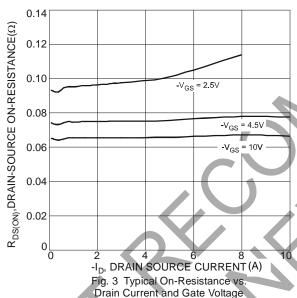
Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	-30	4		V	$V_{GS} = 0V, I_D = -250\mu A$
Zero Gate Voltage Drain Current	IDSS	_	7-1	-1	μA	$V_{DS} = -30V, V_{GS} = 0V$
Gate-Body Leakage	I _{GSS}		1-7	±100	nA	$V_{GS} = \pm 12V, V_{DS} = 0V$
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.6		-1.3	V	$V_{DS} = V_{GS}, I_{D} = -250\mu A$
			59	77		$V_{GS} = -10V, I_D = -4.2A$
Static Drain-Source On-Resistance	R _{DS(ON)}		73	95	$m\Omega$	$V_{GS} = -4.5V$, $I_D = -4A$
		1	115	150		$V_{GS} = -2.5V, I_D = -3A$
Forward Transconductance	g fs		8		S	$V_{DS} = -5V, I_{D} = -4A$
Source-Drain Diode Forward Voltage	V_{SD}		-0.8	-1.25	٧	$V_{GS} = 0V, I_{S} = -3.0A$
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	Ciss		432	864	рF	V 45V V 0V
Output Capacitance	Coss		87	174	рF	$V_{DS} = -15V, V_{GS} = 0V$ f = 1.0MHz
Reverse Transfer Capacitance	C_{rss}		62	124	рF	1 - 1.01VII 12
Gate Resistance	R _G		4.04		Ω	$V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz$
SWITCHING CHARACTERISTICS (Note 8)						
Total Gate Charge	Q_{G}		5.9	11.8		$V_{DS} = -15V$, $V_{GS} = -4.5V$, $I_{D} = -4.0A$
Total Gate Gharge	વહ		12	24	nC	$V_{DS} = -15V$, $V_{GS} = -10V$, $I_{D} = -4.0A$
Gate-Source Charge	Q_{GS}		1.0	2.0	110	Vns = -15V, Vgs = -4.5V, In = -4.0A
Gate-Drain Charge	Q_{GD}		3.1	6.2		$V_{DS} = -15V$, $V_{GS} = -4.5V$, $I_{D} = -4.0A$
Turn-On Delay Time	t _{D(ON)}		4.6	9.2		
Rise Time	t _R		6.5	13.0	nc	$V_{DS} = -15V$, $V_{GS} = -10V$,
Turn-Off Delay Time	t _{D(OFF)}		27.8	55.6	ns	$I_D = -1A, R_G = 6.0\Omega$
Fall Time	t _F	_	15.0	30.0		

Notes:

- 5. Device mounted on FR-4 PC board, with minimum recommended pad layout, single sided.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal vias to bottom layer 1inch square copper plate.
 7. Short duration pulse test used to minimize self-heating effect.
 8. Guaranteed by design. Not subject to production testing.





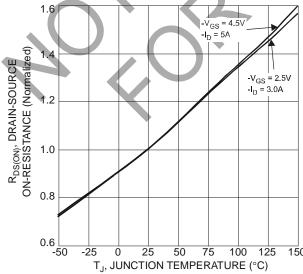
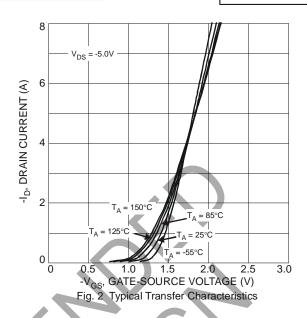
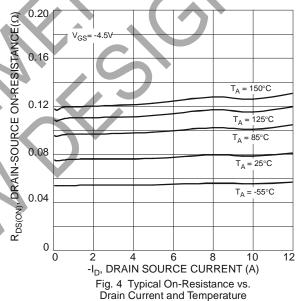


Fig. 5 On-Resistance Variation with Temperature





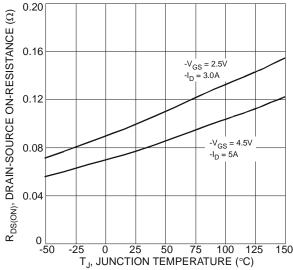


Fig. 6 On-Resistance Variation with Temperature



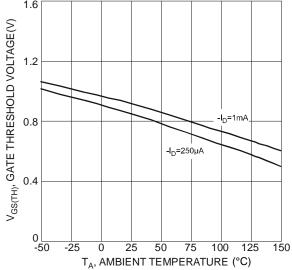
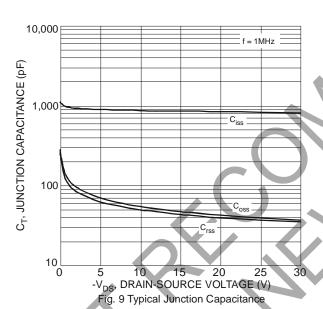
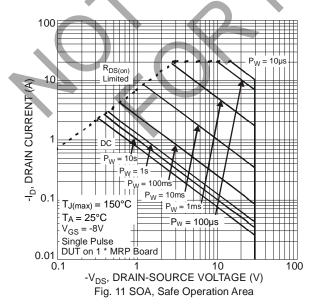
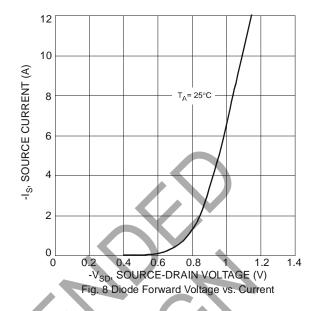
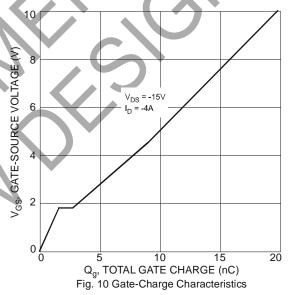


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

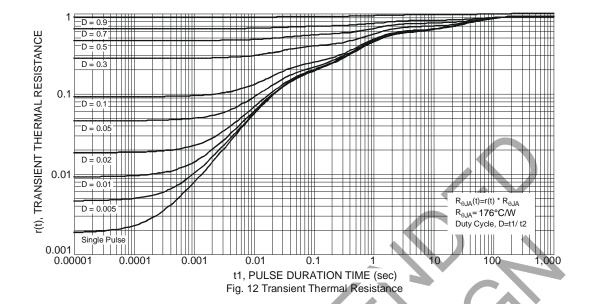










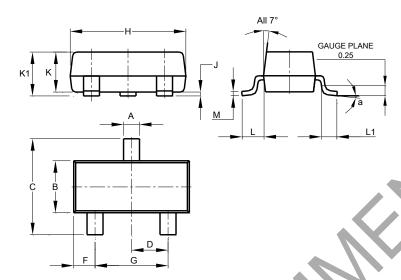




Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SOT23

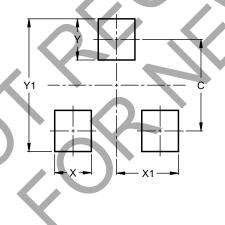


SOT23							
Dim	Min	Max	Тур				
A	0.37	0.51	0.40				
В	1.20	1.40	1.30				
С	2.30	2.50	2.40				
D	0.89	1.03	0.915				
F	0.45	0.60	0.535				
G	1.78	2.05	1.83				
H	2.80	3.00	2.90				
7	0.013	0.10	0.05				
K	0.890	1.00	0.975				
K1	0.903	1.10	1.025				
L	0.45	0.61	0.55				
L1	0.25	0.55	0.40				
М	0.085	0.150	0.110				
а	0°	8°					
All Dimensions in mm							

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.





Dimensions	Value (in mm)
C	2.0
Х	0.8
X1	1.35
Y	0.9
Y1	2.9



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DMP3130L

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