6.5-W MONO CLASS-D AUDIO POWER AMPLIFIER

FEATURES

- **6.5 W Into 8-Ω Load From 12-V Supply (10% THD+N)**
- **Short Circuit Protection (Short to V_{CC}, Short to GND, Short Between Outputs)**
- **Third-Generation Modulation Technique:**
  - **Replaces Large LC Filter With Small, Low-Cost Ferrite Bead Filter in Most Applications**
  - **Improved Efficiency**
  - **Improved SNR**
- **Low Supply Current ... mA Typ at 12 V**
- **Shutdown Control ... < 1μA Typ**

APPLICATIONS

- **LCD Monitors/TVs**
- **Desktop Replacement Notebook PCs**
- **Hands-Free Car Kits**
- **Powered Speakers**

DESCRIPTION

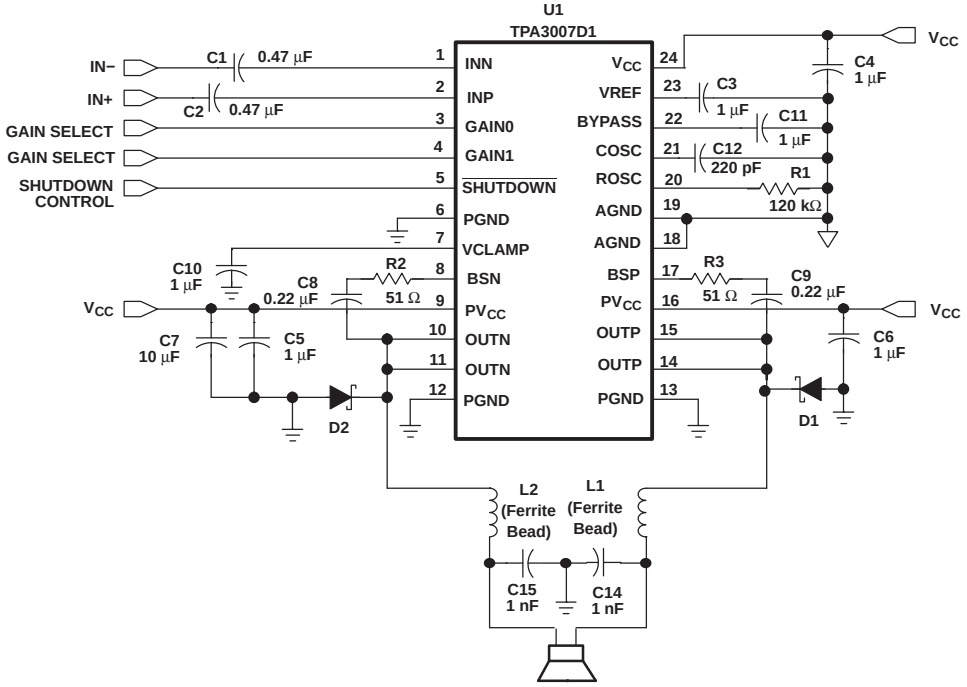
The TPA3007D1 is a 6.5-W mono bridge-tied load (BTL) class-D audio power amplifier with high efficiency, eliminating the need for heat sinks. The TPA3007D1 can drive 8-Ω speakers with only a ferrite bead filter required to reduce EMI.

The gain of the amplifier is controlled by two input terminals, GAIN1 and GAIN0. This allows the amplifier to be configured for a gain of 12, 18, 23.6, and 36 dB. The differential input stage provides high common mode rejection and improved power supply rejection.

The amplifier also includes "de-pop" circuitry to reduce the amount of pop at power-up and when cycling $\overline{\text{SHUTDOWN}}$.

The TPA3007D1 is available in the 24-pin TSSOP package (PW) and does not require an external heat sink.

Functional Schematic Diagram



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

AVAILABLE OPTIONS

T_A	PACKAGED DEVICES
	TSSOP (PW)(1)
-40°C to 85°C	TPA3007D1PW

(1) The PW package is available taped and reeled. To order a taped and reeled part, add the suffix R to the part number (e.g., TPA3007D1PWR).

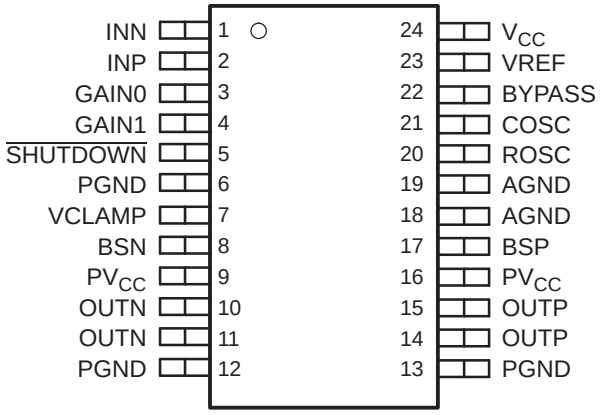
LEAD (PB)-FREE AND GREEN ORDERING INFORMATION

ORDERED DEVICE	STATUS (1)	ECO-STATUS(2)
TPA3007D1PWRG4	ACTIVE	Pb-Free and Green

(1) The marketing status values are defined as follows:
ACTIVE: This device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued production of the device.

(2) Eco-Status information – Additional details including specific material content can be accessed at www.ti.com/leadfree
N/A: Not yet available Lead (Pb)-Free; for estimated conversion dates, go to www.ti.com/leadfree.
Pb-Free: TI defines "Lead (Pb)-Free" or "Pb-Free" to mean RoHS compatible, including a lead concentration that does not exceed 0.1% of total product weight, and, if designed to be soldered, suitable for use in specified lead-free soldering processes.
Green: TI defines "Green" to mean Lead (Pb)-Free and in addition, uses package materials that do not contain halogens, including bromine (Br), or antimony (Sb) above 0.1% of total product weight.

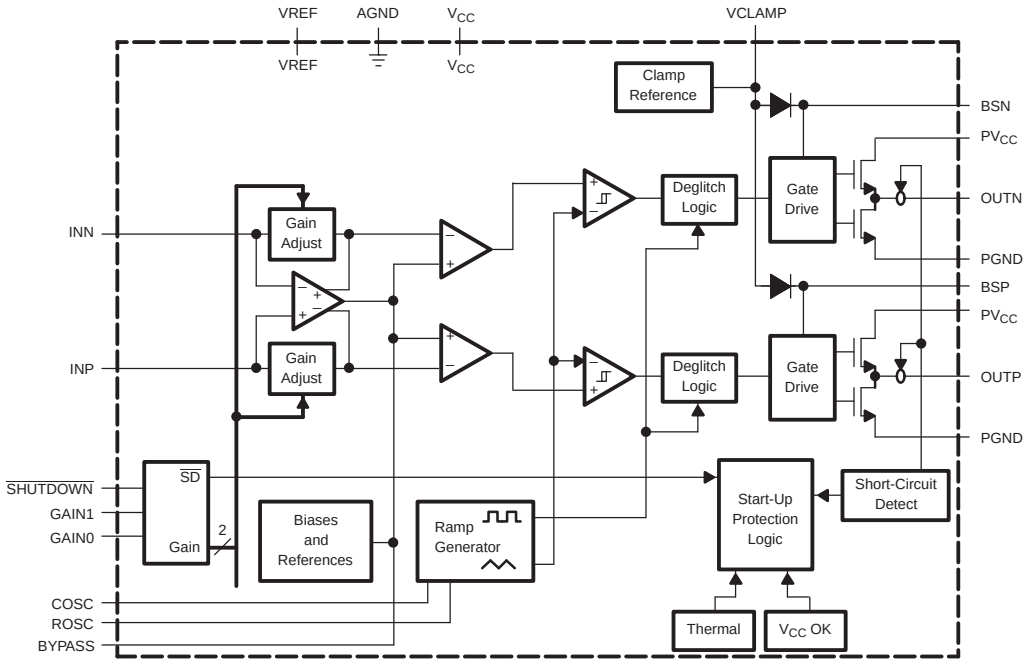
PW PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AGND	18, 19		Analog ground terminal
BSN	8	I	Bootstrap terminal for high-side gate drive of negative BTL output (connect a 0.22 µF capacitor with a 51 Ω resistor in series from OUTN to BSN)
BSP	17	I	Bootstrap terminal for high-side gate drive of positive BTL output (connect a 0.22 µF capacitor with a 51 Ω resistor in series from OUTP to BSP)
BYPASS	22	I	Connect 1 µF capacitor to ground for BYPASS voltage filtering
COSC	21	I	Connect a 220 pF capacitor to ground to set oscillation frequency
GAIN0	3	I	Bit 0 of gain control (see Table 2 for gain settings)
GAIN1	4	I	Bit 1 of gain control (see Table 2 for gain settings)
INN	1	I	Negative differential input
INP	2	I	Positive differential input
OUTN	10, 11	O	Negative BTL output, connect Schottky diode from PGND to OUTN for short-circuit protection
OUTP	14, 15	O	Positive BTL output, connect Schottky diode from PGND to OUTP for short-circuit protection
PGND	6, 12, 13		Power ground
PV_{CC}	9, 16	I	High-voltage power supply (for output stages)
ROSC	20	I	Connect 120 kΩ resistor to ground to set oscillation frequency
$\overline{SHUTDOWN}$	5	I	Shutdown terminal (active low), TTL compatible, 21-V compliant
V_{CC}	24	I	Analog high-voltage power supply
VCLAMP	7	O	Connect 1 µF capacitor to ground to provide reference voltage for H-bridge gates
VREF	23	O	5-V internal regulator for control circuitry (connect a 0.1 µF to 1 µF capacitor to ground)

Functional Block Diagram



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		UNIT
Supply voltage: V_{CC}, PV_{CC}		–0.3 V to 21 V
Load impedance, R_L		≥ 7 Ω
Input voltage	$\overline{SHUTDOWN}$	–0.3 V to V_{CC} + 0.3 V
	GAIN0, GAIN1	–0.3 V to 5.5 V
	INN, INP	–0.3 V to 7 V
Continuous total power dissipation		See Dissipation Rating Table
Operating free-air temperature range, T_A		–40°C to 85°C
Operating junction temperature range, T_J		–40°C to 150°C
Storage temperature range, T_{stg}		–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE

PACKAGE	T_A≤ 25°C	DERATING FACTOR	T_A = 70°C	T_A = 85°C
PW	1.43 W	11.45 mW/°C(1)	0.915 W	0.744 W

(1) Based on High-K board

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply voltage, V_{CC}, PV_{CC}	R_L≥ 7.0Ω(1)	8	18	V
Load impedance, R_L		7.0		Ω
High-level input voltage, V_{IH}	GAIN0, GAIN1, $\overline{SHUTDOWN}$	2		V
Low-level input voltage, V_{IL}	GAIN0, GAIN1, $\overline{SHUTDOWN}$		0.8	V
Operating free-air temperature, T_A		–40	85	°C
Operating junction temperature, T_J(2)			125	°C

(1) The TPA3007D1 must not be used with any speaker or load (including speaker with output filter) that could vary below 7.0Ω over the audio frequency band.

(2) Continuous operation above the recommended junction temperature may result in reduced reliability and/or lifetime of the device. The junction temperature is controlled by the thermal design of the application and should be carefully considered in high power dissipation applications. See the *thermal considerations* section on page 14 for recommendations on improving the thermal performance of your application.

ELECTRICAL CHARACTERISTICS

T_A= 25°C, PV_{CC} = V_{CC} = 12 V (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OS}\|$	Output offset voltage (measured differentially)	V_I = 0 V, A_V = 12 dB, 18, 23.6 dB			50	mV
		V_I = 0 V, A_V = 36 dB			100	
PSRR	Power supply rejection ratio	PV_{CC} = 11.5 V to 12.5 V		–73		dB
$\|I_{IH}\|$	High-level input current	PV_{CC} = 12 V, V_I = PV_{CC}			1	µA
$\|I_{IL}\|$	Low-level input current	PV_{CC} = 12 V, V_I = 0 V			1	µA
I_{CC}	Supply current	$\overline{SHUTDOWN}$ = 2.0 V, No load		8	15	mA
		$\overline{SHUTDOWN}$ = V_{CC}, V_{CC} = 18 V, P_O = 6.5 W, R_L = 8Ω		0.42		A
$I_{CC(SD)}$	Supply current, shutdown mode	$\overline{SHUTDOWN}$ = 0.8 V		1	2	µA
f_s	Switching frequency	R_{OSC} = 120 kΩ, C_{OSC} = 220 pF		250		kHz
$r_{ds(on)}$	Output transistor on resistance (total)	I_O = 1 A, T_J = 25°C			1.4	Ω
G	Gain	GAIN1 = 0.8 V, GAIN0 = 0.8 V	10.9	12	12.8	dB
		GAIN1 = 0.8 V, GAIN0 = 2 V	17.1	18	18.5	dB
		GAIN1 = 2 V, GAIN0 = 0.8 V	23	23.6	24.3	dB
		GAIN1 = 2 V, GAIN0 = 2 V	34.7	35.5	36.3	dB

OPERATING CHARACTERISTICS

PV_{CC} = V_{CC} = 12 V, Gain = 12 dB, T_A= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Continuous output power at 10% THD+N	f = 1 kHz, R_L = 8Ω		6.5		W
	Continuous output power at 1% THD+N	f = 1 kHz, R_L = 8Ω		5.0		
THD + N	Total harmonic distortion plus noise	P_O = 3.25 W, R_L = 8 Ω , f = 1 kHz		0.19 %		
B_{OM}	Maximum output power bandwidth	THD = 1%		20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz, $C_{(BYPASS)}$ = 1 µF		–70		dB
SNR	Signal-to-noise ratio	P_O = 3.25 W, R_L = 8 Ω		97		dB
V_n	Noise output voltage	$C_{(BYPASS)}$ = 1 µF, f = 20 Hz to 22 kHz, No weighting filter used		86		µV (rms)
				81		dBV
		$C_{(BYPASS)}$ = 1 µF, f = 20 Hz to 22 kHz, A-weighted filter		66		µV (rms)
				84		dBV
Z_I	Input impedance	See Table 2, page 14		> 23		kΩ

OPERATING CHARACTERISTICS

PV_{CC} = V_{CC} = 18 V, Gain = 12 dB, T_A= 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD + N	Total harmonic distortion plus noise	P_O = 3.25 W, R_L = 8 Ω, f = 1 kHz		0.16%		
B_{OM}	Maximum output power bandwidth	THD = 1%		20		kHz
k_{SVR}	Supply ripple rejection ratio	f = 1 kHz, C_{BYPASS} = 1 µF		–70		dB
SNR	Signal-to-noise ratio	P_O = 3.25 W, R_L = 8Ω		97		dB
V_n	Noise output voltage	$C_{(BYPASS)}$ = 1 µF, f = 20 Hz to 20 kHz, No weighting filter used		86		µV(rms)
				81		dBV
		$C_{(BYPASS)}$ = 1 µF, f = 20 Hz to 22 kHz, A-weighted filter		66		µV(rms)
				84		dBV
Z_I	Input impedance	See Table 2, page 14		>23		kΩ

TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

			FIGURE
	Efficiency	vs Output power	1
P_O	Output power	vs Supply Voltage	2
I_{CC}	Supply current	vs Supply voltage	3
$I_{CC(SD)}$	Shutdown current		4
THD+N	Total harmonic distortion + noise	vs Output power	5, 6
		vs Frequency	7, 8
k_{SVR}	Supply voltage rejection ratio	vs Frequency	9
	Gain and phase		10
CMRR	Common-mode rejection ratio		11
V_{IO}	Input offset voltage	vs Common-mode input voltage	12

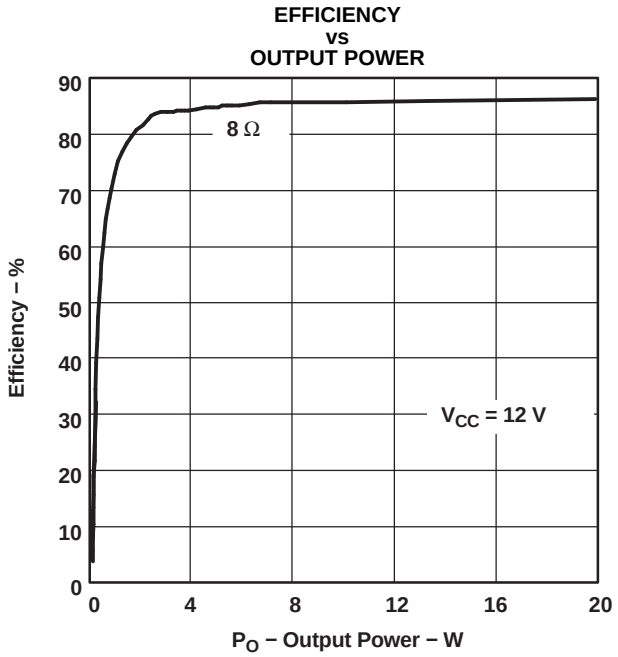


Figure 1.

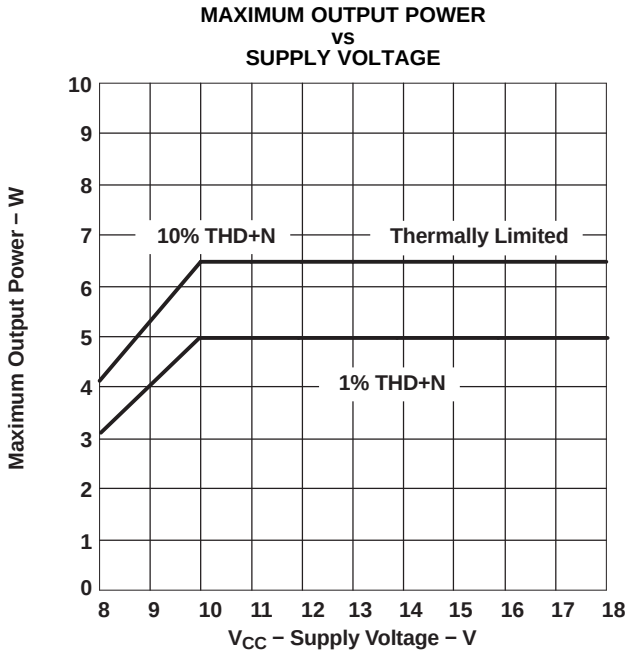


Figure 2.

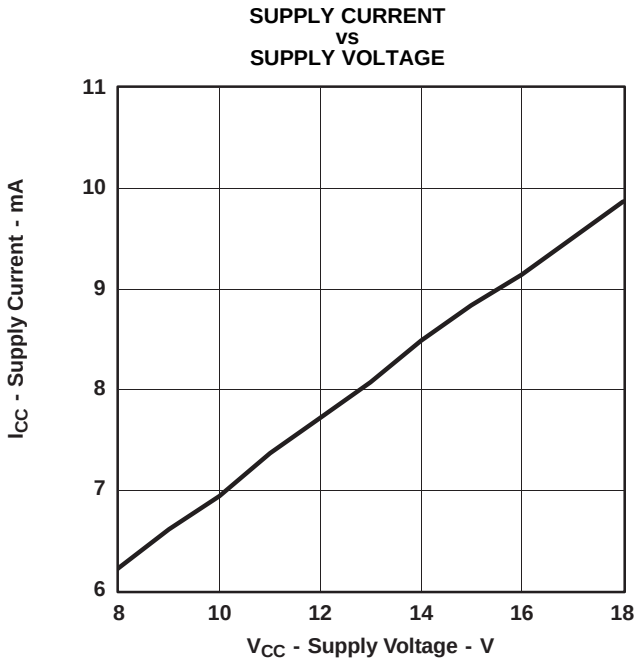


Figure 3.

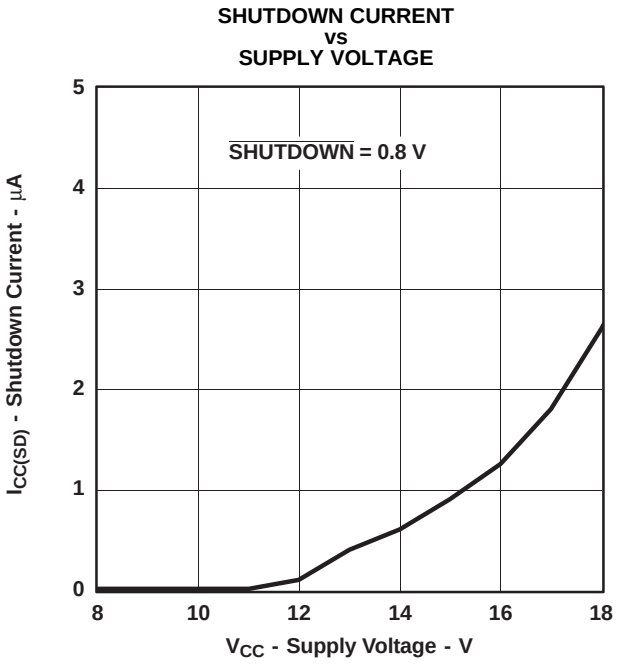


Figure 4.

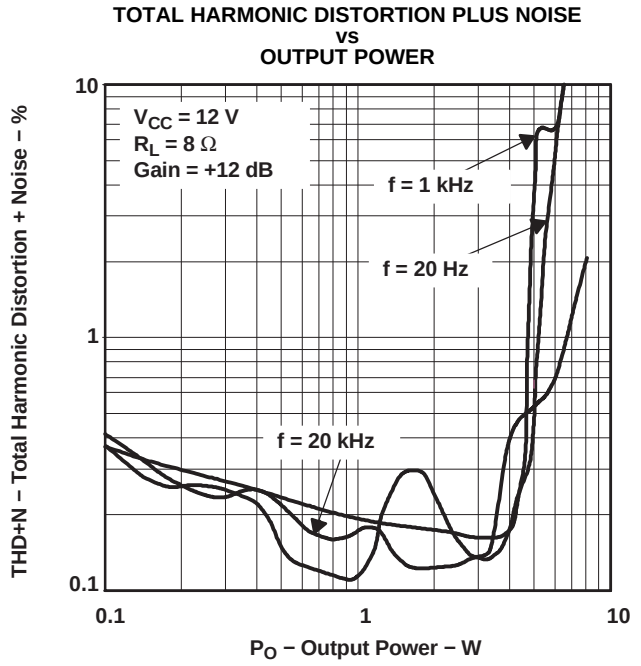


Figure 5.

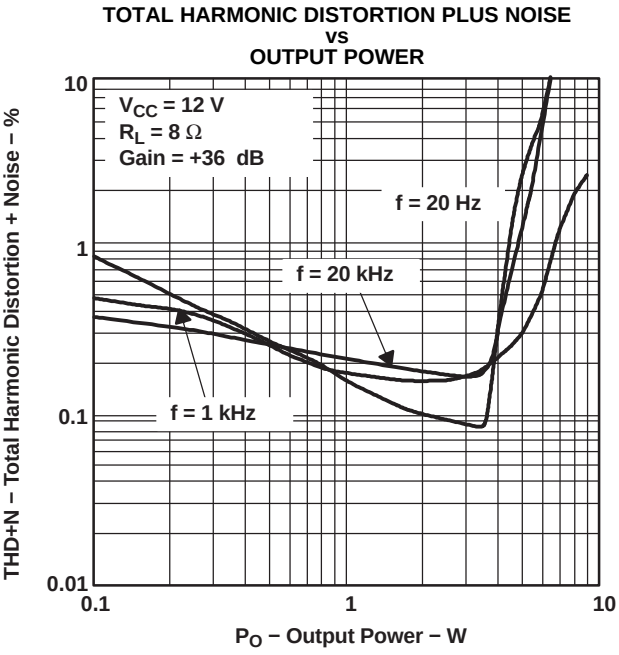


Figure 6.

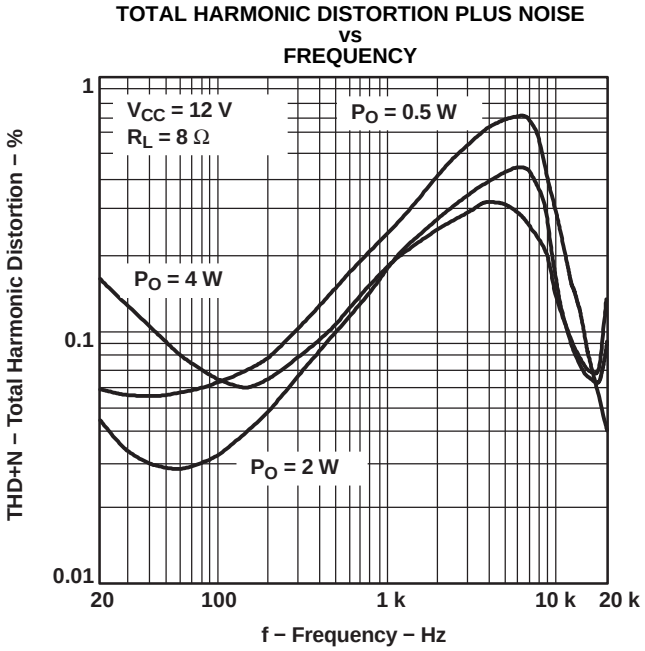


Figure 7.

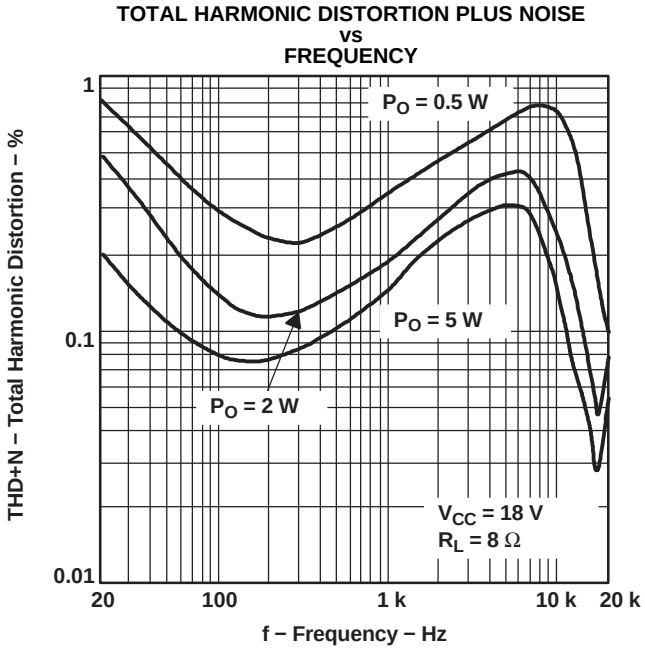


Figure 8.

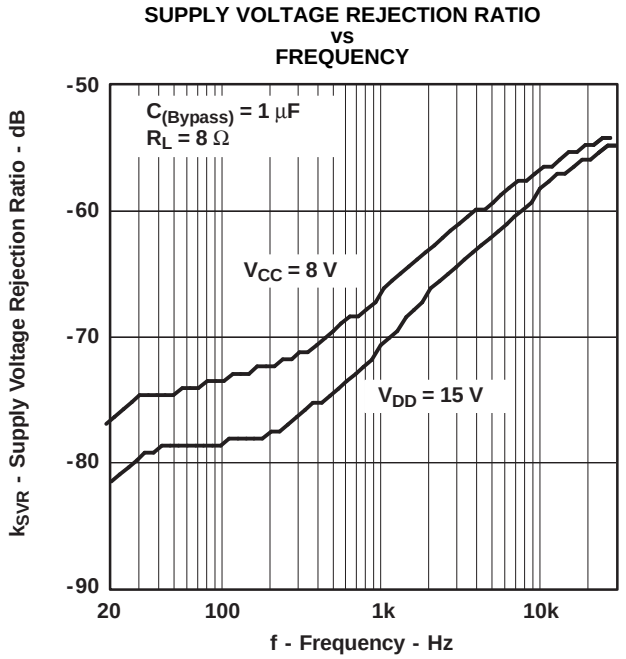


Figure 9.

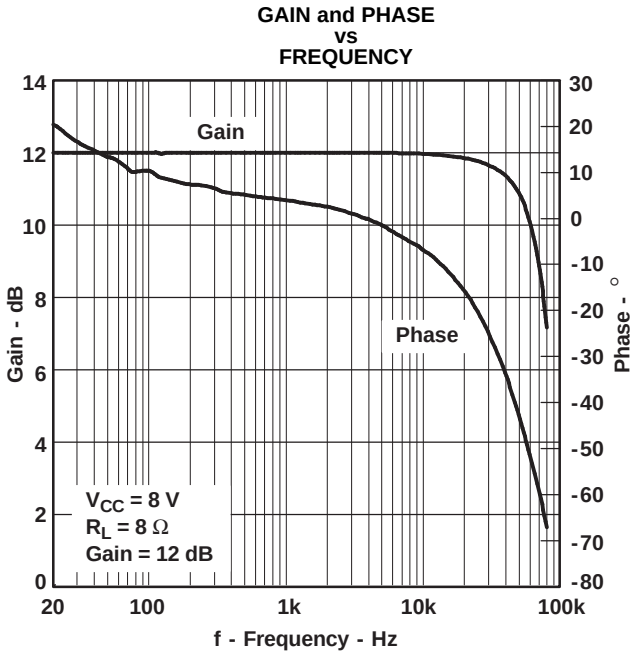


Figure 10.

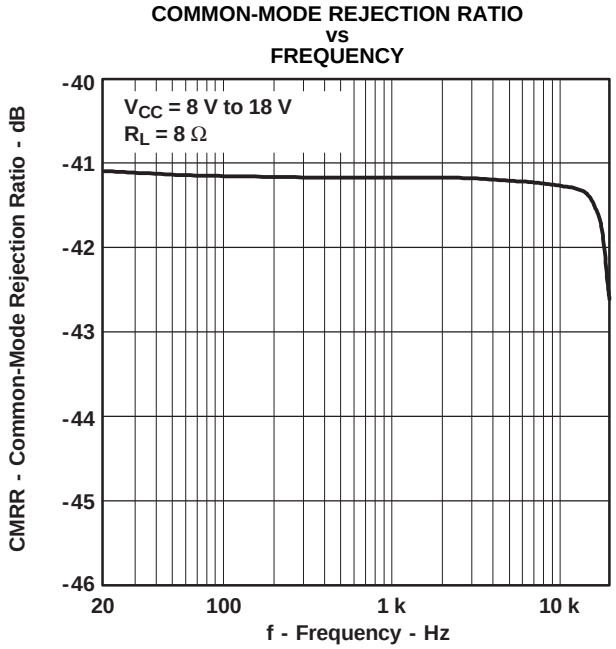


Figure 11.

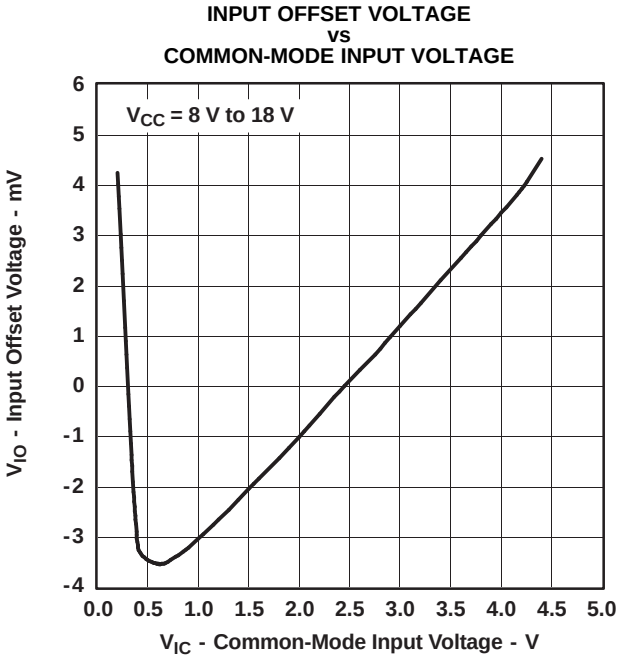


Figure 12.

APPLICATION INFORMATION

APPLICATION CIRCUIT

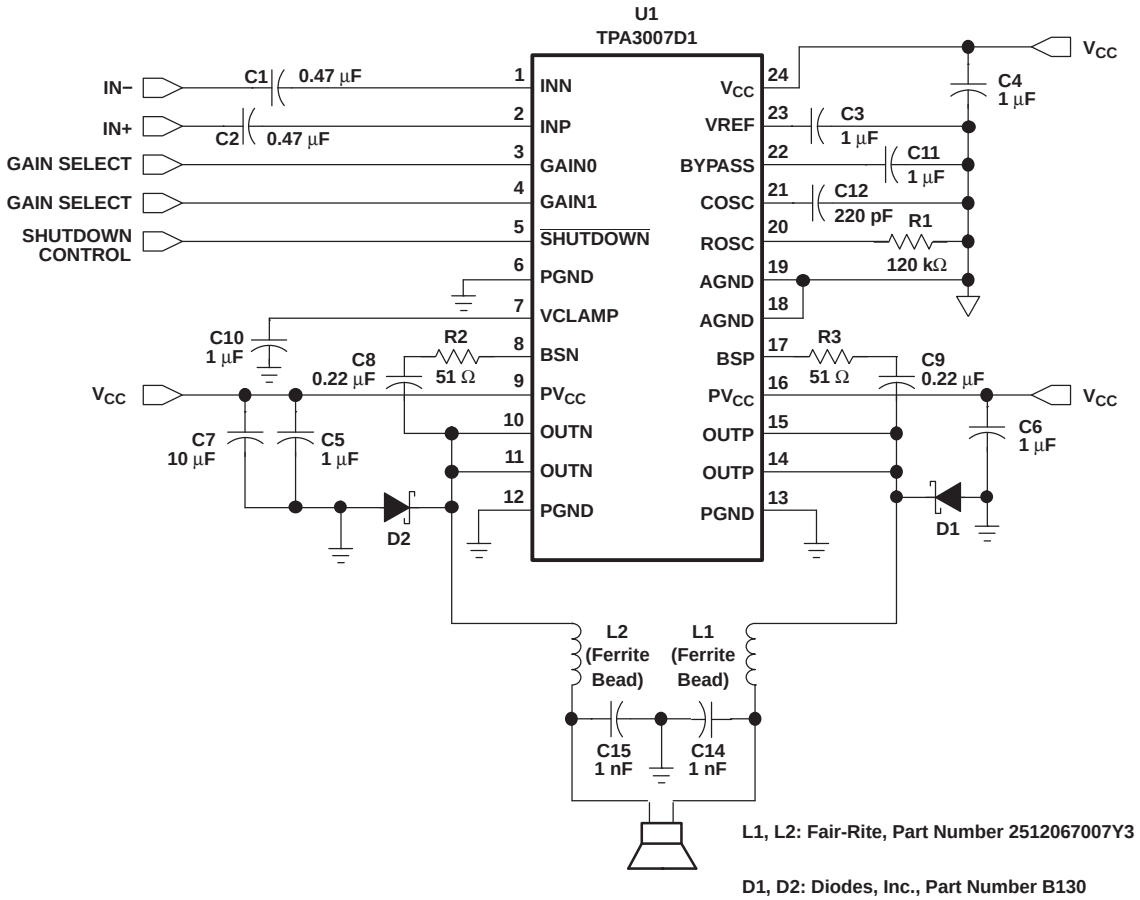


Figure 13. Typical Application Circuit

CLASS-D OPERATION

This section focuses on the class-D operation of the TPA3007D1.

TRADITIONAL CLASS-D MODULATION SCHEME

The traditional class-D modulation scheme, which is used in the TPA032D0x family, has a differential output where each output is 180 degrees out of phase and changes from ground to the supply voltage, V_{CC}. Therefore, the differential pre-filtered output varies between positive and negative V_{CC}, where filtered 50% duty cycle yields 0 V across the load. The traditional class-D modulation scheme with voltage and current waveforms is shown in Figure 14. Note that even at an average of 0 V across the load (50% duty cycle), the current to the load is high, causing high loss, thus causing a high supply current.

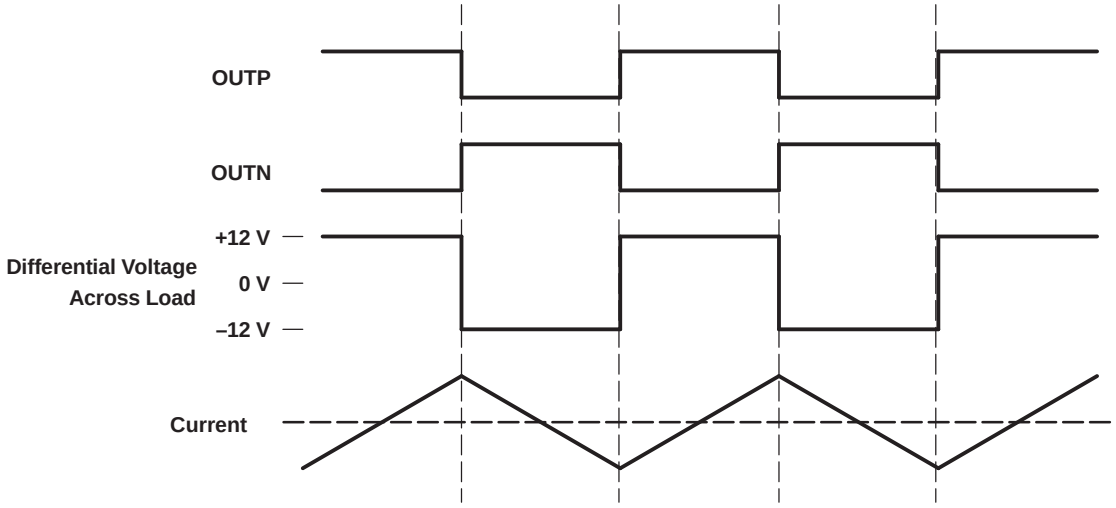


Figure 14. Traditional Class-D Modulation Scheme's Output Voltage and Current Waveforms Into an Inductive Load With No Input

TPA3007D1 MODULATION SCHEME

The TPA3007D1 uses a modulation scheme that still has each output switching from ground to V_{CC}. However, OUTP and OUTN are now in phase with each other with no input. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load is 0 V throughout most of the switching period, greatly reducing the switching current, which reduces any I^2R losses in the load. (See Figure 15).

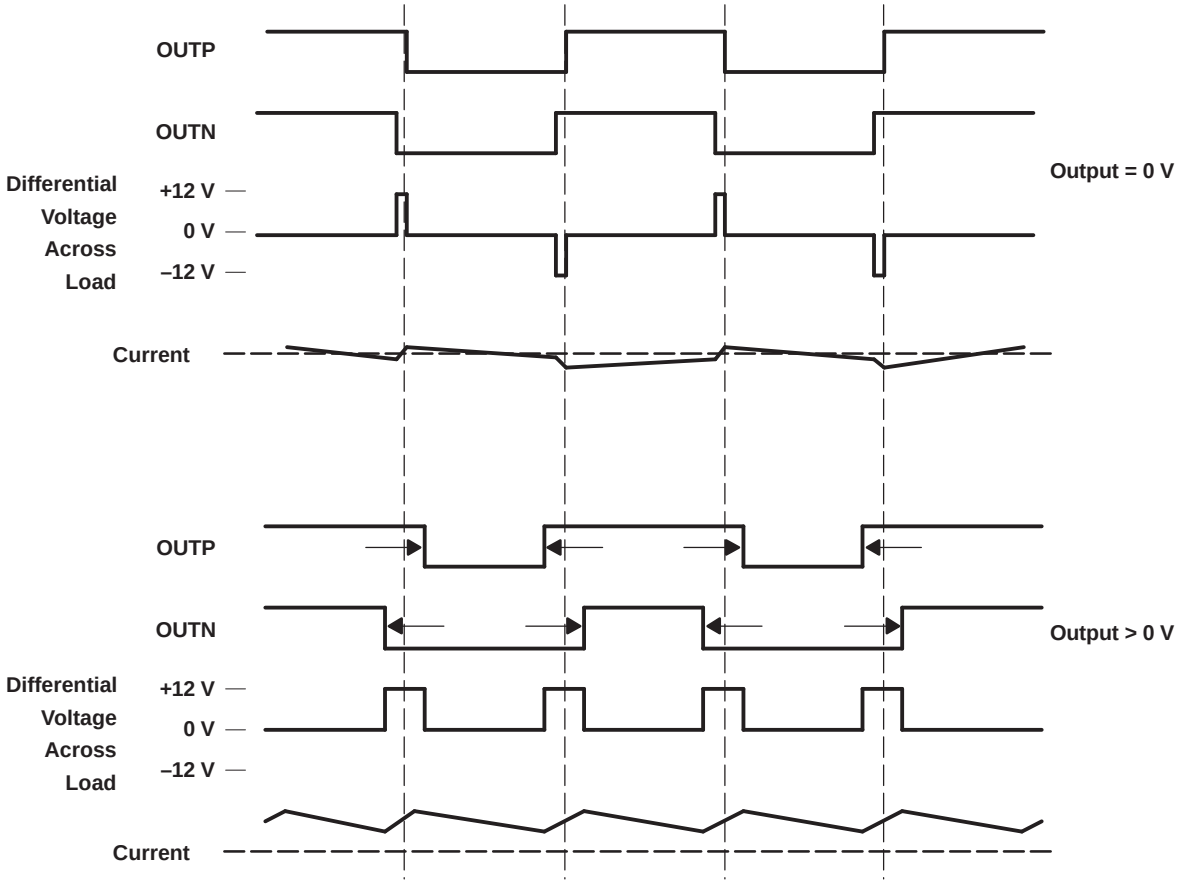


Figure 15. The TPA3007D1 Output Voltage and Current Waveforms Into an Inductive Load

DRIVING THE OUTPUT INTO CLIPPING

The output of the TPA3007D1 may be driven into clipping to attain a higher output power than is possible with no distortion. Clipping is typically quantified by a THD measurement of 10%. The amount of additional power into the load may be calculated with Equation 1.

$$P_{O(10\%\ THD)} = P_{O(1\%\ THD)} \times 1.25 \quad (1)$$

OUTPUT FILTER CONSIDERATIONS

A ferrite bead filter (shown in Figure 16) should be used in order to pass FCC and/or CE radiated emissions specifications and if a frequency sensitive circuit operating higher than 1 MHz is nearby. The ferrite filter reduces EMI around 1 MHz and higher (FCC and CE only test radiated emissions greater than 30 MHz). When selecting a ferrite bead, choose one with high impedance at high frequencies, but very low impedance at low frequencies.

Use an additional LC output filter if there are low frequency (<1 MHz) EMI sensitive circuits and/or there are long wires (greater than 11 inches) from the amplifier to the speaker, as shown in Figure 17.

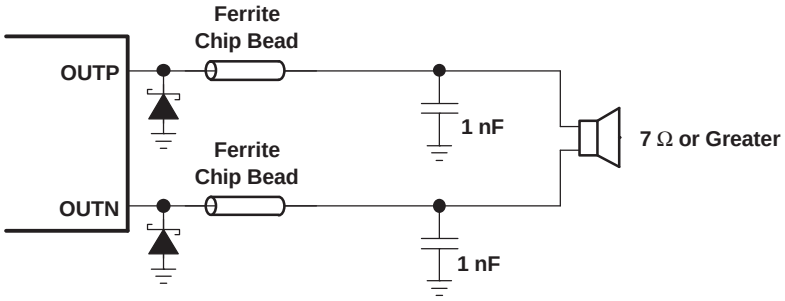


Figure 16. Typical Ferrite Chip Bead Filter (Chip bead example: Fair-Rite 2512067007Y3)

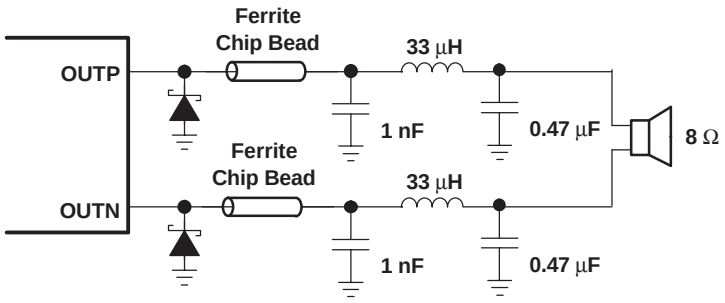


Figure 17. Typical LC Output Filter for 8-Ω Speaker, Cutoff Frequency of 41 kHz

SHORT-CIRCUIT PROTECTION

The TPA3007D1 has short circuit protection circuitry on the outputs that prevents damage to the device during output-to-output shorts, output-to-GND shorts, and output-to-V_{CC} shorts. When a short-circuit is detected on the outputs, the part immediately disables the output drive and enters into shutdown mode. This is a latched fault and must be reset by cycling the voltage on the $\overline{\text{SHUTDOWN}}$ pin to a logic low and back to the logic high state for normal operation. This clears the short-circuit flag and allow for normal operation if the short was removed. If the short was not removed, the protection circuitry again activates.

Two Schottky diodes are required to provide short-circuit protection. The diodes should be placed as close to the TPA3007D1 as possible, with the anodes connected to PGND and the cathodes connected to OUTP and OUTN as shown in the application circuit schematic. The diodes should have a forward voltage rating of 0.5 V at a minimum of 1A output current and a dc blocking voltage rating of at least 30 V. The diodes must also be rated to operate at a junction temperature of 150°C.

If short-circuit protection is not required, the Schottky diodes may be omitted.

THERMAL PROTECTION

Thermal protection on the TPA3007D1 prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal set point, the device enters into the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die is reduced by 15°C. The device begins normal operation at this point with no external system interaction.

THERMAL CONSIDERATION: OUTPUT POWER AND RECOMMENDED AMBIENT TEMPERATURE

To calculate the maximum ambient temperature, this equation can be used:

$$T_{A(max)} = T_J - \theta_{JA} P_{Dissipated}$$

where : $T_J = 125°C$

$$\theta_{JA} = \frac{1}{\text{derating factor}} = \frac{1}{0.01145} = 87.3°C/W \quad (2)$$

(The derating factor for the 24-pin PW package is given in the dissipation rating table.)

To estimate the power dissipation, this equation can be used:

$$P_{Dissipated} = P_{O(average)} \times \left(\left(\frac{1}{\text{Efficiency}} \right) - 1 \right)$$

$$\text{Efficiency} = \sim 85\% \text{ for an 8-}\Omega \text{ load} \quad (3)$$

Example: What is the maximum ambient temperature for an application that requires the TPA3007D1 to drive 3 W into an 8-Ω speaker?

$P_{Dissipated}$ = 3 W x ((1 / 0.85) - 1) = 0.529 W

T_{Amax} = 125°C - (87.3°C/W x 0.529 W) = 78.8°C

This calculation shows that the TPA3007D1 can drive 3 W into an 8-Ω speaker up to the absolute maximum ambient temperature rating of 78.8°C, which must never be exceeded.

GAIN SETTING VIA GAIN0 AND GAIN1 INPUTS

The gain of the TPA3007D1 is set by two input terminals, GAIN0 and GAIN1.

The gains listed in Table 2 are realized by changing the taps on the input resistors inside the amplifier. This causes the input impedance (Z_I) to be dependent on the gain setting. The actual gain settings are controlled by ratios of resistors, so the gain variation from part-to-part is small. However, the input impedance may shift by 30% due to shifts in the actual resistance of the input resistors.

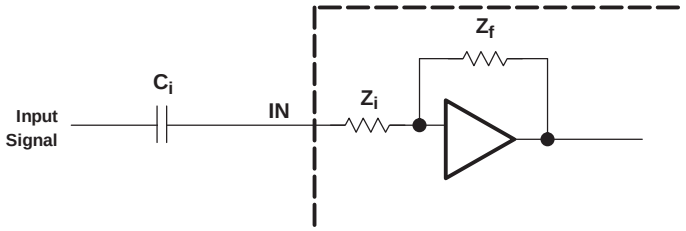
For design purposes, the input network (discussed in the next section) should be designed assuming an input impedance of 23 kΩ, which is the absolute minimum input impedance of the TPA3007D1. At the lower gain settings, the input impedance could increase as high as 313 kΩ.

Table 2. Gain Settings

GAIN1	GAIN0	AMPLIFIER GAIN (dB) TYP	INPUT IMPEDANCE (kΩ) TYP
0	0	12	241
0	1	18	168
1	0	23.6	104
1	1	36	33

INPUT RESISTANCE

Each gain setting is achieved by varying the input resistance of the amplifier, which can range from its smallest value to over six times that value. As a result, if a single capacitor is used in the input high-pass filter, the -3 B or cutoff frequency also changes by over six times.



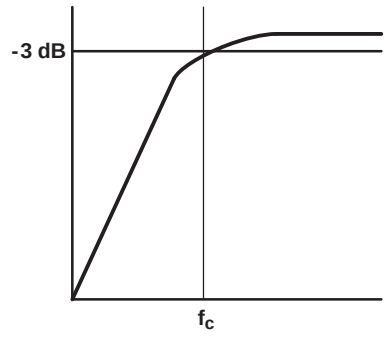
The -3 dB frequency can be calculated using Equation 4. Use Table 2 for Z_I values.

$$f = \frac{1}{2\pi Z_i C_i} \quad (4)$$

INPUT CAPACITOR, C_I

In the typical application an input capacitor ($_I$) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_I and the input impedance of the amplifier (Z_I) form a high-pass filter with the corner frequency determined in Equation 5.

$$f_c = \frac{1}{2\pi Z_i C_i} \quad (5)$$



The value of C_I is important, as it directly affects the bass (low frequency) performance of the circuit. Consider the example where Z_I is 241 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 5 is reconfigured as Equation 6.

$$C_i = \frac{1}{2\pi Z_i f_c} \quad (6)$$

In this example, C_I is 33 nF, so one would likely choose a value of 0.1 µF, as this value is commonly used. If the gain is known and will be constant, use Z_I from Table 2 to calculate C_I. A further consideration for this capacitor is the leakage path from the input source through the input network ($_I$) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 2.5 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application.

POWER SUPPLY DECOUPLING

The TPA3007D1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. The optimum decoupling is achieved by using two capacitors of different types that target different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1 µF placed as close as possible to the device V_{CC} lead works best. For filtering lower-frequency noise signals, a larger aluminum electrolytic capacitor of 10 µF or greater placed near the audio power amplifier is recommended.

BSN AND BSP CAPACITORS

The full H-bridge output stage uses only NMOS transistors. It therefore requires bootstrap capacitors for the high side of each output to turn on correctly. A 0.22-µF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22-µF capacitor must be connected from OUTP to BSP, and one 0.22-µF capacitor must be connected from OUTN to BSN. (See Figure 13.)

BSN AND BSP RESISTORS

To limit the current when charging the bootstrap capacitors, a resistor with a value of 51 Ω (±10% maximum) must be placed in series with each bootstrap capacitor. The current is limited to less than 500 µA.

VCLAMP CAPACITOR

To ensure that the maximum gate-to-source voltage for the NMOS output transistors is not exceeded, an internal regulator clamps the gate voltage. A 1-µF capacitor must be connected from VCLAMP (pin 7) to ground and must be rated for at least 25 V. The voltage at VCLAMP (pin 7) varies with V_{CC} and may not be used for powering any other circuitry.

MIDRAIL BYPASS CAPACITOR

The midrail bypass capacitor (C11 of Figure 13) is the most critical capacitor and serves several important functions. During start-up or recovery from shutdown mode, C_{BYPASS} determines the rate at which the amplifier starts up. The second function is to reduce noise produced by the power supply caused by coupling into the output drive signal. This noise is from the midrail generation circuit internal to the amplifier, which appears as degraded PSRR and THD+N.

Bypass capacitor (C11) values of 0.47 µF to 1 µF ceramic or tantalum low-ESR capacitors are recommended for the best THD noise and de-pop performance. The bypass capacitor **must** be a value greater than the input capacitors for optimum de-pop performance.

VREF DECOUPLING CAPACITOR

The VREF terminal (pin 23) is the output of an internally-generated 5-V supply, used for the oscillator and gain setting logic. It requires a 0.1-µF to 1-µF capacitor to ground to keep the regulator stable. The regulator may not be used to power any additional circuitry.

DIFFERENTIAL INPUT

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3007D1 EVM with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3007D1 with a single-ended source, ac ground the INN input through a capacitor and apply the audio signal to the INP input. In a single-ended input application, the INN input should be ac-grounded at the audio source instead of at the device input for best noise performance.

SWITCHING FREQUENCY

The switching frequency is determined using the values of the components connected to R_{OSC} (pin 20) and C_{OSC} (pin 21) and may be calculated with this equation:

$$f_S = \frac{6.6}{R_{OSC} C_{OSC}} \quad (7)$$

The frequency can be varied from 225 kHz to 275 kHz by adjusting the values chosen for R_{OSC} and C_{OSC}.

$\overline{\text{SHUTDOWN}}$ OPERATION

The TPA3007D1 employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of non-use for battery-power conservation. The $\overline{\text{SHUTDOWN}}$ input terminal should be held high during normal operation when the amplifier is in use. Pulling $\overline{\text{SHUTDOWN}}$ low causes the outputs to mute and the amplifier to enter a low-current state, $I_{CC(SD)}$ = 1 µA. $\overline{\text{SHUTDOWN}}$ should never be left unconnected, because amplifier operation would be unpredictable.

Ideally, the device should be held in shutdown when the system powers up and brought out of shutdown once any digital circuitry has settled. However, if $\overline{\text{SHUTDOWN}}$ is to be left unused, the terminal may be connected directly to V_{CC}.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

PRINTED-CIRCUIT BOARD (PCB) LAYOUT

Because the TPA3007D1 is a class-D amplifier that switches at a high frequency, the layout of the printed-circuit board (PCB) should be optimized according to the following guidelines for the best possible performance.

- Decoupling capacitors—As described in the Power Supply Decoupling section, the high-frequency 0.1-µF decoupling capacitors should be placed as close to the PVCC (pin 9 and pin 16) and VCC (pin 24) terminals as possible. The BYPASS (pin 22) capacitor, VREF (pin 23) capacitor, and VCLAMP (pin 7) capacitor should also be placed as close to the device as possible. The large (10 µF or greater) bulk power supply decoupling capacitor should be placed near the TPA3007D1.
- Grounding—The VCC (pin 24) decoupling capacitor, VREF (pin 23) capacitor, BYPASS (pin 22) capacitor, COSC (pin 21) capacitor, and ROSC (pin 20) resistor should each be grounded to analog ground (AGND, pin 18 and pin 19). The PVCC (pin 9 and pin 16) decoupling capacitors should each be grounded to power ground (PGND, pin 12 and pin 13). Analog ground and power ground should be connected as a central ground connection or star ground for the TPA3007D1.
- Output filter—The ferrite filter (Figure 16) should be placed as close to the output terminals (pins 10, 11, 14, and 15) as possible for the best EMI performance. The LC filter (Figure 17) should be placed close to the ferrite filter. The capacitors used in both the ferrite and LC filters should be grounded to power ground.

Related Documentation

For an example layout, refer to the *TPA3007D1 Evaluation Module (TPA3007D1EVM) 6.5W Mono Class-D Audio Power Amplifier* User's Guide, TI literature number SLOU164, available on the TI Internet site www.ti.com.

For further layout information, refer to *Layout Guidelines for TPA300x Series Parts* Application Report, TI literature number SLOA103, also available on the TI Internet site.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPA3007D1PW	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA3007D1
TPA3007D1PW.A	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA3007D1
TPA3007D1PWG4	Active	Production	TSSOP (PW) | 24	60 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA3007D1
TPA3007D1PWR	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA3007D1
TPA3007D1PWR.A	Active	Production	TSSOP (PW) | 24	2000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPA3007D1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

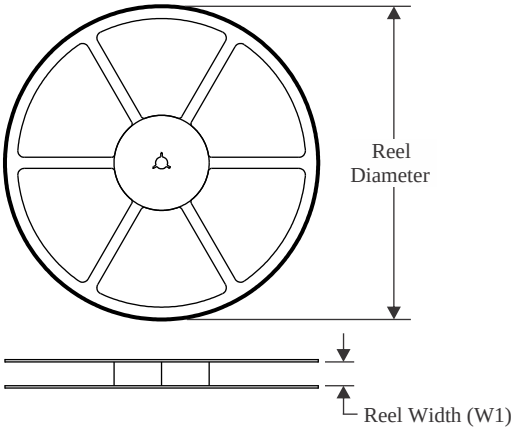
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

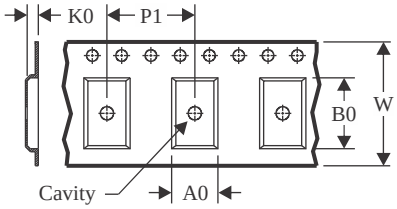
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

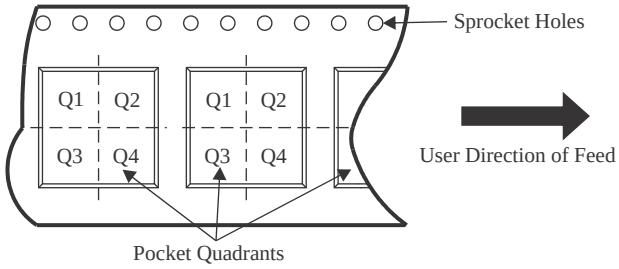


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

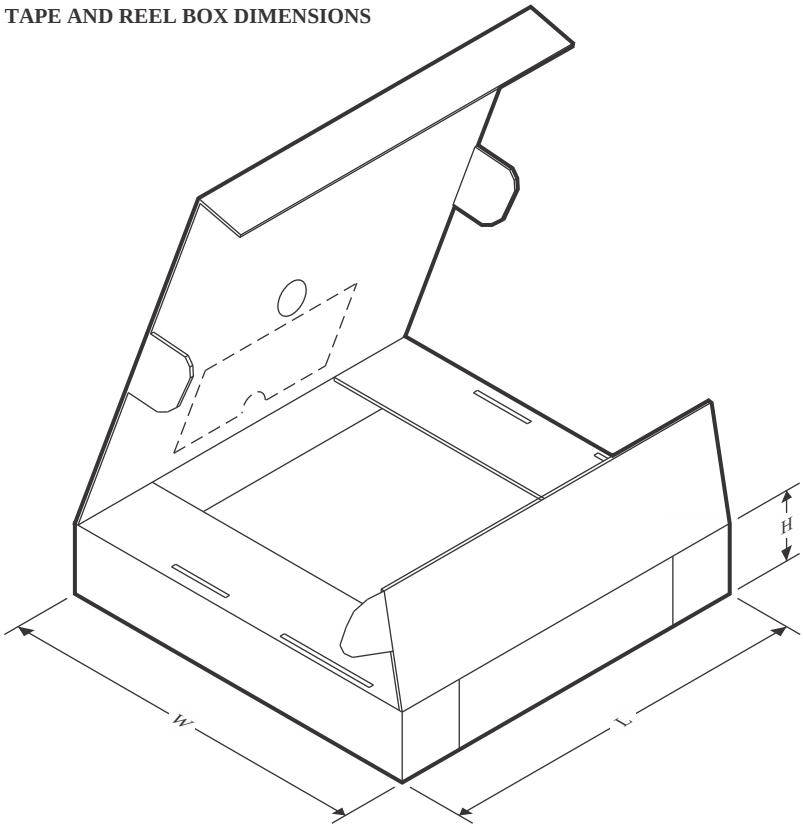
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3007D1PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

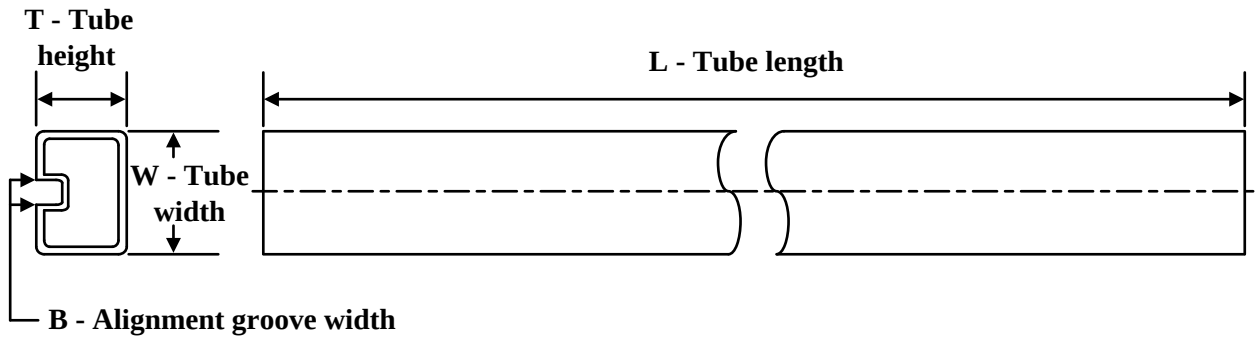
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3007D1PWR	TSSOP	PW	24	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

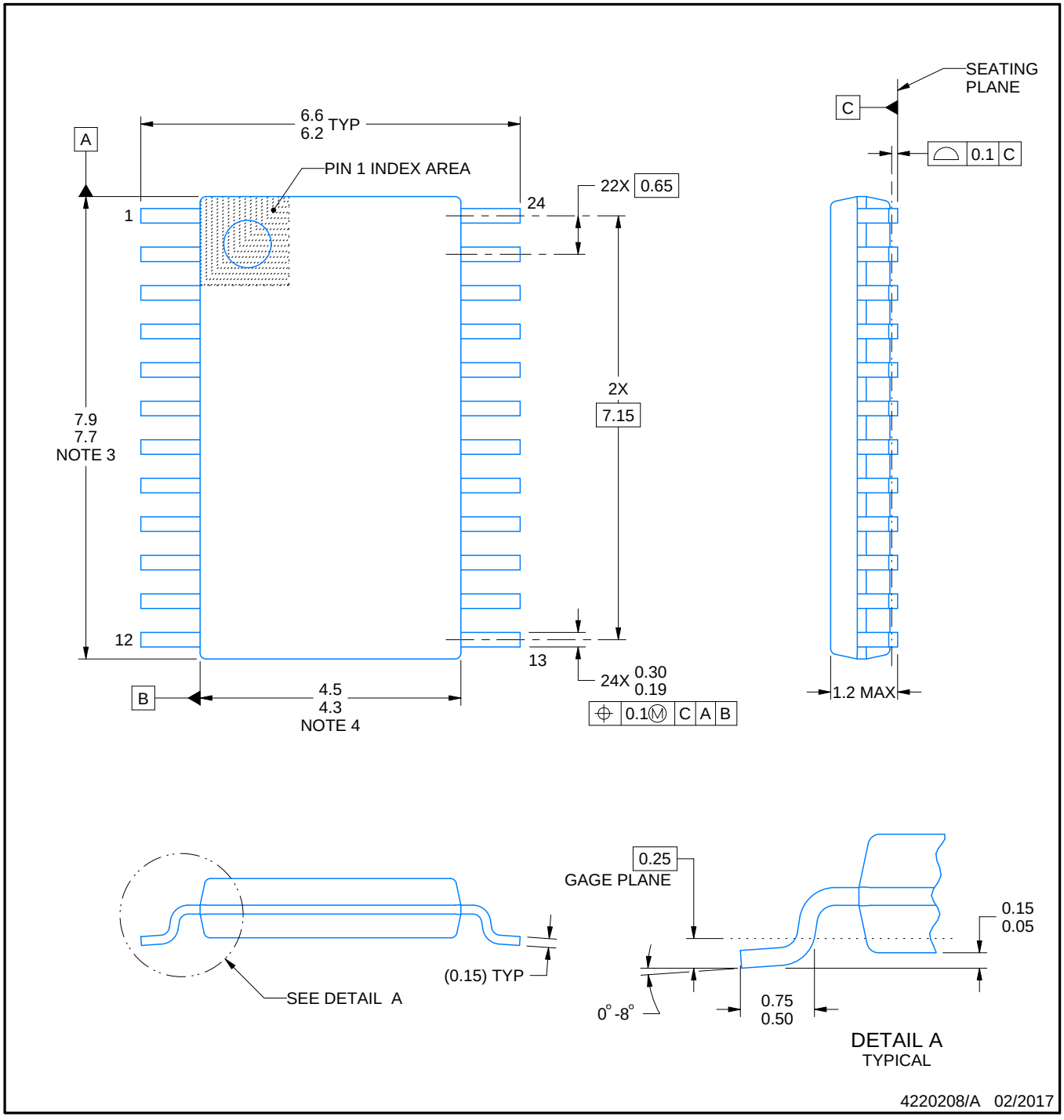
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA3007D1PW	PW	TSSOP	24	60	530	10.2	3600	3.5
TPA3007D1PW.A	PW	TSSOP	24	60	530	10.2	3600	3.5
TPA3007D1PWG4	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

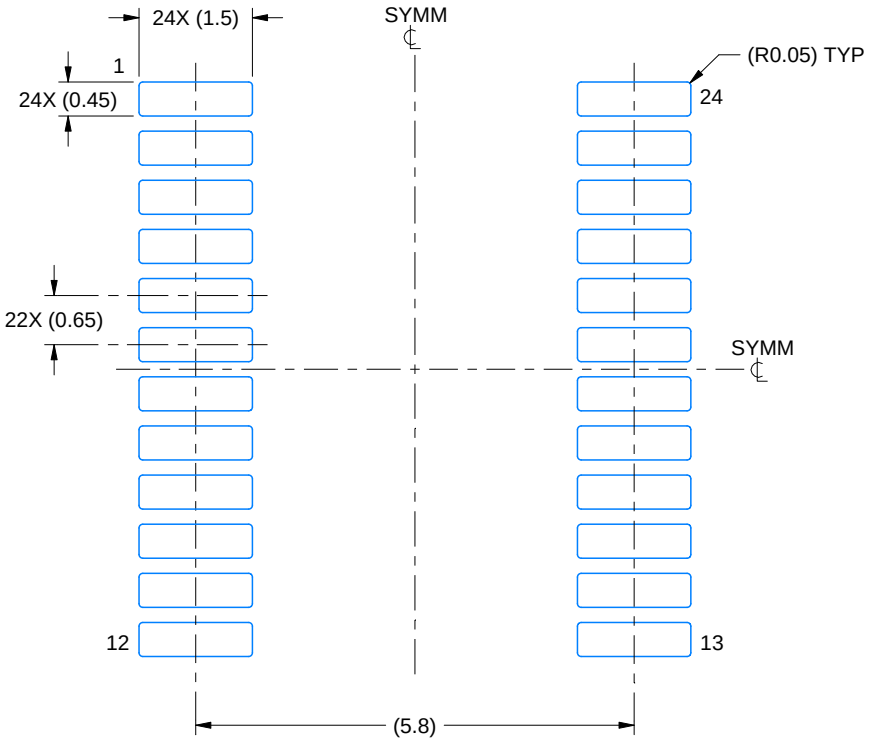
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

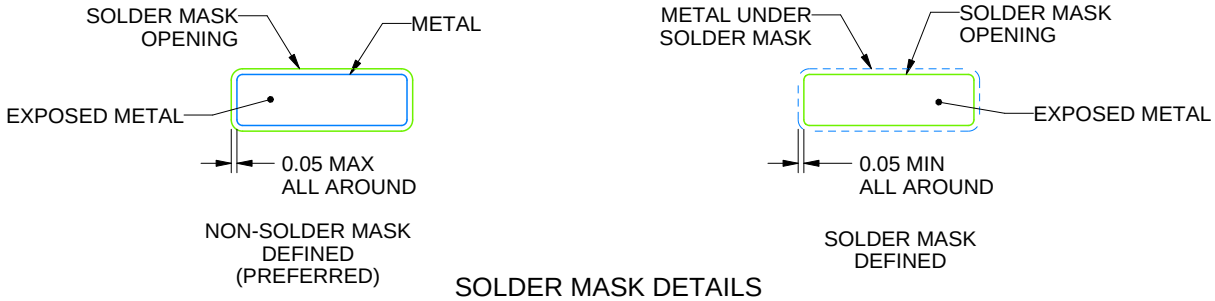


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

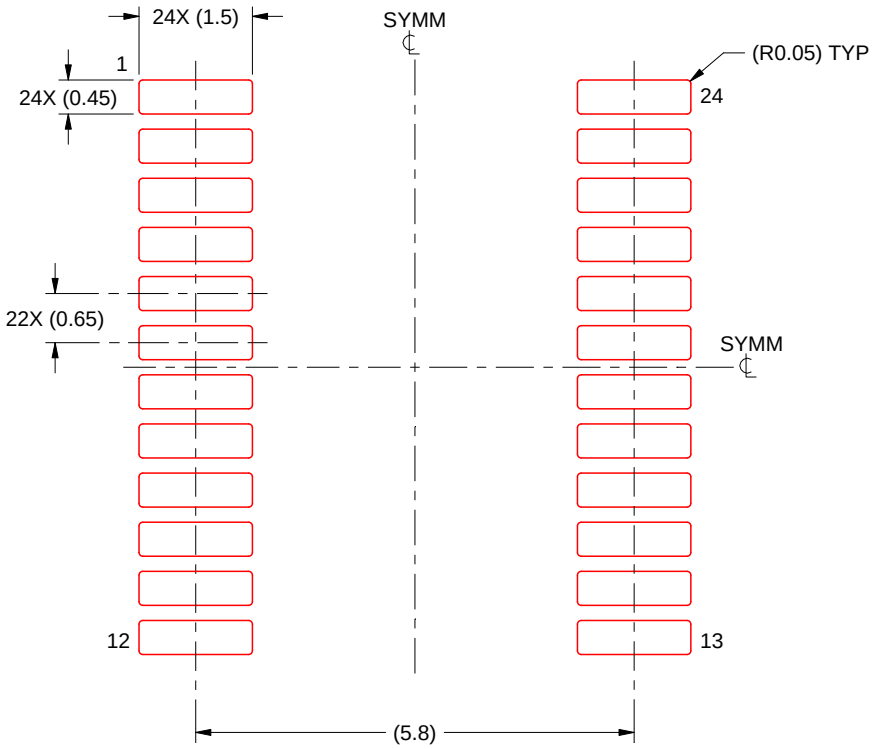


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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