

## 300mA, High PSRR, Tiny package, LDO Regulator

### Features

- Input Voltage Range: 1.7V to 5.5V
- 300mA Guaranteed Output Current
- Stable with 0.47µF Ceramic Output Capacitors
- Low Dropout Voltage 150mV@150mA (Vout=2.8V)
- Low Quiescent Current 36µA
- High PSRR 75dB@1kHz
- Auto Output Discharge
- High Output Accuracy ±2% Initial Accuracy
- Thermal Shutdown and Current Limit Protection
- Operating Temperature Range: -40 °C to +85 °C
- Packaging (Pb-free & Green):
  - 4-pin UDFN 1mm×1mm
  - 4-pin UDFN 0.8mm×0.8mm

### Description

PT7M8216 is a high accurate, low dropout voltage regulator with low noise, high ripple rejection and low current consumption.

PT7M8216 includes a reference voltage source, an error amplifier, a driver transistor, a current limit protection, a thermal protection and an internal phase compensator.

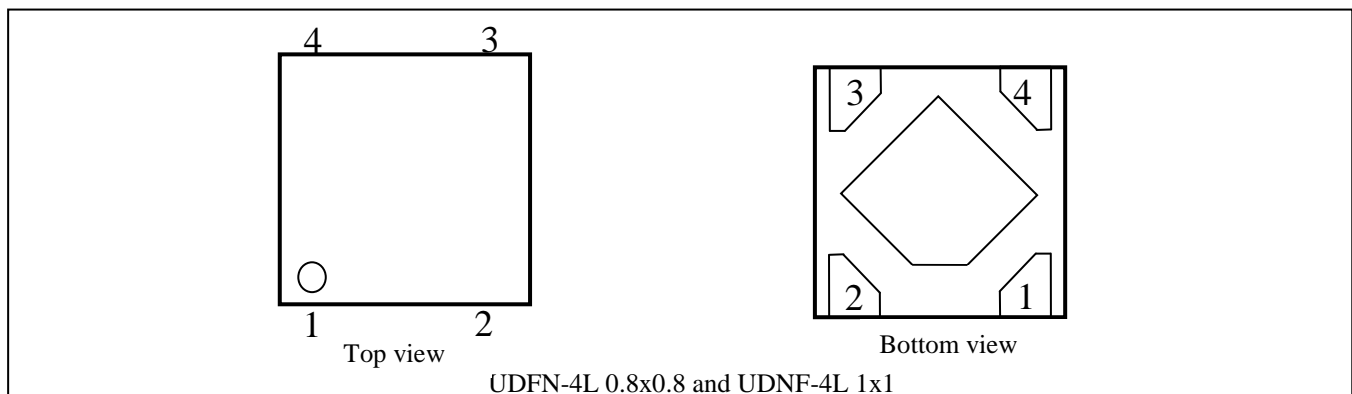
The output voltage for the regulator is set by factory trimming within a range of 0.9V to 3.3V in 100mV step includes 2.85V. PT7M8216 is stable with low ESR ceramic capacitors.

PT7M8216 is available in a 1mm×1mm UDFN-4L and 0.8mm×0.8mm UDFN-4L packages. It operates over a temperature range of -40 to +85 °C.

### Applications

- Cell Phones
- Mobile Phones (PDC, GSM, CDMA, IMT2000 etc.)
- Cordless Phones and Radio Communication
- Digital Still Cameras and Video Cameras
- PDA
- MP3 Players
- Portable Devices

### Pin Assignment



### Pin Description

Pin No	I/O	Pin Name	Description
4	I	VIN	Regulator Supply Input. Supply voltage can range from 1.7V to 5.5V. Bypass with a 0.47µF ceramic capacitor (X5R/X7R) to GND.
2	P	GND	Ground.
3	I	EN	ON/OFF Control of Regulator. High active.
5	-	NC	This pin is better to be connected to the GND, but leaving it open is also acceptable
1	O	VOUT	Output of Regulator. Bypass with a 0.47µF ceramic capacitor (X5R/X7R) to GND.

## Maximum Ratings

Storage Temperature.....	-55°C to +125°C
Ambient Temperature with Power Applied.....	-40°C to 85°C
Input Voltage .....	+6.0V
Output Voltage .....	-0.3 to V <sub>CC</sub> +0.3V
EN pin Voltage .....	+6.0V
DC Input/Output Current .....	700mA
Power Dissipation.....	UDFN-4L 1x1 400mW UDFN-4L 0.8x0.8 280mW

### Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V <sub>IN</sub>	Operating Voltage	-	1.7	-	5.5	V
V <sub>EN</sub>	Control Input Voltage	-	0	-	5.5	V
T <sub>A</sub>	Operating Temperature	-	-40	25	85	°C

## DC Electrical Characteristics

(T<sub>A</sub> = 25°C, V<sub>IN</sub> = V<sub>OUT</sub> + 1V for V<sub>OUT</sub> options greater than 1.5V. V<sub>IN</sub> = 2.5V for V<sub>OUT</sub> ≤ 1.5V, unless otherwise noted.)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output Voltage	V <sub>OUT(E)</sub> *	V <sub>IN</sub> =V <sub>OUT(S)</sub> * +1.0V, I <sub>OUT</sub> =30mA	V <sub>OUT(S)</sub> * 0.98	V <sub>OUT(S)</sub>	V <sub>OUT(S)</sub> * 1.02	V
Input Voltage	V <sub>IN</sub>	-	1.7	-	5.5	V
Maximum Output Current	I <sub>OUTMAX</sub>	V <sub>IN</sub> =V <sub>OUT(S)</sub> +1.0V	300	-	-	mA
Dropout Voltage	V <sub>DIF</sub> *	I <sub>OUT</sub> = 150mA	2.8V ≤ V <sub>OUT(S)</sub>	-	150	-
			V <sub>OUT(S)</sub> ≤ 2.7V	-	180	-
Supply Current	I <sub>SS</sub>	V <sub>IN</sub> = V <sub>OUT(S)</sub> + 1.0V, no load	-	36	65	µA
Standby Current	I <sub>STB</sub>	V <sub>IN</sub> = V <sub>OUT(S)</sub> + 1.0V, EN=GND	-	0.05	1	µA
Line Regulation	$\frac{\Delta V_{OUT}}{\Delta V_{IN}} * V_{OUT}$	V <sub>OUT(S)</sub> +1.0V ≤ V <sub>IN</sub> ≤ 5.5V, I <sub>OUT</sub> =30mA	-	0.02	0.2	%/V
Load Regulation	ΔV <sub>OUT2</sub>	V <sub>IN</sub> = V <sub>OUT(S)</sub> +1.0V, 1.0mA ≤ I <sub>OUT</sub> ≤ 150mA	-	10	30	mV
Output Voltage Temperature Characteristic	$\frac{\Delta V_{OUT}}{\Delta T_{opr}} * V_{OUT}$	I <sub>OUT</sub> =30mA, -40°C ≤ T <sub>opr</sub> ≤ 85°C	-	+/-100	-	ppm/°C
Ripple Rejection	PSRR	V <sub>IN</sub> =[V <sub>OUT(S)</sub> +1.0]V <sub>DC</sub> +0.2Vp-p AC I <sub>OUT</sub> =30mA, f=1kHz (In case that V <sub>out</sub> ≤ 2.0V, V <sub>IN</sub> =3.0V)	-	75	-	dB
Current Limit	I <sub>LIM</sub>	V <sub>OUT</sub> = V <sub>OUT(S)</sub> * 0.9	-	400	-	mA
Short Current Limit	I <sub>SC</sub>	V <sub>out</sub> =0V	-	40	-	mA
Thermal Shutdown	TSD	-	-	170	-	°C
Thermal Shutdown Hysteresis	ΔTSD	-	-	20	-	
EN "High" Voltage	V <sub>ENH</sub>	-	1.2	-	-	V
EN "Low" Voltage	V <sub>ENL</sub>	-	-	-	0.3	
EN "High" Current	I <sub>ENH</sub>	V <sub>IN</sub> =V <sub>OUT(S)</sub> +1.0V	-0.10	-	0.10	µA
EN "Low" Current	I <sub>ENL</sub>	V <sub>IN</sub> = V <sub>OUT(S)</sub> +1.0V, EN=OFF	-0.10	-	0.10	
Output Discharge Resistance	R <sub>dis</sub>	V <sub>IN</sub> = 4.0V, EN=OFF	-	50	-	Ω
Output Voltage Noise	V <sub>N</sub>	C <sub>OUT</sub> =0.47 µF, 10Hz to 100kHz	-	60	-	µVrms

### Note:

\*1: V<sub>OUT(S)</sub>=Specified output voltage

\*2: V<sub>OUT(E)</sub>=Effective output voltage

(I.e. the output voltage when "V<sub>OUT(S)</sub>+1.0V" is provided at the V<sub>IN</sub> pin while maintaining a certain I<sub>OUT</sub> value).

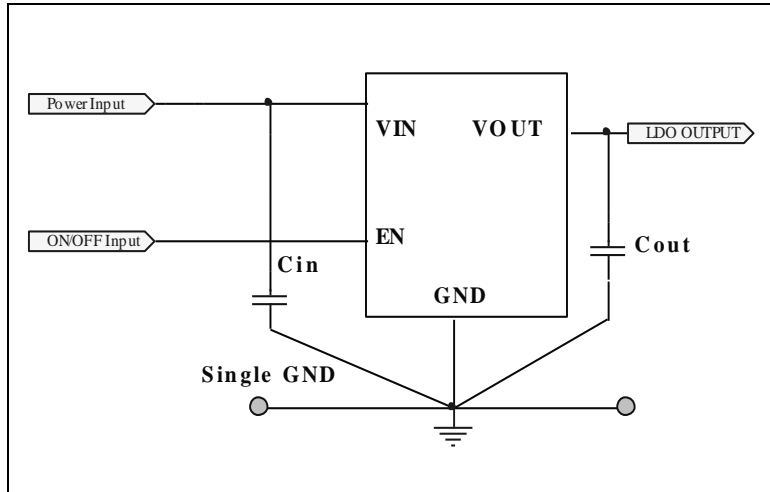
\*3: V<sub>DIF</sub>={ V<sub>IN1</sub>(\*) - V<sub>OUT1</sub>(\*) }

\*4: V<sub>OUT1</sub>=A voltage equal to 98% of the output voltage whenever an amply stabilized I<sub>OUT</sub> {V<sub>OUT(S)</sub>+1.0V} is input.

\*5: V<sub>IN1</sub>=The input voltage when V<sub>OUT1</sub> appears as input voltage is gradually decreased.

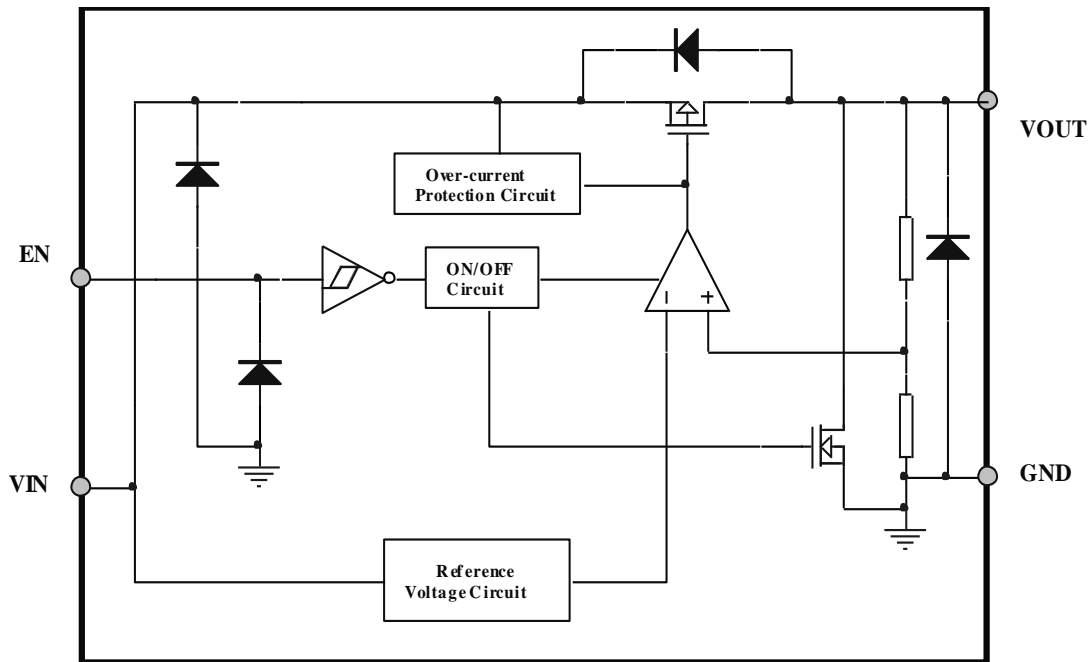
\*6: Unless otherwise stated, V<sub>IN</sub>=V<sub>OUT(S)</sub> +1.0V

**Application Circuits**



**Note:** Cin and Cout are 0.47 $\mu$ F low ESR ceramic capacitors

## Block Diagram



## Functional Description (Refer to Block Diagram)

### Output Voltage

The divided output voltage is compared with the internal reference voltage by the error amplifier with internal phase compensator. The output of the error amplifier then drives the P-channel MOSFET to maintain a stable and constant output voltage.

### Low ESR Capacitors

The internal phase compensator maintains the stable output voltage with low ESR ceramic input and output capacitors. 0.47 $\mu$ F low ESR (X5R/X7R) ceramic capacitor located as close as possible to the IC's pins is recommended.

### Current Limit and Thermal Shutdown Protections

Current limit protection is used to limit the output current when an overload condition occurs. As a result, the output voltage will drop. Thermal shutdown protection will turn off the output to reduce the power dissipation when the operation junction temperature exceeds 170 °C.

### EN Pin

The output of the regulator in PT7M8216 can be controlled with EN pin. The EN pin should be connected to a "VIN" or a "GND" voltage as a floating input applied to inverter input of the enable circuitry will increase the current consumption.

### NOTE ON USE

Please use this IC within the stated absolute maximum ratings.

Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current.

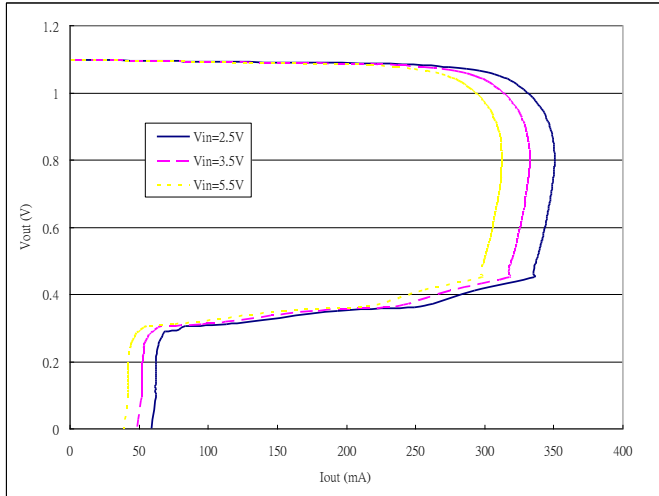
Please keep the resistance low between VIN and GND wiring in particular.

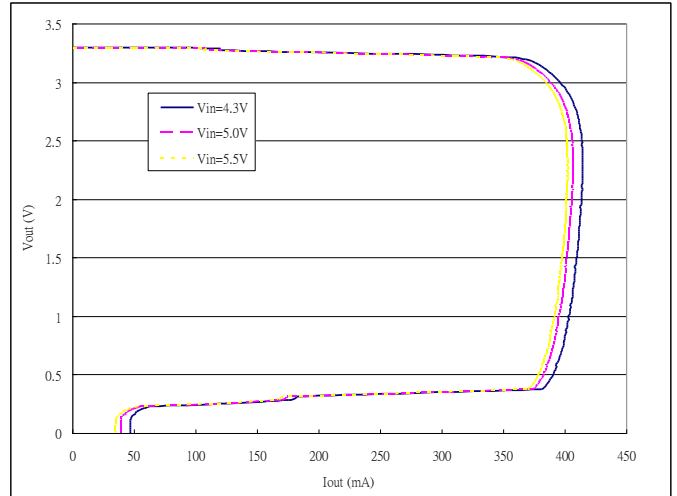
Please wire the input capacitor (C<sub>in</sub>) and the output capacitor (C<sub>out</sub>) as close to the IC as possible.

## Typical Performance Characteristics

### 1. Output Voltage vs. Output Current

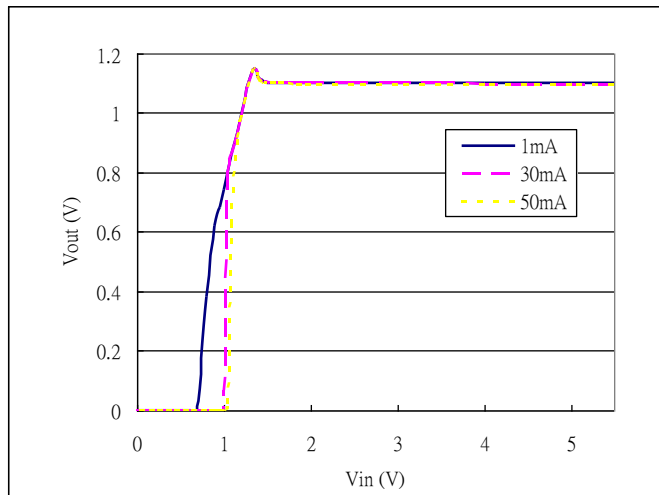
**PT7M8216B (1.1V)**

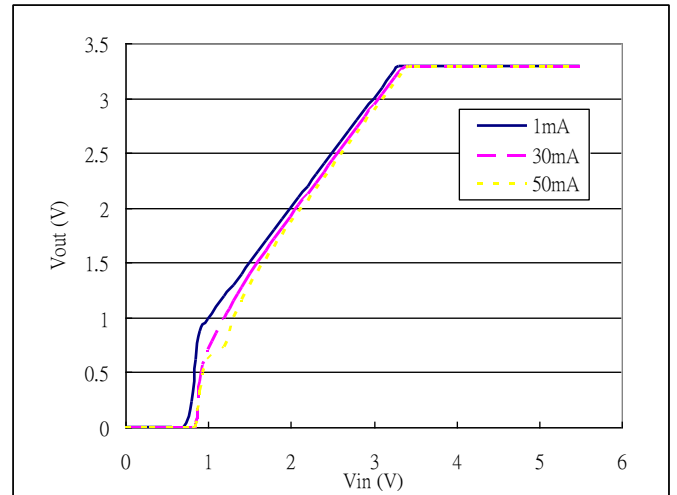
 Cin=0.47  $\mu$ F(Ceramics), Cout=0.47  $\mu$ F(Ceramics), T<sub>A</sub>=25  $^{\circ}$ C

**PT7M8216B (3.3V)**

 Cin=0.47  $\mu$ F(Ceramics), Cout=0.47  $\mu$ F(Ceramics), T<sub>A</sub>=25  $^{\circ}$ C


### 2. Output Voltage vs. Input Voltage

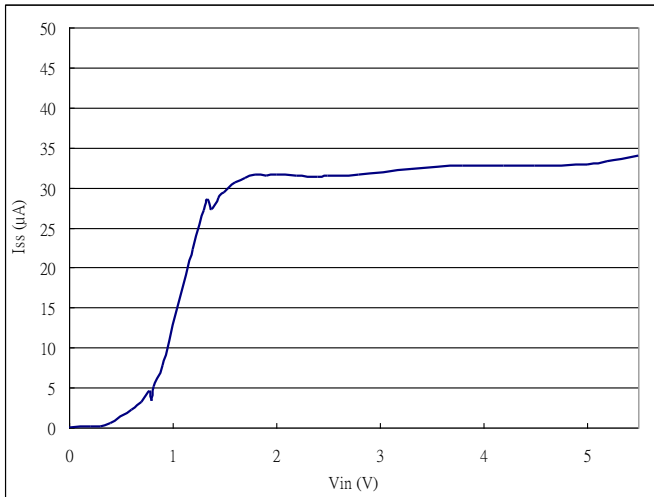
**PT7M8216 (1.1V)**

 Cin=0.47  $\mu$ F(Ceramics), Cout=0.47  $\mu$ F(Ceramics), T<sub>A</sub>=25  $^{\circ}$ C

**PT7M8216B (3.3V)**

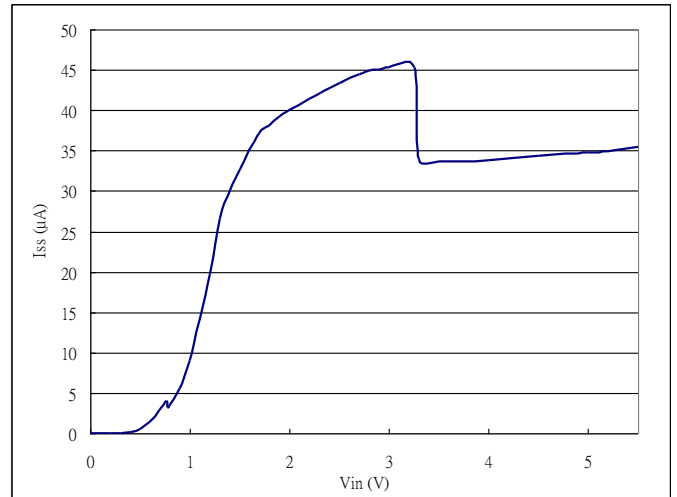
 Cin=0.47  $\mu$ F(Ceramics), Cout=0.47  $\mu$ F(Ceramics), T<sub>A</sub>=25  $^{\circ}$ C


**3. Supply Current vs. Input Voltage**
**PT7M8216 (1.1V)**

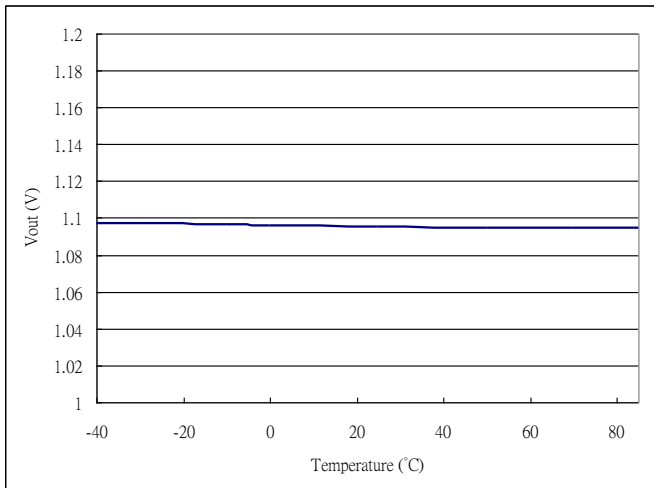
Vin=2.5V

 Cin=0.47  $\mu$ F(Ceramics), Cout=0.47  $\mu$ F(Ceramics), T<sub>A</sub>=25  $^{\circ}$ C

**PT7M8216B (3.3V)**

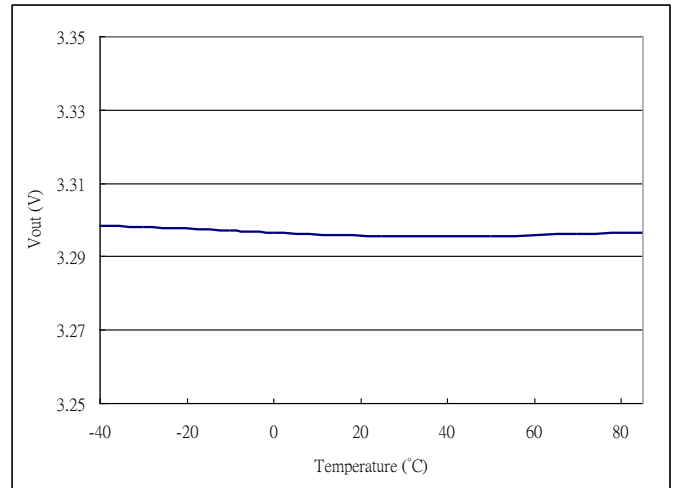
Vin=4.3V

 Cin=0.47  $\mu$ F(Ceramics), Cout=0.47  $\mu$ F(Ceramics), T<sub>A</sub>=25  $^{\circ}$ C

**4. Output Voltage vs. Ambient Temperature**
**PT7M8216 (1.1V)**

 Vin=2.5V, I<sub>OUT</sub>=30mA

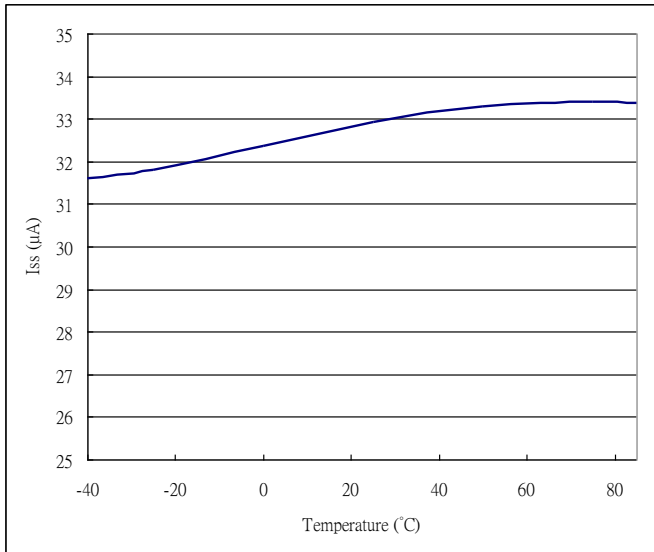
 Cin=0.47  $\mu$ F(Ceramics), Cout=0.47  $\mu$ F(Ceramics), T<sub>A</sub>=25  $^{\circ}$ C

**PT7M8216B (3.3V)**

 Vin=4.3V, I<sub>OUT</sub>=30mA

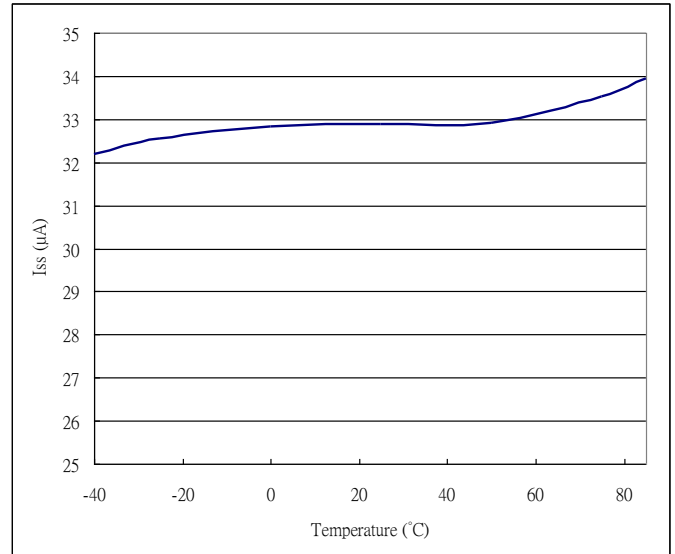
 Cin=0.47  $\mu$ F(Ceramics), Cout=0.47  $\mu$ F(Ceramics), T<sub>A</sub>=25  $^{\circ}$ C


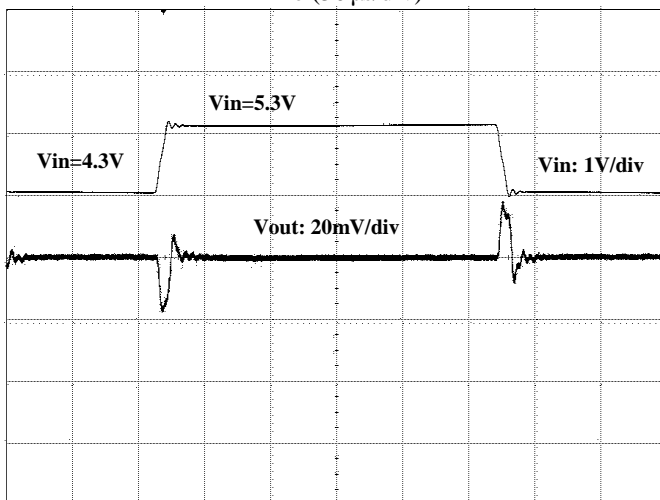
**5. Supply Current vs. Ambient Temperature**
**PT7M8216 (1.1V)**

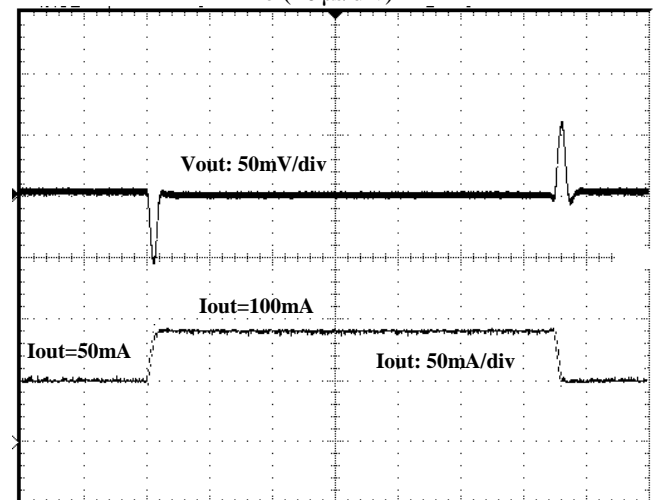
Vin=2.5V

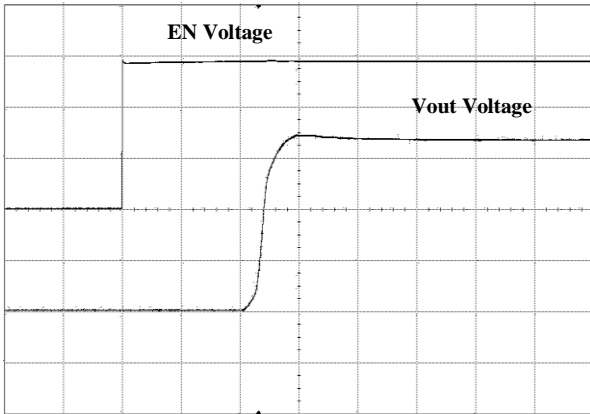
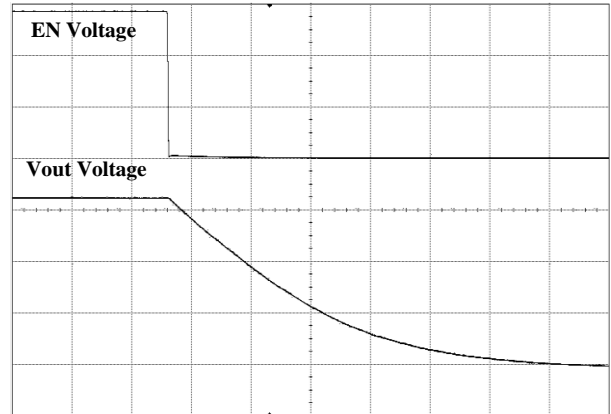
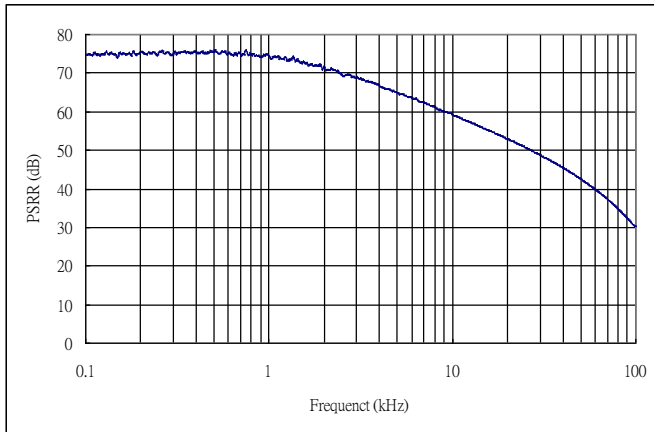
 Cin=0.47 μF(Ceramics), Cout=0.47 μF(Ceramics), T<sub>A</sub>=25 °C

**PT7M8216B (3.3V)**

Vin=4.3V

 Cin=0.47 μF(Ceramics), Cout=0.47 μF(Ceramics), T<sub>A</sub>=25 °C

**6. Line Transient Response**
**PT7M8216B (3.3V)**

 Cin=0.47 μF(Ceramics), Cout=0.47 μF(Ceramics), T<sub>A</sub>=25 °C  
 Time (50 μs/div)

**7. Load Transient Response**
**PT7M8216B (3.3V)**

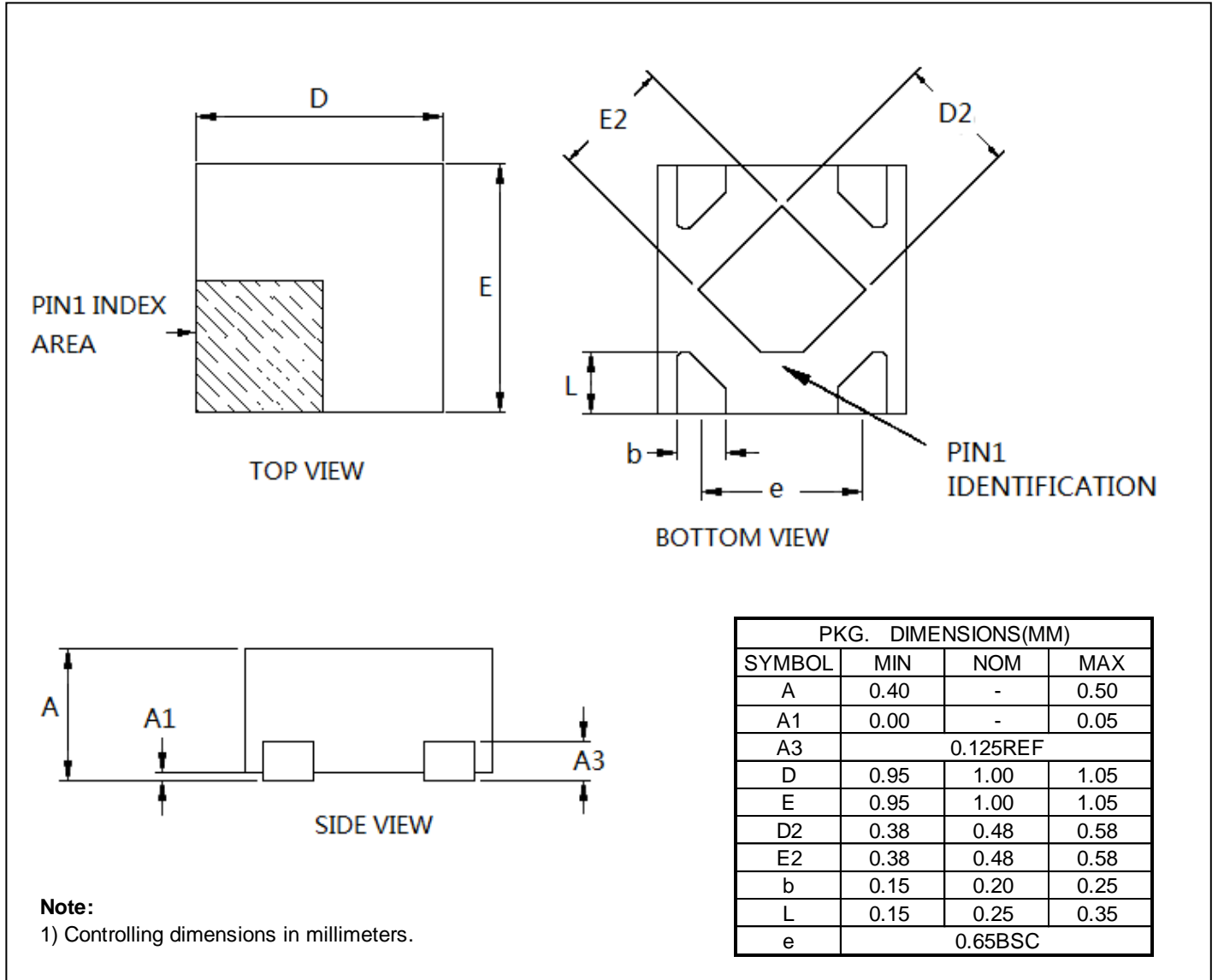
 Cin=0.47 μF(Ceramics), Cout=0.47 μF(Ceramics), T<sub>A</sub>=25 °C  
 Time (40 μs/div)


**8. Turn On Speed with EN pin**
**PT7M8216B (3.3V)**
 $C_{in}=0.47\ \mu\text{F}(\text{Ceramics})$ ,  $C_{out}=0.47\ \mu\text{F}(\text{Ceramics})$ ,  $T_A=25\ \text{°C}$   
 Time (20  $\mu\text{s}/\text{div}$ )

**9. Turn Off Speed with EN pin**
**PT7M8216B (3.3V)**
 $C_{in}=0.47\ \mu\text{F}(\text{Ceramics})$ ,  $C_{out}=0.47\ \mu\text{F}(\text{Ceramics})$ ,  $T_A=25\ \text{°C}$   
 Time (20  $\mu\text{s}/\text{div}$ )

**10. PSRR**
**PT7M8216 (0.9V)**
 $V_{in}=3.0\text{V DC}+0.2\text{Vp-pAC}$ 
 $C_{out}=0.47\ \mu\text{F}(\text{Ceramics})$ ,  $I_{out}=30\text{mA}$ 


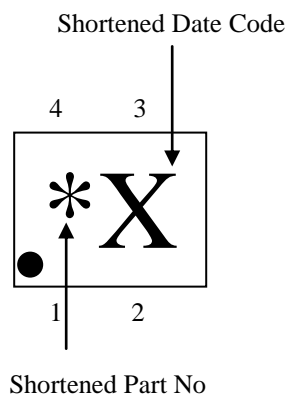


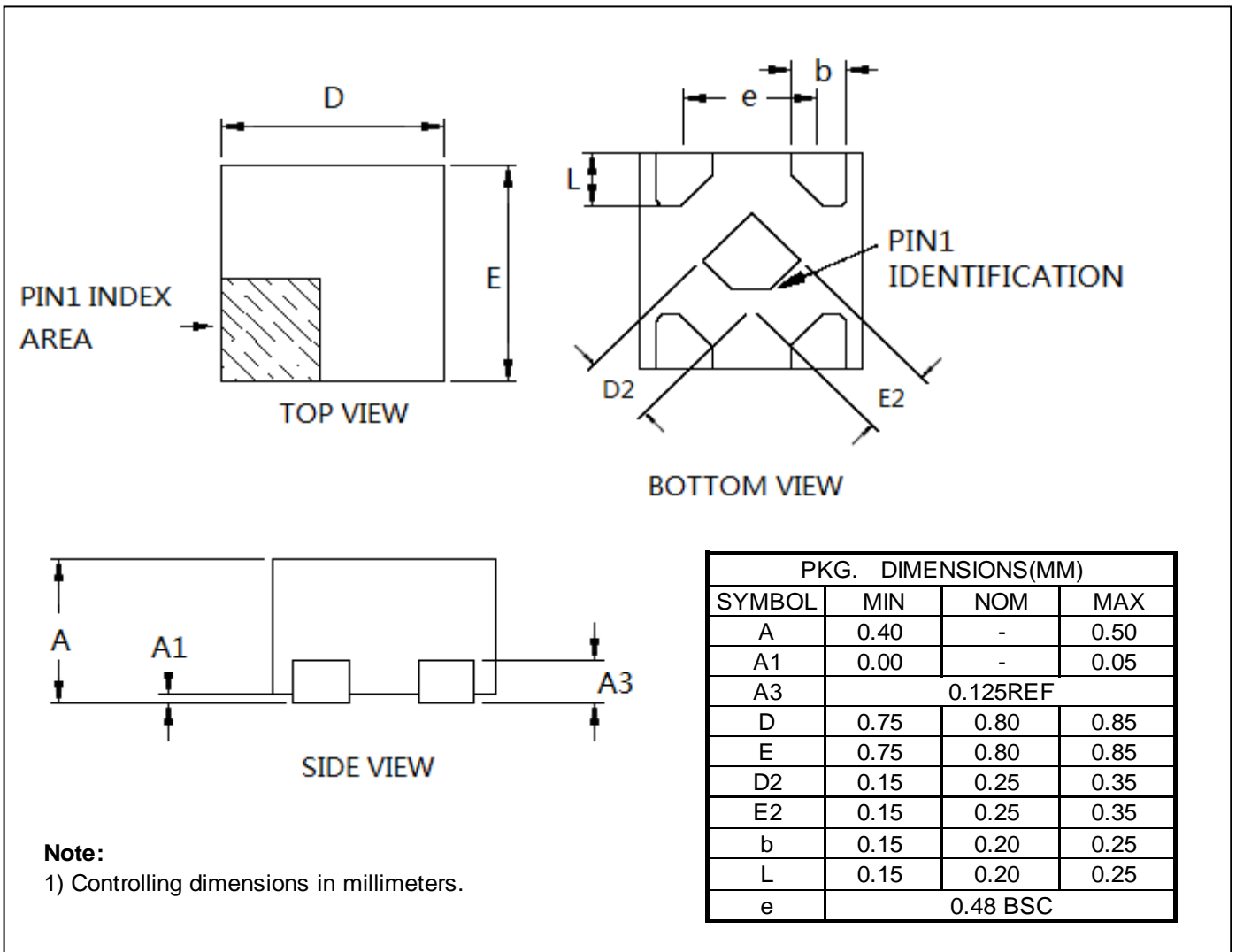
## Mechanical Information

4-pin UDFN 1mmx1mm

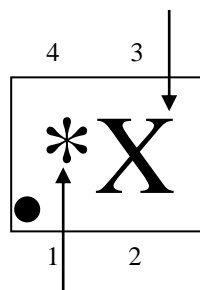


## Marking Description



**4-pin UDFN 0.8mmx0.8mm**

**Marking Description**

Shortened Date Code



Shortened Part No

## Ordering Information

Part Number	Package Code	Package	Top Marking
PT7M8216B①②XZE	XZ	Lead Free and Green UDFN-4 1mmx1mm (XZ)	See below Table1
PT7M8216B①②XYE	XY	Lead Free and Green UDFN-4 0.8mmx0.8mm (XY)	See below Table1

### Notes:

- E = Pb-free and Green
- Adding X Suffix= Tape/Reel
- “B” of PT7M8216B①② means high active for control pin “EN”
- “①②” refer to different output voltage. See below Table1
- Contact Pericom for availability.

### Table1 Sequential Number Description

Designator ①②	VOUT (V)	Top Marking	Designator ①②	VOUT (V)	Top Marking	Designator ①②	VOUT (V)	Top Marking
09	0.9	j	18	1.8	-	27	2.7	-
10	1.0	-	19	1.9	-	28	2.8	n
11	1.1	k	20	2.0	-	29	2.9	-
12	1.2	m	21	2.1	-	30	3.0	p
13	1.3	-	22	2.2	-	31	3.1	-
14	1.4	-	23	2.3	-	32	3.2	-
15	1.5	-	24	2.4	-	33	3.3	q
16	1.6	-	25	2.5	-	2A	2.85	-
17	1.7	-	26	2.6	-			-

Pericom Semiconductor Corporation • 1-800-435-2336 • [www.pericom.com](http://www.pericom.com)

Pericom reserves the right to make changes to its products or specifications at any time, without notice, in order to improve design or performance and to supply the best possible product. Pericom does not assume any responsibility for use of any circuitry described other than the circuitry embodied in Pericom product. The company makes no representations that circuitry described herein is free from patent infringement or other rights, of Pericom.