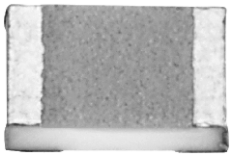
High Precision Wraparound - Wide Ohmic Value Range Thin Film Chip Resistors



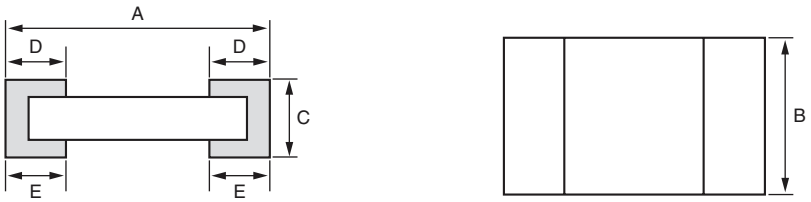
For low noise and precision applications, superior stability, low temperature coefficient of resistance, and low voltage coefficient, Vishay Sfernice's proven precision thin film wraparound resistors exceed requirements of MIL-PRF-55342G characteristics Y ± 10 ppm/°C (- 55 °C; + 155 °C) down to ± 5 ppm/°C (- 55 °C; + 155 °C).

FEATURES

- Load life stability at ± 70 °C for 2000 h: 0.1 % under Pn/0.05 % under Pd
- Low temperature coefficient down to **5 ppm/°C** (- 55 °C; + 155 °C)
- Very low noise < 35 dB and voltage coefficient < 0.01 ppm/V
- Wide resistance range: 10 Ω to 50 MΩ depending on size
- Tolerances to **± 0.01 %**
- In lot tracking ≤ 5 ppm/°C
- Termination: thin film technology
- Gold plated or pre-tinned terminations over nickel barrier
- Short circuits (jumpers) r < 50 mR, I < 2 A
- SMD wraparound terminations
- Withstand moisture resistance test of AEC-Q200
- Compliant to RoHS directive 2002/95/EC

Pb-free Available
RoHS* COMPLIANT
GREEN (5-2008)** Available

DIMENSIONS in millimeters (inches)

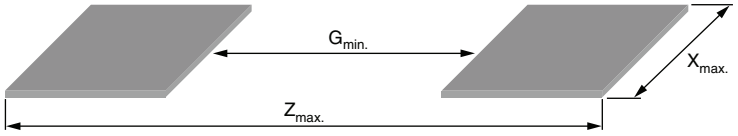


CASE SIZE	A	B	C	D/E	
	MAX. TOL. + 0.152 (+ 0.006) MIN. TOL. - 0.152 (- 0.006)	MAX. TOL. + 0.127 (+ 0.005) MIN. TOL. - 0.127 (- 0.005)			
	NOMINAL	NOMINAL		NOMINAL	TOLERANCE
0302	0.75 (0.029)	0.60 (0.024)	0.5 (0.02) ± 0.127 (0.005)	0.15 (0.006)	0.08 (0.003)
0402	1.00 (0.039)	0.60 (0.024)		0.25 (0.010)	0.1 (0.004)
0505	1.27 (0.005)	1.27 (0.050)		0.38 (0.015)	0.13 (0.005)
0603	1.52 (0.060)	0.85 (0.033)			
0705/0805	1.91 (0.075)	1.27 (0.050)			
1005	2.54 (0.100)	1.27 (0.050)			
1206	3.06 (0.120)	1.60 (0.063)		0.40 (0.016)	
1505	3.81 (0.150)	1.32 (0.052)		0.48 (0.019)	
2010	5.08 (0.200)	2.54 (0.100)			

Note
- Case size 2512 under development. Please consult Vishay Sfernice.

* Pb containing terminations are not RoHS compliant, exemptions may apply
** Please see document "Vishay Material Category Policy": www.vishay.com/doc?99902

SUGGESTED LAND PATTERN (to IPC-7351A)



CHIP SIZE	DIMENSIONS (in millimeter)		
	$Z_{max.}$	$G_{min.}$	$X_{max.}$
0302	1.30	0.14	0.73
0402	1.55	0.15	0.73
0505	1.82	0.10	1.40
0603	2.37	0.35	0.98
0705/0805	2.76	0.74	1.40
1005	3.39	1.37	1.40
1206	3.91	1.85	1.73
1505	4.66	2.44	1.45
2010	5.93	3.71	2.67

Note

- Case size 2512 under development. Please consult Vishay Sfernice.

ELECTRICAL SPECIFICATIONS

CASE SIZE	POWER RATING mW		LIMITING ELEMENT VOLTAGE V	RESISTANCE RANGE (2)
	Pn (1)	Pd (1)		
0302	40	30	25	10 Ω to 500 kΩ
0402	63	40	50	10 Ω to 1.5 MΩ
0505	125	50	50	10 Ω to 4 MΩ
0603	125	100	75	10 Ω to 2.5 MΩ
0705/0805	200	125	150	10 Ω to 10 MΩ
1005	250	125	75	10 Ω to 5 MΩ
1206	330	250	200	10 Ω to 35 MΩ
1505	350	175	75	10 Ω to 10 MΩ
2010	1000	500	300	10 Ω to 50 MΩ

Notes

- Case size 2512 under development. Please consult Vishay Sfernice.

(1) Pn = Nominal power - Pd = Derated power intended to improve stability.

(2) **For ohmic range versus tolerance and TCR see detailed table page 62.**

ELECTRICAL SPECIFICATIONS

Resistance Range: 10 Ω to 50 MΩ

Resistance Tolerance: ± 0.1 % to ± 1 %
± 0.01 % to ± 0.05 % on Y type

Power Dissipation: **Pn:** 40 mW to 1 W
Pd: 40 mW to 500 mW
on tolerance tighter than ± 0.05 %

Temperature Coefficient: 5 ppm (0 °C; 70 °C);
10 ppm (- 55 °C; + 155 °C)

CLIMATIC SPECIFICATIONS

Operating Temp. Range: - 55 °C to + 155 °C

For temperature up to 215 °C, please consult factory

MECHANICAL SPECIFICATIONS

Substrate: Alumina

Technology: Thin film

Film: **Nickel chromium** with mineral passivation or **CrSi**

Protection: Silicone

Terminations: **B type:** SnPb over nickel barrier for solder reflow
N type: SnAg over nickel barrier
G type: gold over nickel barrier for other applications

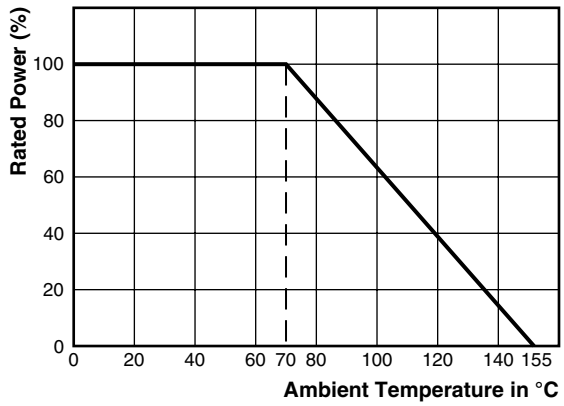
TEMPERATURE COEFFICIENT		
TCR	CODE	FILM
± 5 ppm/°C (1)(2)	Z	NiCr
± 10 ppm/°C (2)	Y	NiCr
± 25 ppm/°C	E	NiCr
± 50 ppm/°C	H	NiCr or CrSi
± 100 ppm/°C	K	NiCr or CrSi

Notes

(1) Reduced temperature operating range:
[0 °C; + 70 °C] option available for (- 25 °C; + 85 °C): 0027
and [- 55 °C; + 155 °C]: 0079

(2) R > 39 Ω on request for lower values.

POWER DERATING CURVE



TOLERANCE AND TCR VERSUS OHMIC VALUE

SIZE	VALUE RANGE	TIGHTEST TOLERANCE %	BEST TCR (ppm/°C)
P0302	10R to 500K	0.1	50
	10R to 75K	0.1	25
	39R to 75K	0.05	25
	39R to 50K	0.05	10 (5) (3)
	100R to 50K	0.02	10 (5) (3)
	250R to 50K	0.01	10 (5) (3)
P0402	10R to 1M5	0.1	50
	10R to 150K	0.1	25
	39R to 150K	0.05	25
	39R to 100K	0.05	10 (5) (3)
	100R to 100K	0.02	10 (5) (3)
	250R to 100K	0.01	10 (5) (3)
P0505	10R to 4M	0.1	50
	10R to 300K	0.1	25
	39R to 300K	0.05	25
	39R to 260K	0.05	10 (5) (3)
	100R to 260K	0.02	10 (5) (3)
	250R to 260K	0.01	10 (5) (3)
P0603	10R to 2M5	0.1	50
	10R to 500K	0.1	25
	39R to 500K	0.05	25
	39R to 332K	0.05	10 (5) (3)
	100R to 332K	0.02	10 (5) (3)
	250R to 332K	0.01	10 (5) (3)
P0705/0805	10R to 10M	0.1	50
	10R to 750K	0.1	25
	39R to 750K	0.05	25
	39R to 511K	0.05	10 (5) (3)
	100R to 511K	0.02	10 (5) (3)
	250R to 511K	0.01	10 (5) (3)
P1005	10R to 5M	0.1	50
	10R to 750K	0.1	25
	39R to 750K	0.05	25
	39R to 500K	0.05	10 (5) (3)
	100R to 500K	0.02	10 (5) (3)
	250R to 500K	0.01	10 (5) (3)
P1206	10R to 35M	0.1	50
	10R to 3M5	0.1	25
	39R to 3M5	0.05	25
	39R to 1M8	0.05	10 (5) (3)
	100R to 1M8	0.02	10 (5) (3)
	250R to 1M8	0.01	10 (5) (3)
P1505	10R to 10M	0.1	50
	10R to 1M	0.1	25
	39R to 1M	0.05	25
	39R to 750K	0.05	10 (5) (3)
	100R to 750K	0.02	10 (5) (3)
	250R to 750K	0.01	10 (5) (3)
P2010	10R to 50M	0.1	50
	10R to 6M	0.1	25
	39R to 6M	0.05	25
	39R to 3M	0.05	10 (5) (3)
	100R to 3M	0.02	10 (5) (3)
	250R to 3M	0.01	10 (5) (3)

Note

- Size 2512 under development. Please consult Vishay Sfernice.

(3) 5 ppm/°C in a reduced operating range (0 °C; + 70 °C). Options available for operating range (- 25 °C; + 85 °C) and (- 55 °C; + 155 °C) upon request with price adder.

POPULAR OPTIONS

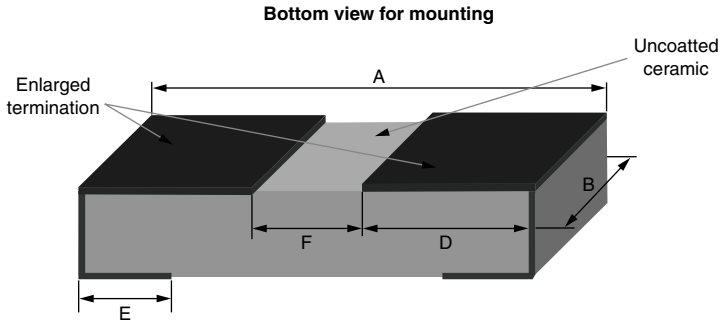
For any option it is recommended to consult Vishay Sfernice for availability first.

Option: Enlarged terminations:

For stringent and special power dissipation requirements, the thermal resistance between the resistive layer and the solder joint can be reduced using enlarged terminations chip resistors which are soldered on large and thick copper pads acting as heatsink (see application note: 53048 Power Dissipation in High Precision Vishay Sfernice Chip Resistors and Arrays (P Thin Film, PRA Arrays, CHP Thick Film) www.vishay.com/doc?53048.

Option to order: 0063 (applies to size 1206/1505/2010).

DIMENSIONS (Option 0063) in millimeters

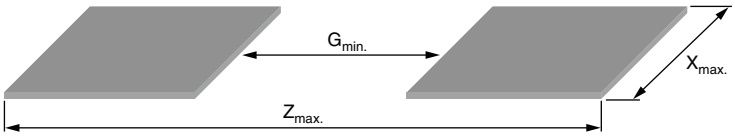


CASE SIZE	A	B	E	D	F		
	MAX. TOL. + 0.152 MIN. TOL. - 0.152	MAX. TOL. + 0.127 MIN. TOL. - 0.127	MAX. TOL. + 0.13 MIN. TOL. - 0.13	MAX. TOL. + 0.13 MIN. TOL. - 0.13			
	NOMINAL	NOMINAL	NOMINAL	NOMINAL	NOMINAL	MIN.	MAX.
1206	3.06	1.60	0.40	1.215	0.63	0.50	0.76
1505	3.81	1.32	0.48	1.59			
2010	5.08	2.54		2.25			

Note

- Case size 2512 under development. Please consult Vishay Sfernice.

SUGGESTED LAND PATTERN (Option 0063)



CHIP SIZE	DIMENSIONS (in millimeter)		
	$Z_{max.}$	$G_{min.}$	$X_{max.}$
1206	3.91	0.50	1.73
1505	4.66		1.45
2010	5.93		2.67

Note

- Case size 2512 under development. Please consult Vishay Sfernice.

Option: Tightest Temperature Coefficient on Extended Temperature Range

Option to order 0027:
TCR: 5 ppm/°C in [- 25 °C; + 85 °C] temperature range. Price adder will apply. Please consult Vishay Sfernice.

Option to order 0079:
TCR: 5 ppm/°C in [- 55 °C; + 155 °C] temperature range. Price adder will apply. Please consult Vishay Sfernice.

Option: High Temperature

For applications such as down hole drilling, high temperature withstanding is required. Vishay Sfernice offers an option for utilization on extended temperature range: [- 55 °C; + 215 °C] powered (and up to 230 °C unpowered).

For guidance in designs, please refer to application note: 53047 Power Dissipation Considerations in High Precision Vishay Sfernice Thin Film Chip Resistors and Arrays (P, PRA etc.) (High Temperature Application) www.vishay.com/doc?53047.

Option to order 0031:

Recommended terminations: Gold (< 1 µ)

Performances:

Best temperature coefficient:

5 ppm/°C in [0 °C; + 70 °C]

10 ppm/°C [- 55 °C; + 155 °C]

15 ppm/°C [- 55 °C; + 185 °C]

25 ppm/°C [- 55 °C; + 215 °C]

Power rating: 0.1 x Pn

Best tolerance after high temperature assembly: 0.1 %

Long term stability: 0.5 % after 1000 h at 215 °C (ambient temperature) at 0.1 Pn

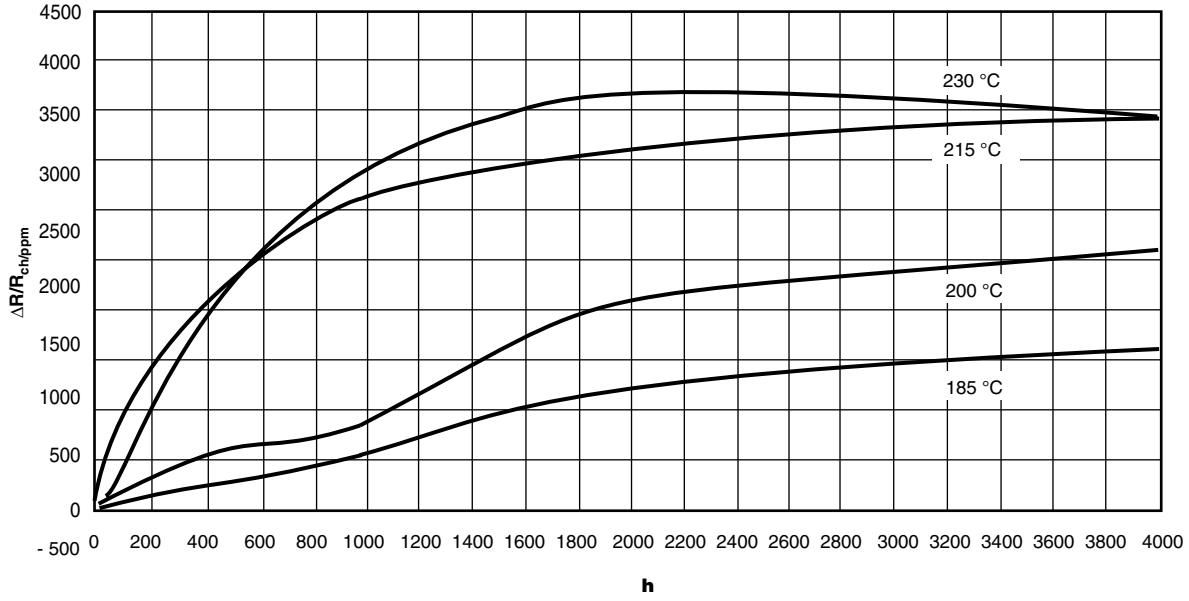
Caution:

Performances obtained with following mounting conditions:

PCB: Polymide

Solder paste: PbSnAg (93.5/5/1.5)

Stability after 4000 h unpowered



Option: Marking

Option to order 0013:
Marking of ohmic value and tolerance:
Sizes: 0805 to 1005: 3 digits marking (according to EIA-96)
Sizes: 1206 to 2010: 4 digits marking (same codification than in the ordering procedure)
Tolerance indicated by a color dot.

Option to order 0014:
Marking of ohmic value:
Sizes: 0805 to 1005: 3 digits marking (according to EIA-96)
Sizes: 1206 to 2010: 4 digits marking (same codification than in the ordering procedure)
No standard marking available for smaller sizes.
A price adder will apply to the unit price of the parts for options 0013 and 0014.

PACKAGING

ESD packaging available: waffle-pack, and plastic tape and reel (low conductivity). Paper tape available upon request (ESD only).

SIZE	MOQ	NUMBER OF PIECES PER PACKAGE			TAPE WIDTH
		WAFFLE PACK 2" × 2"	TAPE AND REEL		
			MIN.	MAX.	
0302	100	100	100	4000	8 mm
0402					
0505					
0603					
0805 0705					
1005		221			
1206		140			
1505		60			
2010			100	2000	8 mm (1)

Note
(1) 12 mm on request

PACKAGING RULES

Waffle Pack
Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered exceeds maximum quantity of a single waffle pack, the waffle packs are stacked up on the top of each other and closed by one single cover.
To get "not stacked up" waffle pack in case of ordered quantity > maximum number of pieces per package: Please consult Vishay Sfernice for specific ordering code

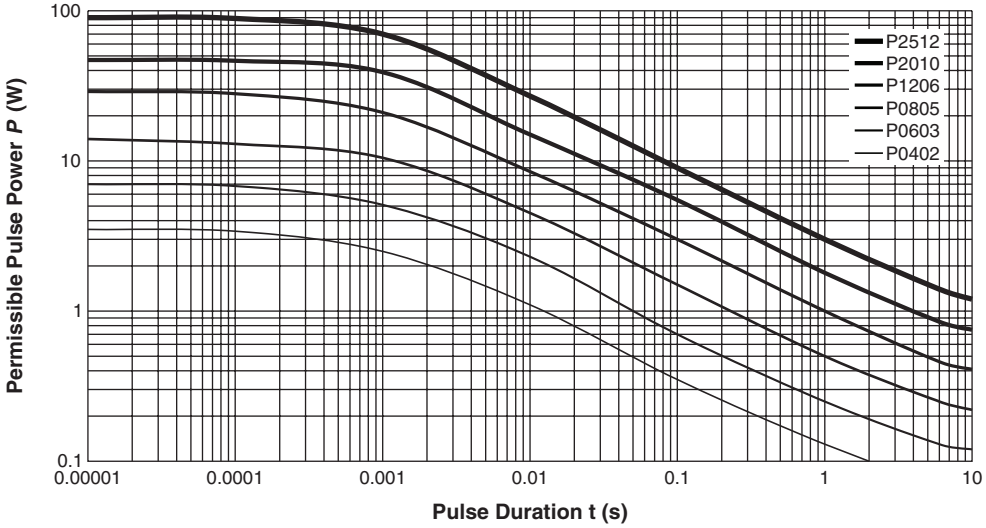
Tape and Reel
Can be filled up to maximum quantity indicated in the table here above, taking into account the minimum order quantity. When quantity ordered is between the MOQ and the maximum reel capacity, only one reel is provided.
When several reels are needed for ordered quantity within MOQ and maximum reel capacity: Please consult Vishay Sfernice for specific ordering code

PERFORMANCE

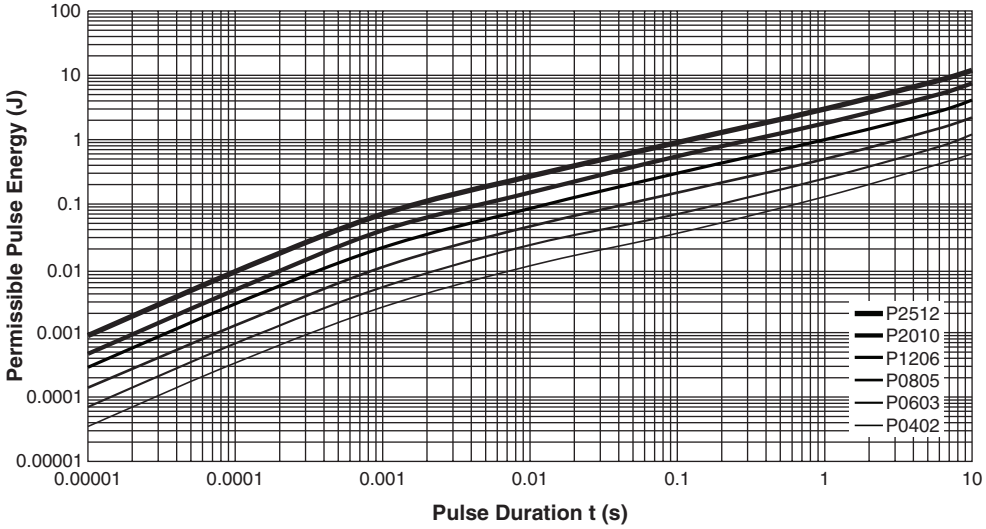
TESTS	CONDITIONS	MIL OR CECC REQUIREMENTS	TYPICAL PERFORMANCES
Thermal Shock	MIL-PRF-55342G MIL-STD-202 F-Method 107 F	± 0.05 %	± 0.02 %
Short Time Overload	MIL-PRF-55342G PARA 3.10.4.7.5	± 0.05 %	± 0.01 %
Low Temperature Operation	MIL-PRF-55342G PARA 3.9 and 4.7.4	± 0.05 %	± 0.01 %
Resistance to Solder Heat	MIL-PRF-55342G PARA 3.12, 4.7.7, 4.7.1.2	± 0.05 %	± 0.03 %
Moisture Resistance	MIL-PRF-55342G PARA 3.13 and 4.7.8 MIL-STD-202 F-Method 106 E	± 0.10 %	± 0.01 %
	CECC 56 days/40 °C/93 % RH	± 0.10 %	± 0.01 %
	AEC-Q200 85 °C/85 % RH/Pn/10 1000 h	± 0.5 % + 0.05 Ω	Max. < 0.3 % + 0.05 Ω
High Temperature	MIL-PRF-55342G PARA 3.11 and 4.7.6	± 0.05 %	± 0.05 %
Load Life	MIL-PRF-55342G 2000 h Pn at 70 °C MIL-STD-202 F-Method 108 A	± 0.5 %	± 0.10 % (2)

Note
(2) 0.05 % under Pd

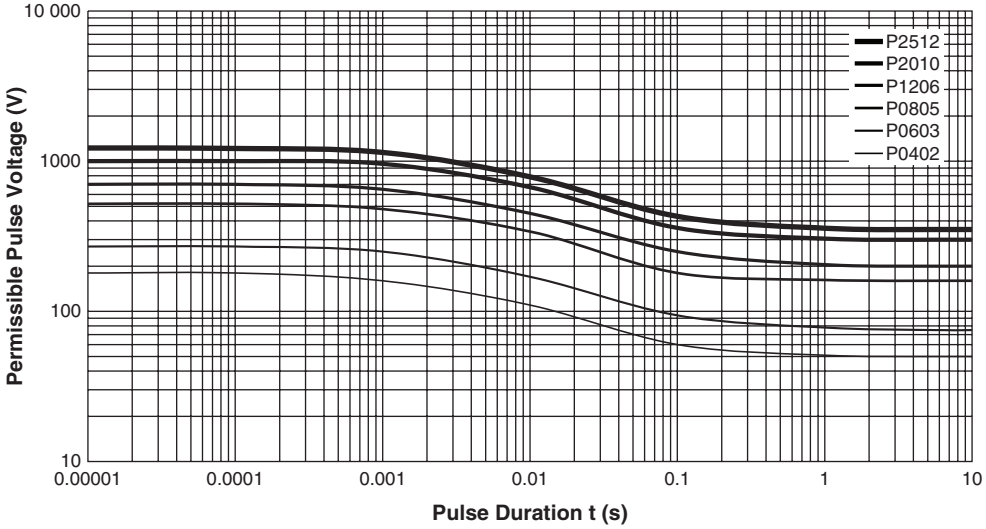
Maximum permissible pulse load P_i max. for single pulse



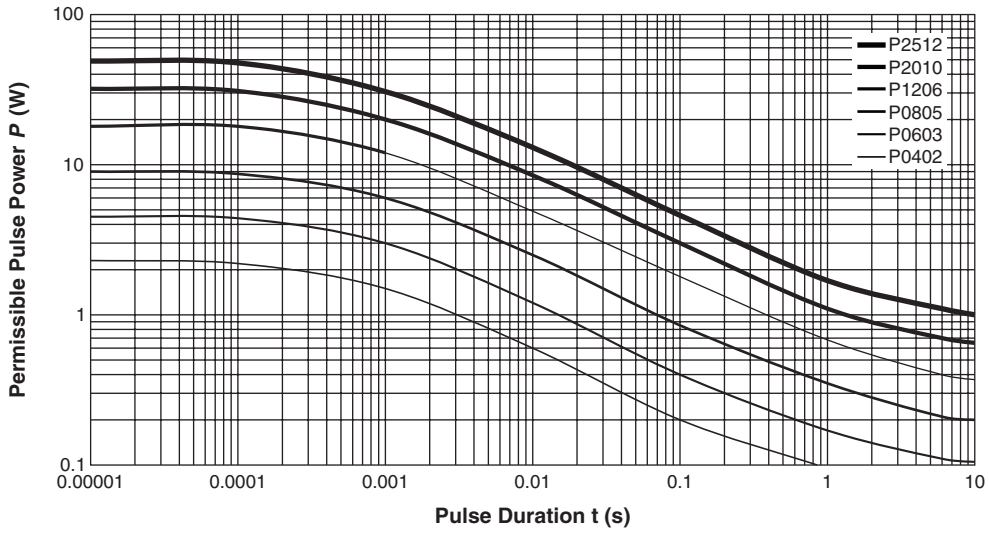
Energy for single pulse



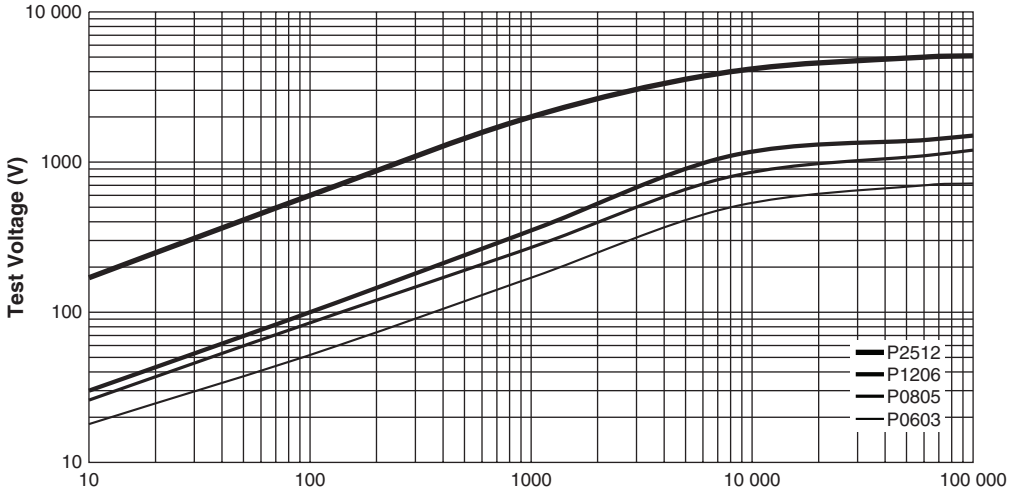
Maximum permissible pulse voltage U_i max.



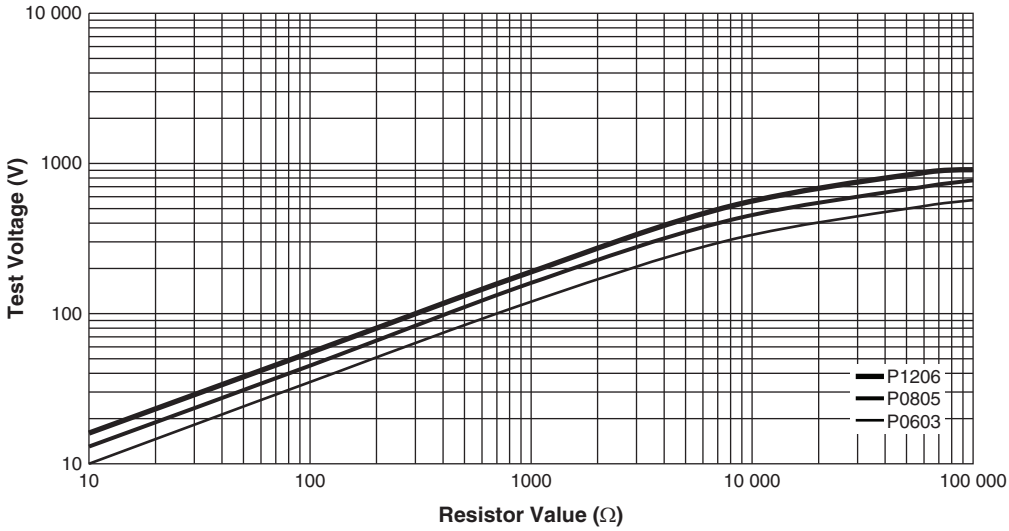
Maximum permissible pulse load P_i max.



1.2/50 µs lightning surge



10/70 µs lightning surge



GLOBAL PART NUMBER INFORMATION

New Global Part Numbering: P0505Y1003BBT0933

P	0	5	0	5	Y	1	0	0	3	B	B	T	0	9	3	3

GLOBAL MODEL	SIZE	TCR	VALUE	TOLERANCE	TERMINATION	PACKAGING	OPTION
P	**0302** **0402** **0505** **0603** **0705** **0805** **1005** **1206** **1505** **2010**	**K** = ± 100 ppm/°C **H** = ± 50 ppm/°C **E** = ± 25 ppm/°C **Y** = ± 10 ppm/°C **X** = Jumper **Z** = ± 5 ppm (0.70 °C)	The first three digits are significant figures and the last digit specifies the number of zeros to follow, R designates decimal point 10R0 = 10 Ω 3901 = 3900 Ω 1004 = 1 MΩ 0R00 = Jumper	**L** = ± 0.01 % **P** = ± 0.02 % **W** = ± 0.05 % **B** = ± 0.1 % **C** = ± 0.25 % **D** = ± 0.5 % **F** = ± 1 % **G** = ± 2 % **J** = ± 5 % **X** = Jumper	**B:** SnPb over nickel barrier **N:** SnAg over nickel barrier **G:** Gold over nickel barrier **B:** Lead bearing version **N and G:** Lead (Pb)-free/ RoHS version	**Blank** = Waffle pack **T** = Tape (1) **PT** = Paper tape (2)	Leave blank if no option

Historical Part Number example: P 0505 Y 1003 B B TR R0933 e2

P	0505	Y	1003	B	B	TR	R0933	e2
HISTORICAL MODEL	SIZE	TCR	VALUE	TOLERANCE	TERMINATION	PACKAGING	OPTION	RoHS
P	**0302** **0402** **0505** **0603** **0705** **0805** **1005** **1206** **1505** **2010**	**K** = ± 100 ppm/°C **H** = ± 50 ppm/°C **E** = ± 25 ppm/°C **Y** = ± 10 ppm/°C **X** = Jumper **Z** = ± 5 ppm (0.70 °C)	The first three digits are significant figures and the last digit specifies the number of zeros to follow, R designates decimal point 10R0 = 10 Ω 3901 = 3900 Ω 1004 = 1 MΩ 0R00 = Jumper	**L** = ± 0.01 % **P** = ± 0.02 % **W** = ± 0.05 % **B** = ± 0.1 % **C** = ± 0.25 % **D** = ± 0.5 % **F** = ± 1 % **G** = ± 2 % **J** = ± 5 % **X** = Jumper	**B:** SnPb over nickel barrier **N:** SnAg over nickel barrier **G:** Gold over nickel barrier **B:** Lead bearing version **N and G:** Lead (Pb)-free/ RoHS version	**Blank** = Waffle pack **TR** = Tape (1)	Leave blank if no option	e2: Tin/silver e4: Gold blank: SnPb

Notes

- Chips ready to be trimmed available. (P_{trim}) - Please consult Vishay Sfernice.

(1) For specific quantity of parts per packaging please consult Vishay Sfernice.

(2) For paper tape please consult Vishay Sfernice.

QUICK PROTOTYPING

Vishay Sfernice can offer quick prototyping service in 3 weeks production time for most popular case sizes: 0603, 0805, 1206 (Best tolerance: 0.05 %, best TCR: 10 ppm/°C) - Premium will apply - Check availability

Disclaimer

All product specifications and data are subject to change without notice.

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