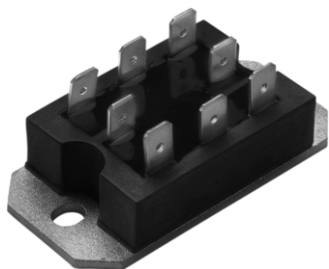



Passivated Assembled Circuit Elements, 40 A



PACE-PAK (D-19)

FEATURES

- Glass passivated junctions for greater reliability
- Electrically isolated base plate
- Available up to 1200 V_{RRM}/V_{DRM}
- High dynamic characteristics
- Wide choice of circuit configurations
- Simplified mechanical design and assembly
- UL E78996 approved 
- Compliant to RoHS directive 2002/95/EC



RoHS
COMPLIANT

PRODUCT SUMMARY

| | |
|-------|------|
| I_o | 40 A |
|-------|------|

DESCRIPTION

The P400 series of integrated power circuits consists of power thyristors and power diodes configured in a single package. With its isolating base plate, mechanical designs are greatly simplified giving advantages of cost reduction and reduced size.

Applications include power supplies, control circuits and battery chargers.

MAJOR RATINGS AND CHARACTERISTICS

| SYMBOL | CHARACTERISTICS | VALUES | UNITS |
|--------------------------|-----------------|-------------|-------------------|
| I_o | 80 °C | 40 | A |
| I_{TSM} , I_{FSM} | 50 Hz 60 Hz | 385 400 | A |
| I^2t | 50 Hz 60 Hz | 745 680 | A ² s |
| $I^2\sqrt{t}$ | | 7450 | A ² √s |
| V_{RRM} | Range | 400 to 1200 | V |
| V_{ISOL} | | 2500 | V |
| T_J T_{Stg} | | - 40 to 125 | °C |

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS

| TYPE NUMBER | V_{RRM}/V_{DRM} , MAXIMUM REPETITIVE PEAK REVERSE AND PEAK OFF-STATE VOLTAGE V | V_{RSM} , MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V | I_{RRM} MAXIMUM AT T_J MAXIMUM mA |
|------------------|---|--|--|
| P401, P421, P431 | 400 | 500 | 10 |
| P402, P422, P432 | 600 | 700 | |
| P403, P423, P433 | 800 | 900 | |
| P404, P424, P434 | 1000 | 1100 | |
| P405, P425, P435 | 1200 | 1300 | |

| ON-STATE CONDUCTION | | | | | | |
|--|-------------------------------------|--|----------------------------------|---|--------|-------------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | | VALUES | UNITS |
| Maximum DC output current at case temperature | I _O | Full bridge circuits | | | 40 | A |
| | | | | | 80 | °C |
| Maximum peak, one-cycle non-repetitive on-state or forward current | I _{TSM} , I _{FSM} | t = 10 ms | No voltage reapplied | Sinusoidal half wave, initial T _J = T _J maximum | 385 | A |
| | | t = 8.3 ms | | | 400 | |
| | | t = 10 ms | 100 % V _{RRM} reapplied | | 325 | |
| | | t = 8.3 ms | | | 340 | |
| Maximum I ² t for fusing | I ² t | t = 10 ms | No voltage reapplied | | 745 | A ² s |
| | | t = 8.3 ms | | | 680 | |
| | | t = 10 ms | 100 % V _{RRM} reapplied | | 530 | |
| | | t = 8.3 ms | | | 480 | |
| Maximum I ² √t for fusing | I ² √t | t = 0.1 ms to 10 ms, no voltage reapplied I ² t for time tx = I ² √t · √tx | | | 7450 | A ² √s |
| Low level value of threshold voltage | V _{T(TO)1} | (16.7 % x π x I _{T(AV)}) < I < π x I _{T(AV)} , T _J = T _J maximum | | | 0.83 | V |
| High level value of threshold voltage | V _{T(TO)2} | (I > π x I _{T(AV)}), T _J = T _J maximum | | | 1.03 | |
| Low level value of on-state slope resistance | r _{t1} | (16.7 % x π x I _{T(AV)}) < I < π x I _{T(AV)} , T _J = T _J maximum | | | 9.61 | mΩ |
| High level value of on-state slope resistance | r _{t2} | (I > π x I _{T(AV)}), T _J = T _J maximum | | | 7.01 | |
| Maximum on-state voltage drop | V _{TM} | I _{TM} = π x I _{T(AV)} | | T _J = 25 °C | 1.4 | V |
| Maximum forward voltage drop | V _{FM} | I _{FM} = π x I _{F(AV)} | | | | |
| Maximum non-repetitive rate of rise of turned-on current | di/dt | T _J = 125 °C from 0.67 V _{DRM} I _{TM} = π x I _{T(AV)} , I _g = 500 mA, t _r < 0.5 μs, t _p > 6 μs | | | 200 | A/μs |
| Maximum holding current | I _H | T _J = 25 °C anode supply = 6 V, resistive load | | | 130 | mA |
| Maximum latching current | I _L | | | | 250 | |

| BLOCKING | | | | |
|---|-------------------------------------|--|--------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | VALUES | UNITS |
| Maximum critical rate of rise of off-state voltage | dV/dt | T _J = 125 °C, exponential to 0.67 V _{DRM} gate open | 200 | V/μs |
| Maximum peak reverse and off-state leakage current at V _{RRM} , V _{DRM} | I _{RRM} , I _{DRM} | T _J = 125 °C, gate open circuit | 10 | mA |
| Maximum peak reverse leakage current | I _{RRM} | T _J = 25 °C | 100 | μA |
| RMS isolation voltage | V _{ISOL} | 50 Hz, circuit to base, all terminals shorted, T _J = 25 °C, t = 1 s | 2500 | V |

| TRIGGERING | | | | | | |
|--|--------------------|---|--------------------------------------|--------|-------|--|
| PARAMETER | SYMBOL | TEST CONDITIONS | | VALUES | UNITS | |
| Maximum peak gate power | P _{GM} | | | 8 | W | |
| Maximum average gate power | P _{G(AV)} | | | 2 | | |
| Maximum peak gate current | I _{GM} | | | 2 | A | |
| Maximum peak negative gate voltage | -V _{GM} | | | 10 | V | |
| Maximum gate voltage required to trigger | V _{GT} | T _J = - 40 °C | Anode supply = 6 V resistive load | 3 | V | |
| | | T _J = 25 °C | | 2 | | |
| | | T _J = 125 °C | | 1 | | |
| Maximum gate current required to trigger | I _{GT} | T _J = - 40 °C | | 90 | mA | |
| | | T _J = 25 °C | | 60 | | |
| | | T _J = 125 °C | | 35 | | |
| Maximum gate voltage that will not trigger | V _{GD} | T _J = 125 °C, rated V _{DRM} applied | | 0.2 | V | |
| Maximum gate current that will not trigger | I _{GD} | | | 2 | mA | |

| THERMAL AND MECHANICAL SPECIFICATIONS | | | | |
|---|-----------------------------------|--------------------------------------|-------------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | VALUES | UNITS |
| Maximum junction operating and storage temperature range | T _J , T _{Stg} | | - 40 to 125 | °C |
| Maximum thermal resistance, junction to case per junction | R _{thJC} | DC operation | 1.05 | K/W |
| Maximum thermal resistance, case to heatsink | R _{thCS} | Mounting surface, smooth and greased | 0.10 | |
| Mounting torque, base to heatsink ⁽¹⁾ | | | 4 | Nm |
| Approximate weight | | | 58 | g |
| | | | 2.0 | oz. |

Note

⁽¹⁾ A mounting compound is recommended and the torque should be checked after a period of 3 hours to allow for the spread of the compound

| CIRCUIT TYPE AND CODING ⁽¹⁾ | | | |
|--|---|------------------------------------|-----------------------------|
| | CIRCUIT "0" | CIRCUIT "2" | CIRCUIT "3" |
| Terminal positions | | | |
| Schematic diagram | | | |
| | Single phase hybrid bridge common cathode | Single phase hybrid bridge doubler | Single phase all SCR bridge |
| Basic series | P40. | P42. | P43. |
| With voltage suppression | P40.K | P42.K | P43.K |
| With freewheeling diode | P40.W | - | - |
| With both voltage suppression and freewheeling diode | P40.KW | - | - |

Note

⁽¹⁾ To complete code refer to Voltage Ratings table, i.e.: For 600 V P40.W complete code is P402W

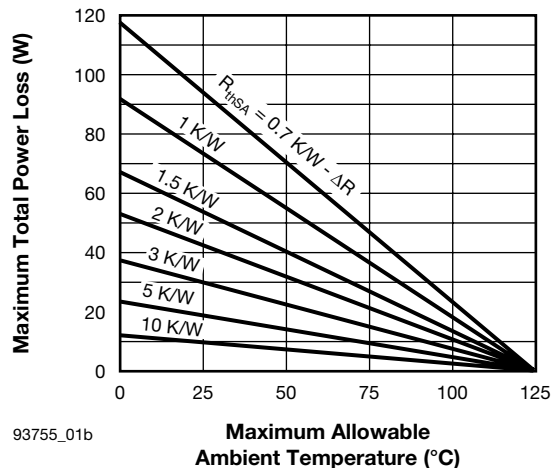
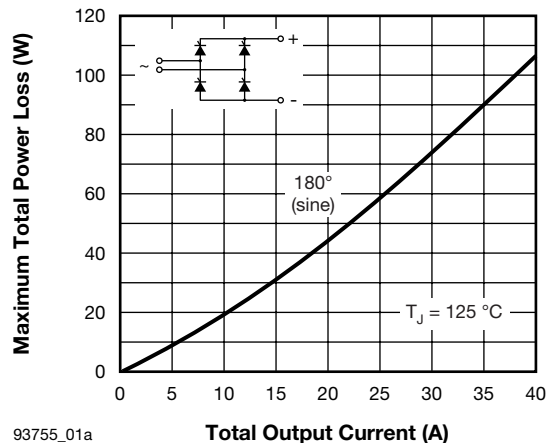


Fig. 1 - Current Ratings Nomogram (1 Module Per Heatsink)

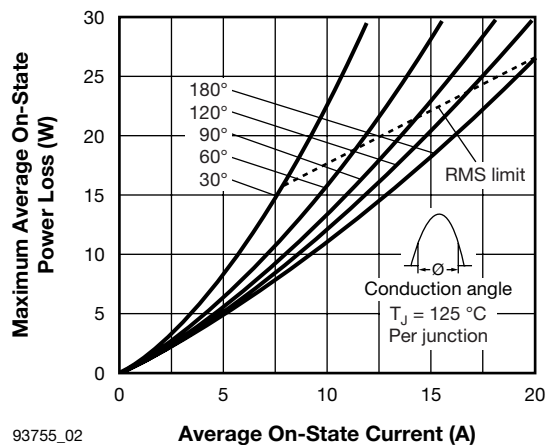


Fig. 2 - On-State Power Loss Characteristics

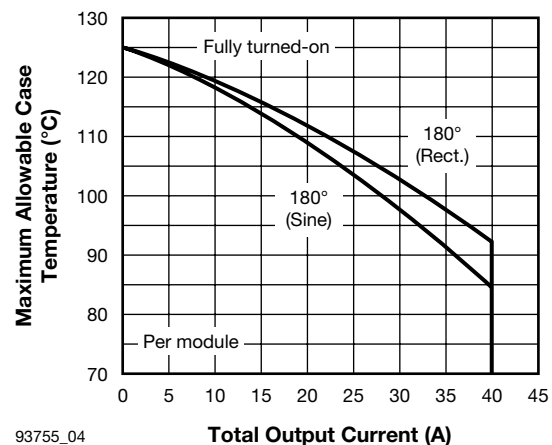


Fig. 4 - Current Ratings Characteristics

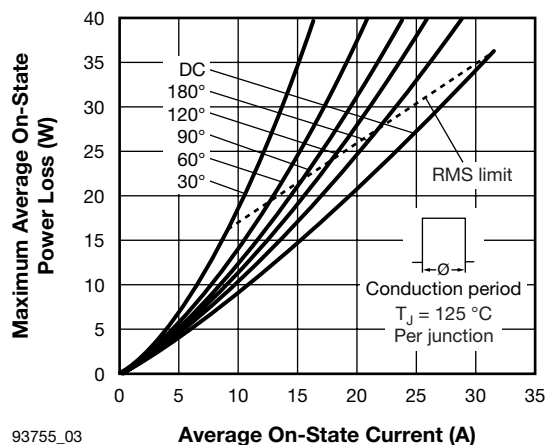


Fig. 3 - On-State Power Loss Characteristics

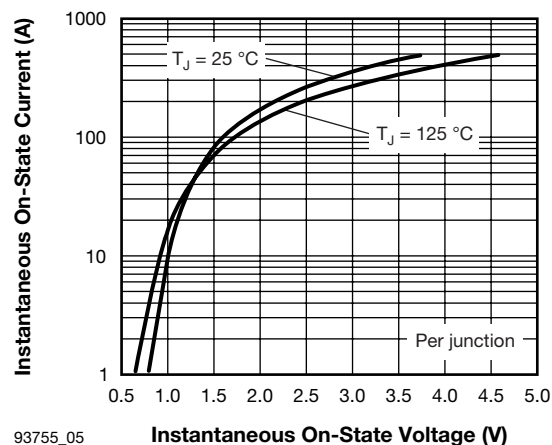


Fig. 5 - On-State Voltage Drop Characteristics

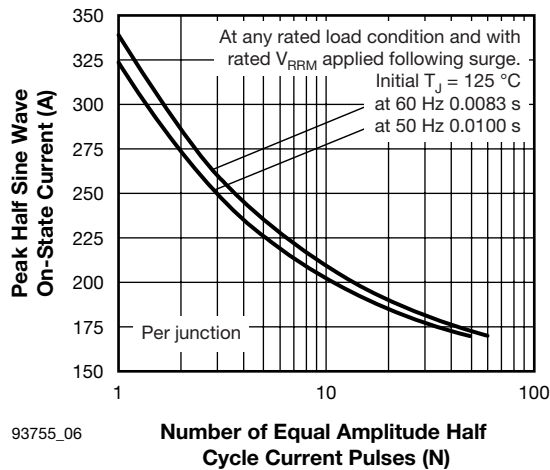


Fig. 6 - Maximum Non-Repetitive Surge Current

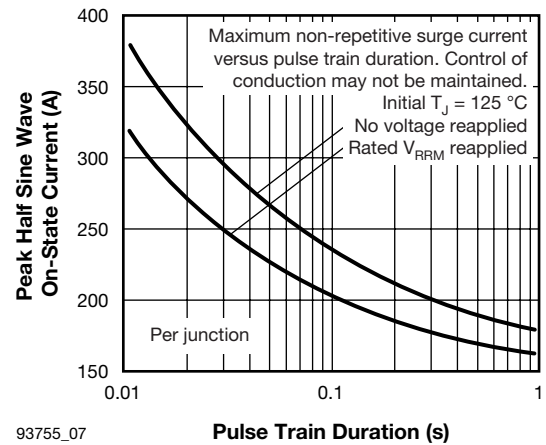


Fig. 7 - Maximum Non-Repetitive Surge Current

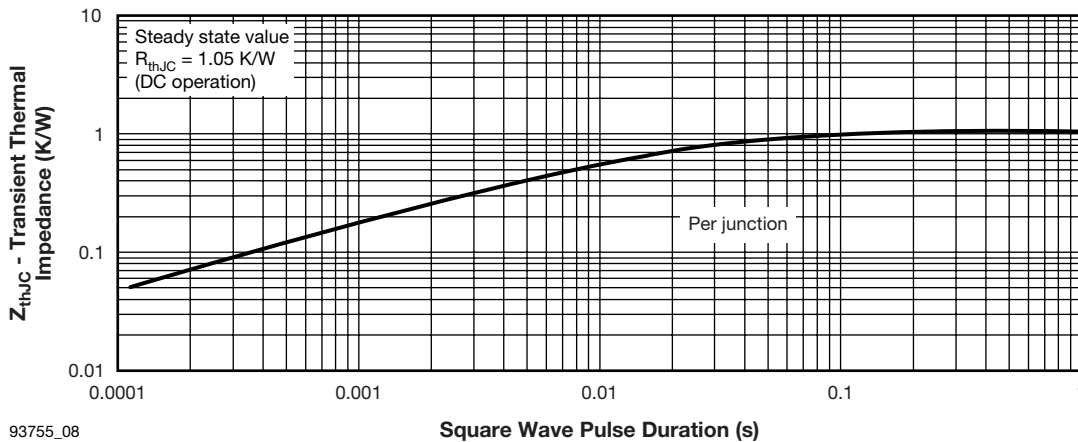


Fig. 8 - Thermal Impedance Z_{thJC} Characteristics

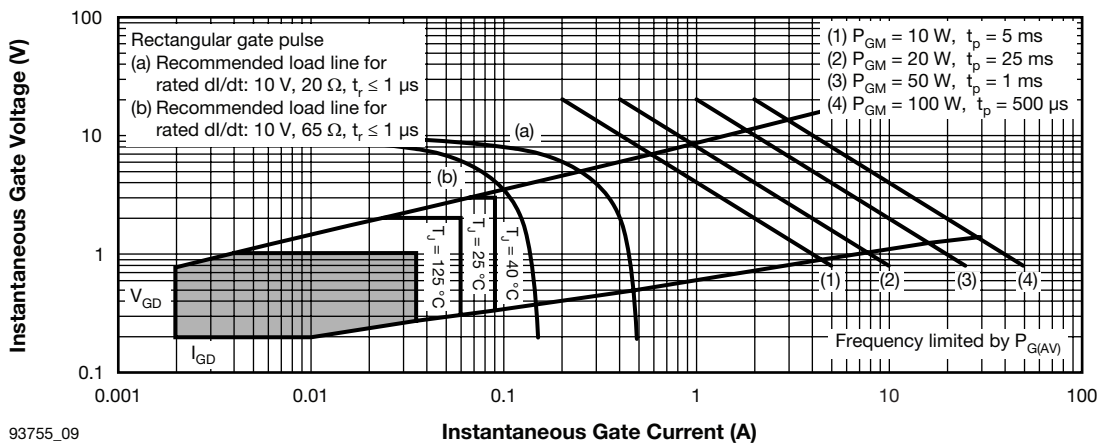


Fig. 9 - Gate Characteristics

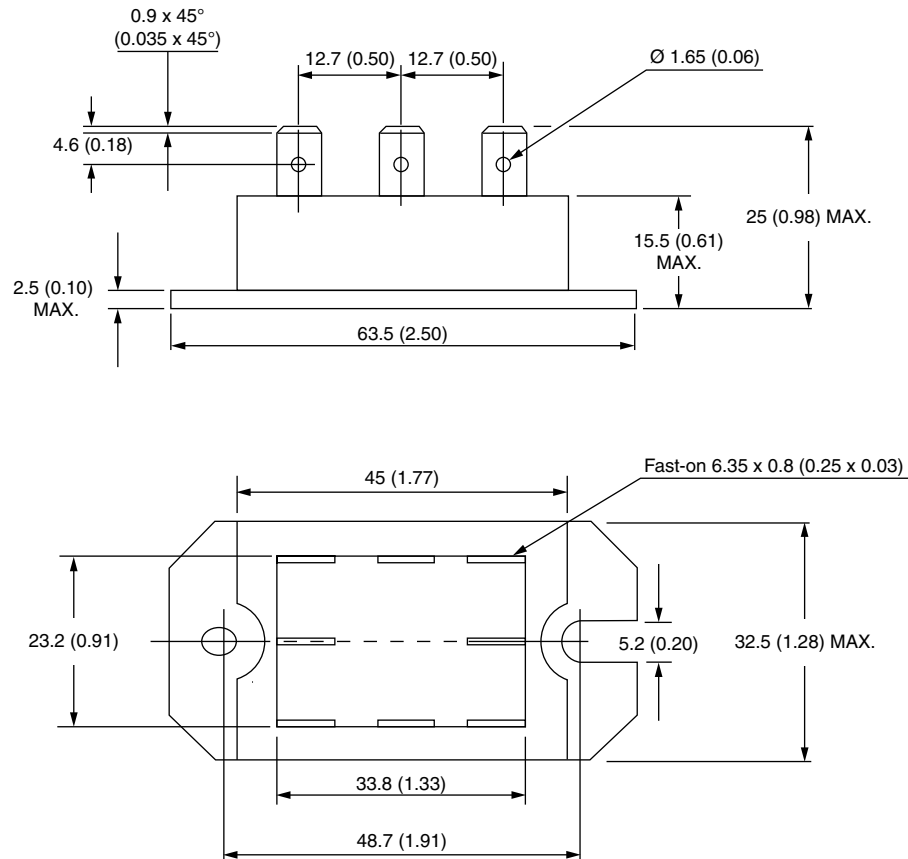
LINKS TO RELATED DOCUMENTS

Dimensions

www.vishay.com/doc?95335

D-19 PACE-PAK

DIMENSIONS in millimeters (inches)





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