Monolithic 3XSPDT PMOS Switch with Driver

Siliconix

designed for . . .

- **Make-Before-Break Switching i.e. Feedback Resistor Switching in Variable Gain Op-Amps**
- **Low Leakage Switching such as Sample and Hold Circuits**

BENEFITS

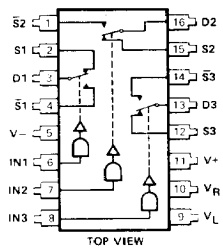
- **Easily Interfaced**
  - TTL, CMOS, DTL Direct Driver Compatibility
- **Reduces External Component Requirements**
  - No Interface Components Required

DESCRIPTION

The DG170 contains six MOS field-effect transistors designed to function as a single-pole, double-throw electronic switches. In the ON state, each switch will conduct current equally well in either direction. In the OFF state, the switch will block voltages up to 20 V peak-to-peak. A level-shifting push-pull driver enables low-level logic to control the state of the switch.

PIN CONFIGURATION

Dual-In-Line Package

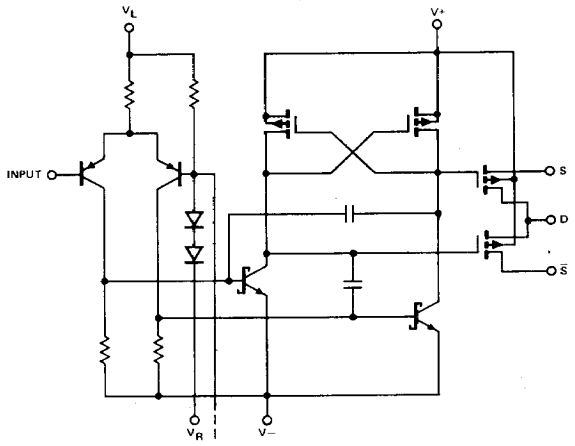


TOP VIEW

ORDER NUMBERS: DG170AP OR DG170BP
SEE PACKAGE 12
DG170CJ
SEE PACKAGE 8

SWITCH STATES ARE FOR LOGIC "1" INPUTS
(POSITIVE LOGIC)

SCHEMATIC DIAGRAM (One SPDT Function Shown)



LOGIC	DRAIN-TO-SOURCE	DRAIN-TO-SOURCE
0	OFF	ON
1	ON	OFF

ABSOLUTE MAXIMUM RATINGS

V+ to V−	36 V
V+ to V_D	25 V
V+ to $V_{S(\overline{S})}$	25 V
$V_{S(\overline{S})}$ to V−	36 V
V_D to V−	36 V
$V_{S(\overline{S})}$ to V_D	25 V
V_L to V−	30 V
V_L to V_{IN}	±12 V
V_L to V_R	±6 V
V_{IN} to V_R	+18, −6 V
Current DC (Any Terminal)	12 mA
Peak I_S, $I_{\overline{S}}$, I_D (200 μs pulse width, 100 pps)	100 mA
Storage Temp. (A & B Suffix)	−65 to 150°C
(C Suffix)	−65 to 125°C
Power Dissipation (P Package Suffix)*	825 mW
(J Package Suffix)*	470 mW
Thermal Resistance (θ_{JA}, J Package Suffix)	0.16°C/mW

*All leads soldered or welded to PC board. For P package suffix, derate 11 mW/°C above +75°C. For J package suffix, derate 6.5 mW/°C above +25°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

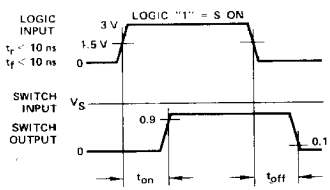
		CHARACTERISTIC		MAX LIMITS DG170AP −55°C	DG170AP 25°C	DG170AP 125°C	DG170BP/(DG170CJ) −20°C [0°C]	DG170BP/(DG170CJ) 25°C	DG170BP/(DG170CJ) 85°C [70°C]	UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 10 V, V− = −20 V, V_L = 5 V, V_R = 0	
1	SWITCH	$r_{DS(on)}$	Drain-Source ON Resistance	200	200	300	250	250	300	Ω	V_D = 10 V, I_S = −1 mA	V_{IN} = 2 V (S ON), V_{IN} = 0.8 V ($\overline{S}$ ON)
2				250	250	400	300	300	450		V_D = 0, I_S = −1 mA	
3				800	800	1200	850	850	1300		V_D = −10 V, I_S = −0.1 mA	
4		$I_{S(off)}$ or $I_{\overline{S}(off)}$	Source OFF Leakage Current		−1	−1000		−5	−100	nA	V_S = −10 V, V_D = 10 V, $I_{\overline{S}}$ = 0, V_{IN} = 0.8 V, $V_{\overline{S}}$ = −10 V, V_D = 10 V, I_S = 0, V_{IN} = 2 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		−2	−2000		−10	−200		V_D = −10 V, V_S = 10 V, V_{IN} = 0.8 V, $I_{\overline{S}}$ = 0	
6		$I_{D(on)}$ + $I_{S(on)}$	Channel ON Leakage Current		2	2000		10	200		V_D = V_S = 10 V, $V_{\overline{S}}$ = −10 V, V_{IN} = 2 V	
7	IN	I_{INL}	Input Current, Input Voltage Low	−0.4	−0.3	−0.3	−0.4	−0.3	−0.3	mA	V_{IN} = 0 ($\overline{S}$ ON)	
8		I_{INH}	Input Current, Input Voltage High	0.1	0.1	10	0.1	0.1	10	μA	V_{IN} = 5 V (S ON)	
9	DYNAMIC	t_{on}	Turn-ON Time		300			300		ns	See Switching Time Test Circuit	
10		t_{off}	Turn-OFF Time		400			400				
11		$C_{S(off)}$	Source OFF Capacitance		5 Typ*			5 Typ*		pF	V_S = 0, I_D = 0	f = 1 MHz
12		$C_{D(off)}$	Drain OFF Capacitance		10 Typ*			10 Typ*			V_D = 0, I_S = 0	
13		$C_{D(on)}$ + $C_{S(on)}$	Channel ON Capacitance		25 Typ*			25 Typ*			V_D = V_S = 0	
14		Off Isolation		Typ > 50 dB at 2 MHz*							R_L = 100 Ω, C_L = 3 pF	
15	SUPPLY	I+	Positive Supply Current		2			2.4		μA	All V_{IN} = 0 (All $\overline{S}$ ON)	
16		I−	Negative Supply Current		−8			−10		mA		
17		I_L	Logic Supply Current		7			9				
18		I_R	Reference Supply Current		−0.8			−1				
19		I+	Positive Supply Current		2			2.4		μA	All V_{IN} = 5 V (All S ON)	
20		I−	Negative Supply Current		−7			−9		mA		
21		I_L	Logic Supply Current		6			8				
22		I_R	Reference Supply Current		−0.8			−1				

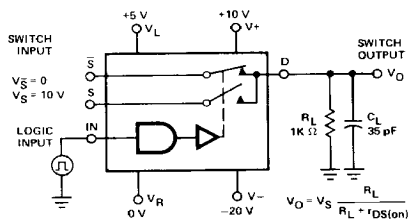
*Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

CMPA

SWITCHING TIME TEST CIRCUIT

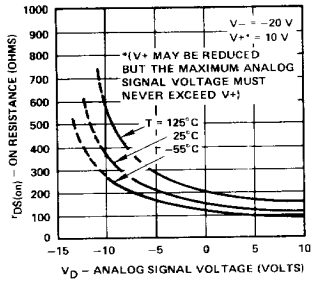
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



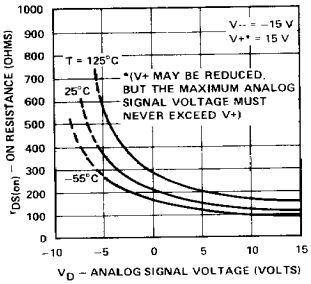


TYPICAL CHARACTERISTICS

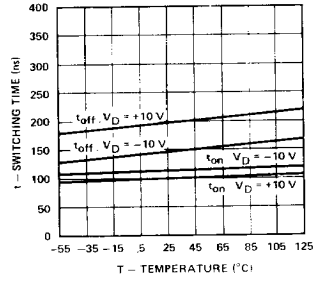
$r_{DS(on)}$ vs V_D and Temperature



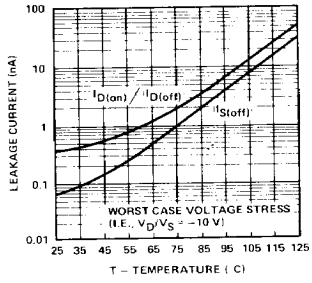
$r_{DS(on)}$ vs V_D and Temperature



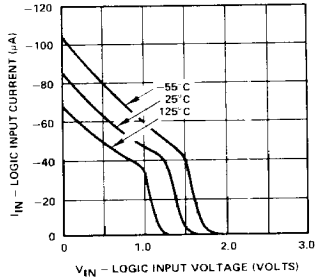
Switching Time vs Temperature and V_D



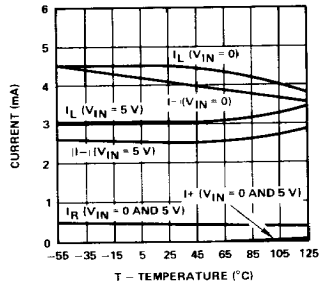
Leakage Currents vs Temperature



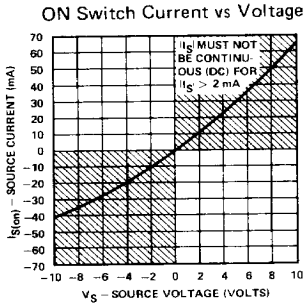
I_{IN} vs V_{IN}

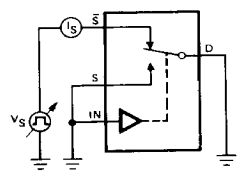


Supply Current vs Temperature

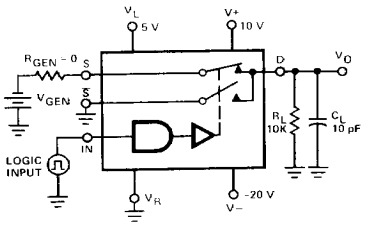


ON Switch Current vs Voltage

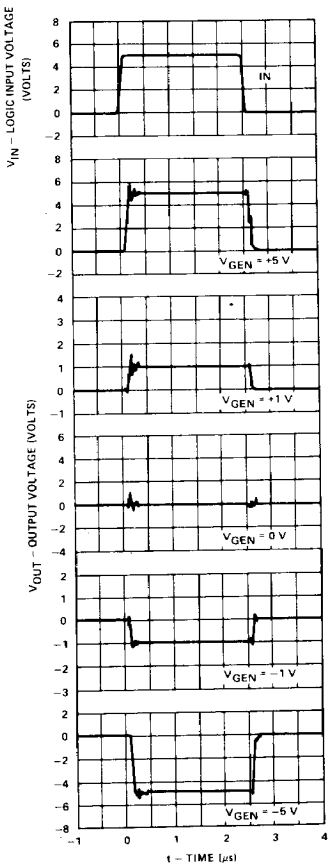




Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.



Control Interface. The logic control input circuit sources less than 0.4 mA for "0" inputs, has a switching threshold of 1.2 V, has very high impedance for "1" inputs, and has a breakdown voltage greater than 15 V. These characteristics make the DG170 directly compatible with all popular logic forms: TTL, CMOS, and DTL.

Analog Signal Range. The range of analog signal voltage levels which can be properly switched depends on the values of V+ and V−. Positive signals may equal V+. Negative signals must be 10 V more positive than V−. The negative limit is not absolute but $r_{DS(on)}$ becomes very large very fast beyond the limit (see $r_{DS(on)}$ versus V_D typical characteristics).

Power Supply Options. The values of V+ = 10 V and V− = −20 V are necessary to switch analog signals from +10 V to −10 V. Other values of V+ and V− may be used but operating characteristics will change. Except for the analog signal range the changes are essentially negligible. Three factor must be considered when changing V+ and V−: the absolute maximum ratings, the analog signal range (see above), and $V+ + |V-| \geq 15$ V.

Power Off and Overvoltage. If positive analog signals are present with V+ = 0 a potentially damaging short circuit exists. The low impedance path is from each switch terminal (S, $\overline{S}$, and D) to V+. The equivalent circuit representation is a diode (see Figure 1).

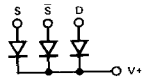
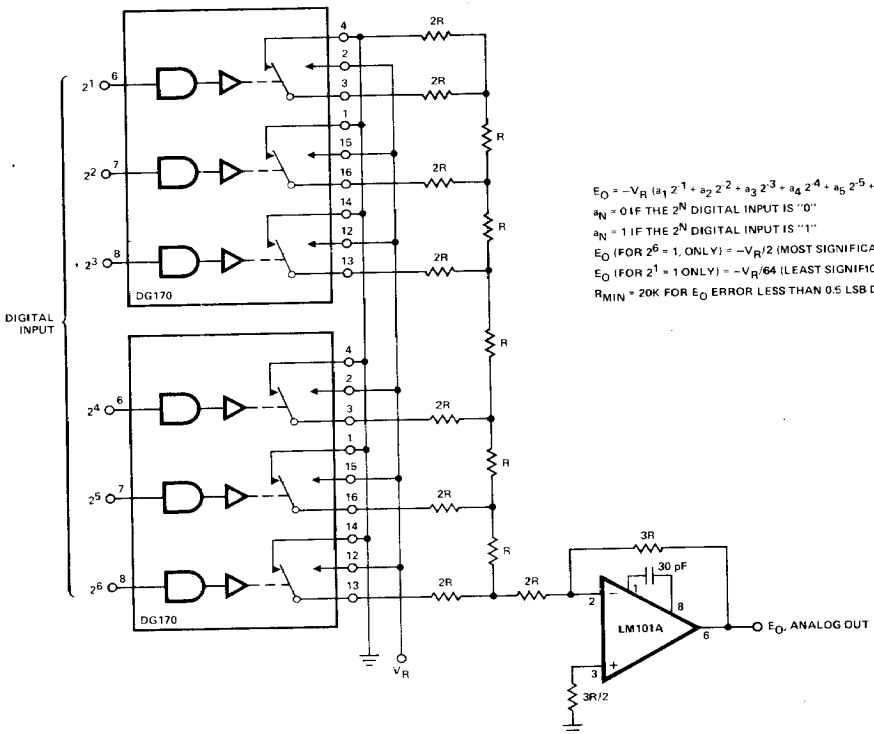
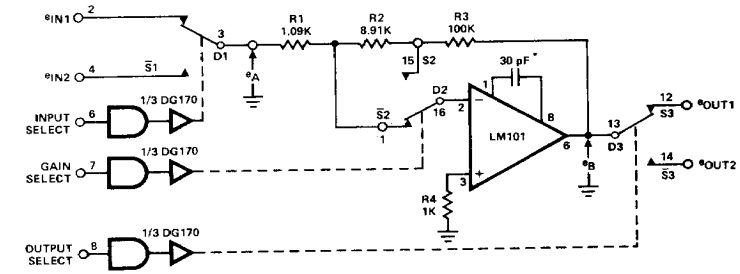


Figure 1.

6-Bit D/A Converter



Programmable Gain Amplifier with Multiplexed Inputs and Outputs



GAIN SELECT = "0" → $A_V = \frac{e_B}{e_A} = -\frac{R_2 + R_3}{R_1} = -99.9$

GAIN SELECT = "1" → $A_V = \frac{e_B}{e_A} = -\frac{R_3}{R_1 + R_2} = -10.0$