
HM62832UH Series

32768-word $\times$ 8-bit High Speed CMOS Static RAM

HITACHI

Rev. 0.0
Dec. 1, 1995

Features

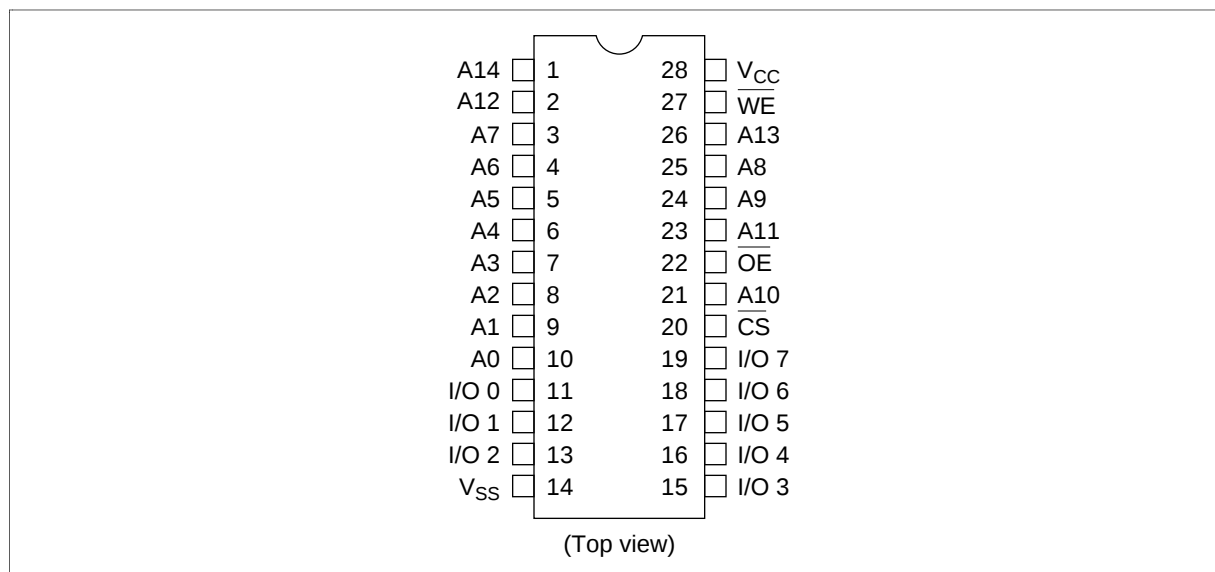
- High speed: Fast access time 15/20 ns (max)
- Low Power
Standby: 15 μ W (typ) (L-version)
Operation: 675/600 mW (typ)
- Single 5 V supply
- Completely static memory
No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs

Ordering Information

Type No.	Access Time	Package
HM62832UHP-15 HM62832UHP-20	15 ns 20 ns	300-mil 28-pin plastic DIP (DP-28NA)
HM62832UHLP-15 HM62832UHLP-20	15 ns 20 ns	
HM62832UHJP-15 HM62832UHJP-20	15 ns 20 n	300-mil 28-pin plastic SOJ (CP-28DN)
HM62832UHLJP-15 HM62832UHLJP-20	15 ns 20 ns	

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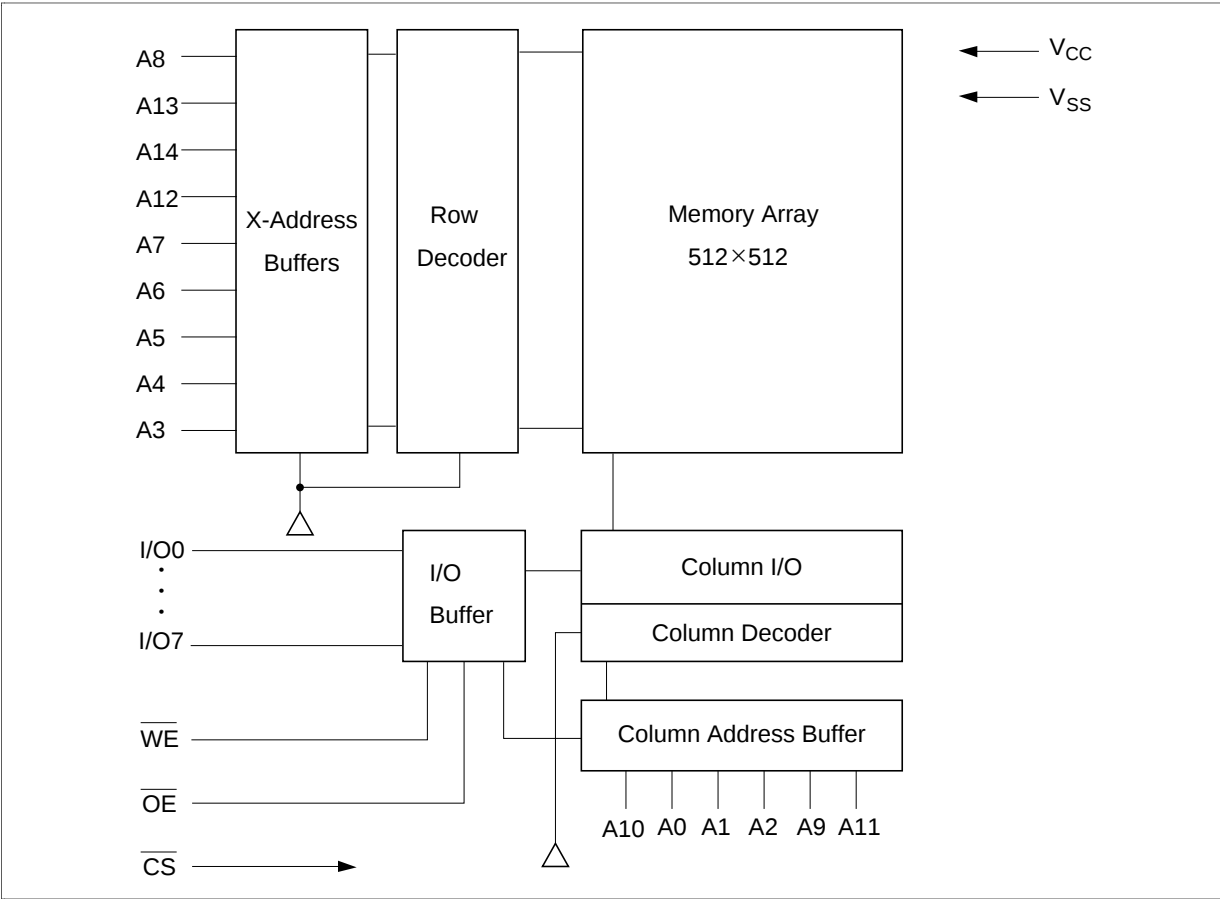
Pin Arrangement



Pin Description

Pin name	Function
A0 – A14	Address
I/O0 – I/O7	Input/output
$\overline{\text{CS}}$	Chip select
$\overline{\text{WE}}$	Write enable
$\overline{\text{OE}}$	Output enable
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



Function Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	V _{CC} Current	I/O Pin	Ref. Cycle
H	X	X	Standby	I _{SB} , I _{SB1}	High-Z	
L	L	H	Read	I _{CC}	Dout	Read cycle 1, 2, 3
L	H	L	Write	I _{CC}	Din	Write cycle 1
L	L	L	Write	I _{CC}	Din	Write cycle 2

Note: X : H or L

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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply voltage ^{*1}	V _{CC}	−0.5 ^{*2} to +7.0	V
Voltage on any pin relative to V _{SS} ^{*1}	V _T	−0.5 ^{*2} to V _{CC} + 0.5	V
Power dissipation	P _T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	−55 to +125	°C
Storage temperature under bias	Tbias	−10 to +85	°C

Notes: 1. With respect to V_{SS}

2. V_{CC} and V_T min = −2.5 V for pulse width ≤ 10 ns

Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	4.5	5.0	5.5	V
	V _{SS}	0	0	0	V
Input high (logic 1) voltage	V _{IH}	2.2	—	V _{CC} + 0.5	V
Input low (logic 0) voltage	V _{IL}	−0.5 ^{*1}	—	0.8	V

Note: 1. V_{IL} min = −2.0 V for pulse width ≤ 10 ns

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DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ ^{*1}	Max	Unit	Test Conditions
Input leakage current	I _{IL}	—	—	2.0	μA	V _{CC} = 5.5 V V _{in} = V _{SS} to V _{CC}
Output leakage current	I _{LO}	—	—	2.0	μA	$\overline{CS} = V_{IH}$ V _{I/O} = V _{SS} to V _{CC}
Operating V _{CC} current	I _{CC1} (-15) ^{*3}	—	135	170	mA	min cycle ^{*2}
	I _{CC2} (-15)	—	100	120	mA	2x min cycle
	I _{CC1} (-20)	—	120	150	mA	min cycle
	I _{CC2} (-20)	—	90	110	mA	2x min cycle
Standby V _{CC} current	I _{SB} (-15)	—	40	60	mA	$\overline{CS} = V_{IH}$, min cycle
	I _{SB} (-20)	—	30	50		
Standby V _{CC} current (1)	I _{SB1} (L-version)	—	0.02	2.0	mA	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ 0 V ≤ V _{in} ≤ 0.2 V or V _{CC} - 0.2 V ≤ V _{in}
		—	0.003	0.1		
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 8 mA
Output high voltage	V _{OH}	2.4	—	—	V	I _{OH} = -4.0 mA

Notes: 1. Typical values are at V_{CC} = 5.0 V, Ta = 25°C and not guaranteed.

2. $\overline{CS} = V_{IL}$, I_{out} = 0 mA

3. Access time version

Capacitance (Ta = 25°C, f = 1.0 MHz)^{*1}

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input capacitance	C _{in}	—	—	6	pF	V _{in} = 0 V
Output capacitance	C _{out}	—	—	10	pF	V _{I/O} = 0 V

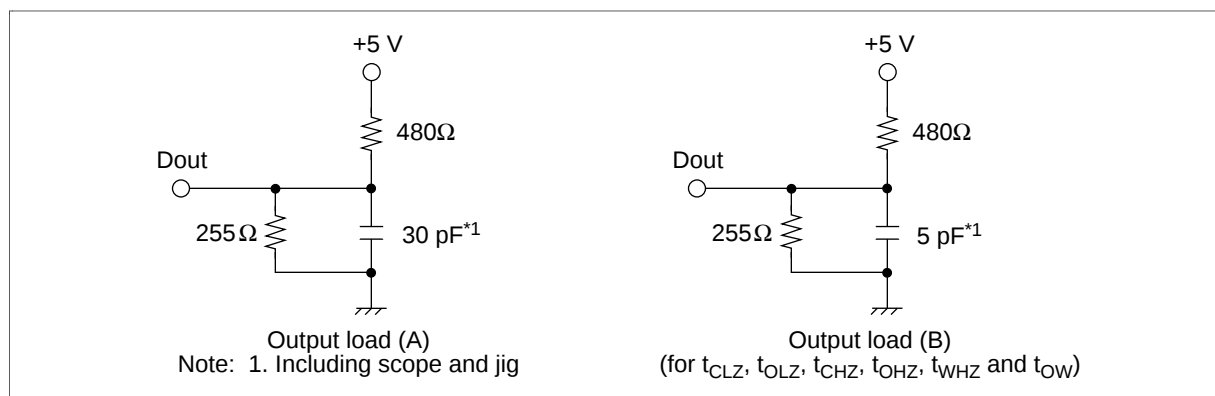
Note: 1. This parameter is sampled and not 100% tested.

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AC Characteristics ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{ V} \pm 10\%$, unless otherwise noted.)

Test Conditions

- Input pulse levels: V_{SS} to 3.0 V
- Input rise and fall time: 4 ns
- Input and Output timing reference levels: 1.5 V
- Output load: See figures

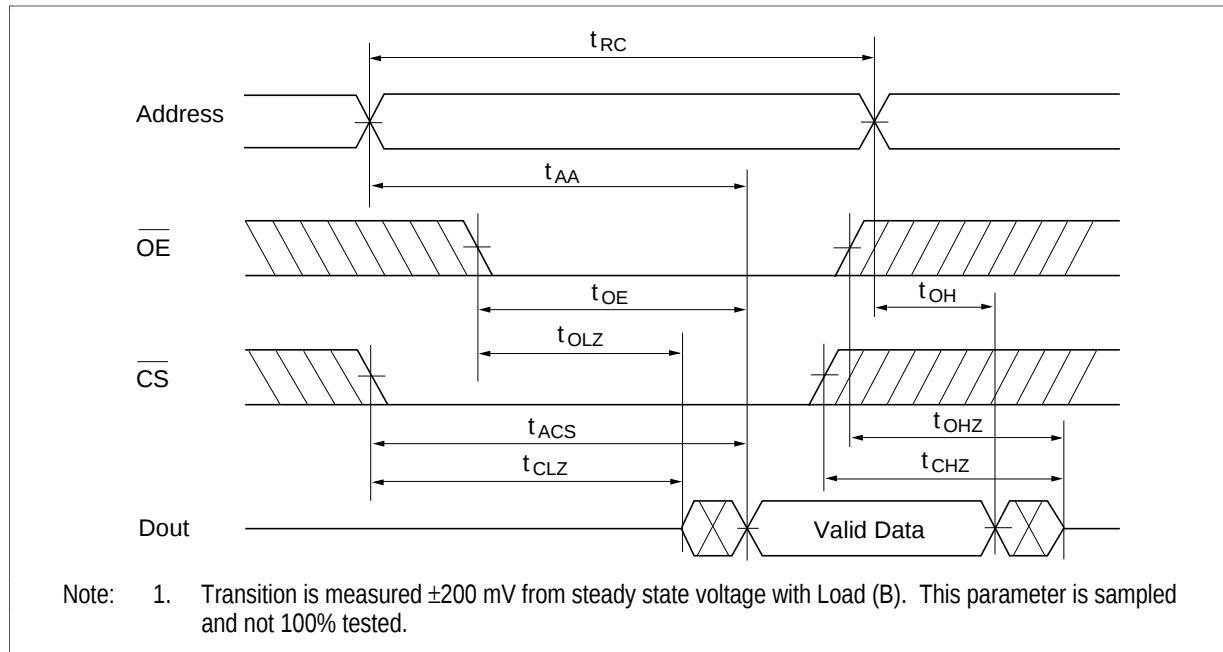


Read Cycle

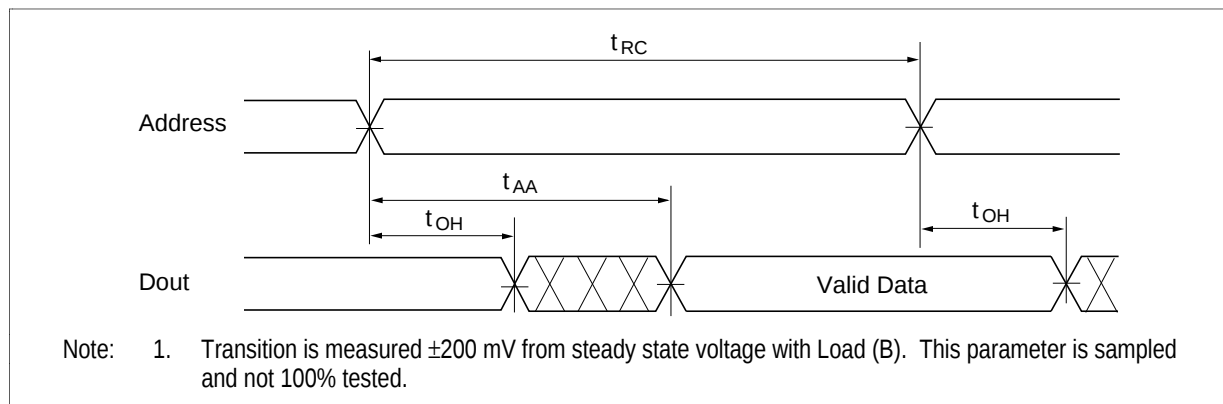
Parameter	Symbol	HM62832UH-15		HM62832UH-20		Unit
		Min	Max	Min	Max	
Read cycle time	t_{RC}	15	—	20	—	ns
Address access time	t_{AA}	—	15	—	20	ns
Chip select access time	t_{ACS}	—	15	—	20	ns
Chip selection to output in low-Z	t_{CLZ}^{*1}	3	—	3	—	ns
Output enable to output valid	t_{OE}	—	8	—	10	ns
Output enable to output in low-Z	t_{OLZ}^{*1}	0	—	0	—	ns
Chip deselection to output in high-Z	t_{CHZ}^{*1}	0	7	0	10	ns
Chip disable to output in high-Z	t_{OHZ}^{*1}	0	7	0	10	ns
Output hold from address change	t_{OH}	3	—	3	—	ns

Note: 1. Transition is measured $\pm 200\text{ mV}$ from steady state voltage with Load (B). This parameter is sampled and not 100% tested.

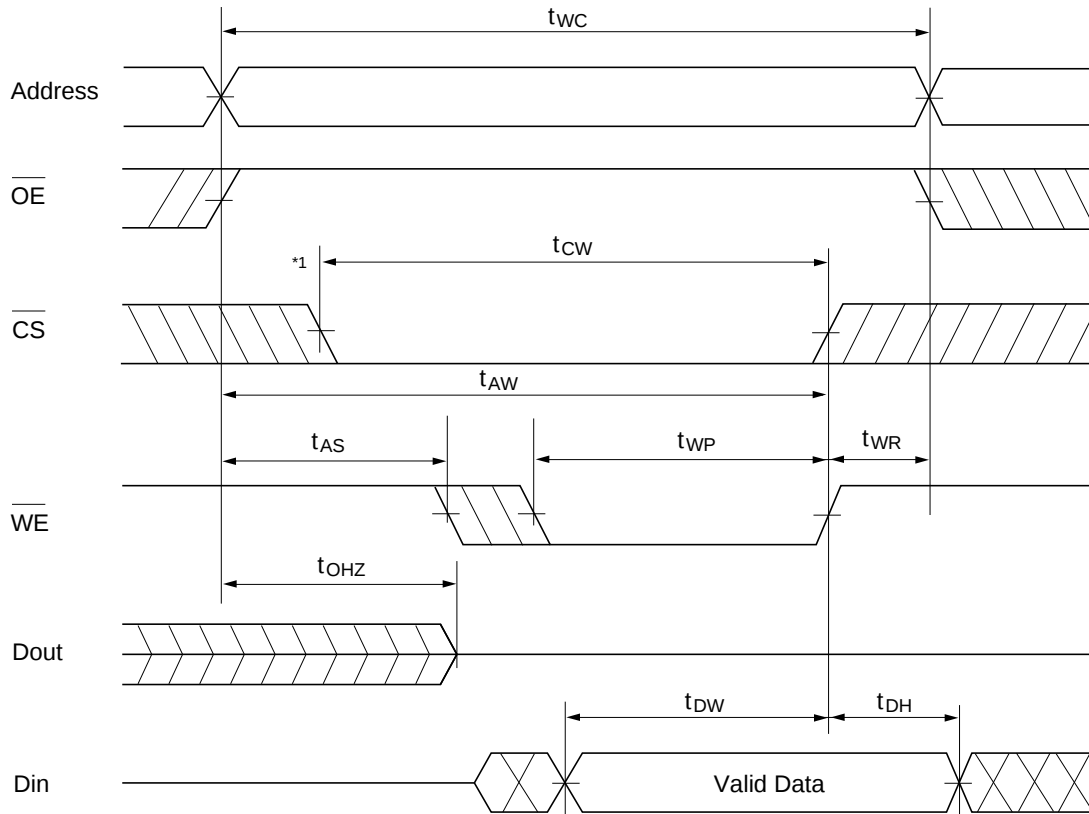
Read Timing Waveform (1)*1 ($\overline{WE} = V_{IH}$)



Read Timing Waveform (2)*1 ($\overline{WE} = V_{IH}$, $\overline{CS} = V_{IL}$, $\overline{OE} = V_{IL}$)



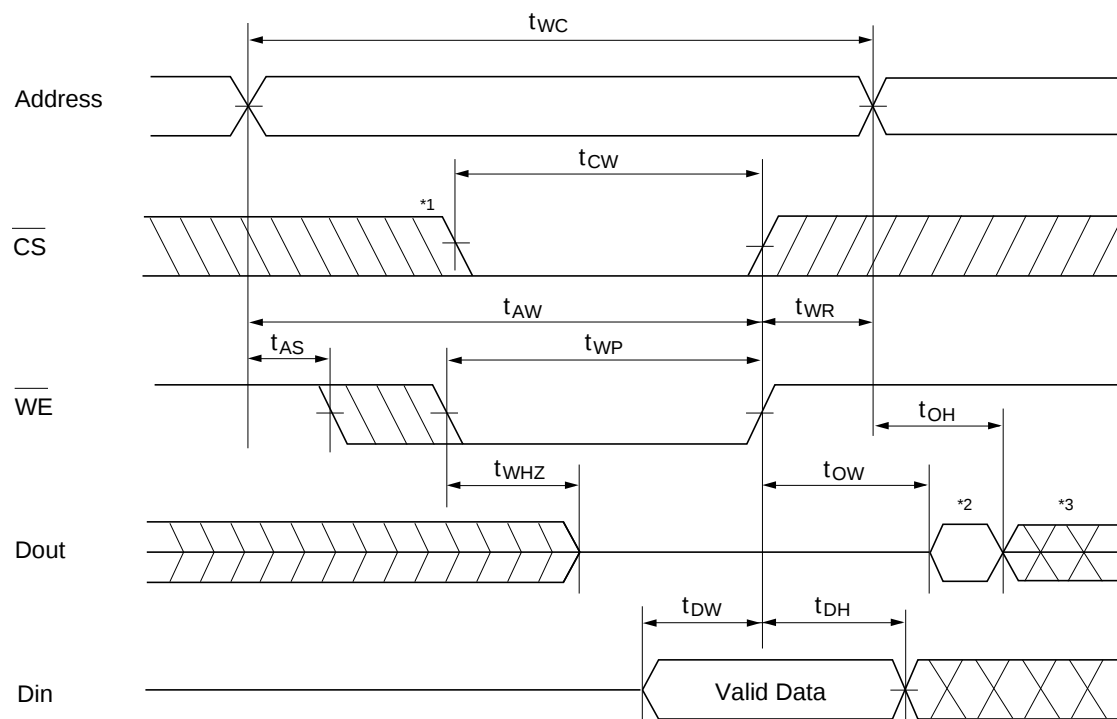
Write Timing Waveform (1)



Note: 1. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the opposite phase to the outputs must not be applied.

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Write Timing Waveform (2) ($\overline{\text{OE}}$ low Fixed)*4



- Notes:
1. If the $\overline{\text{CS}}$ low transition occurs simultaneously with the $\overline{\text{WE}}$ low transitions or after the $\overline{\text{WE}}$ transition, output remain in a high impedance state.
 2. Dout is the same phase of write data of this write cycle.
 3. Dout is the read data of next address.
 4. $\overline{\text{WE}}$ must be high during all address transition except when device is disabled with $\overline{\text{CS}}$.

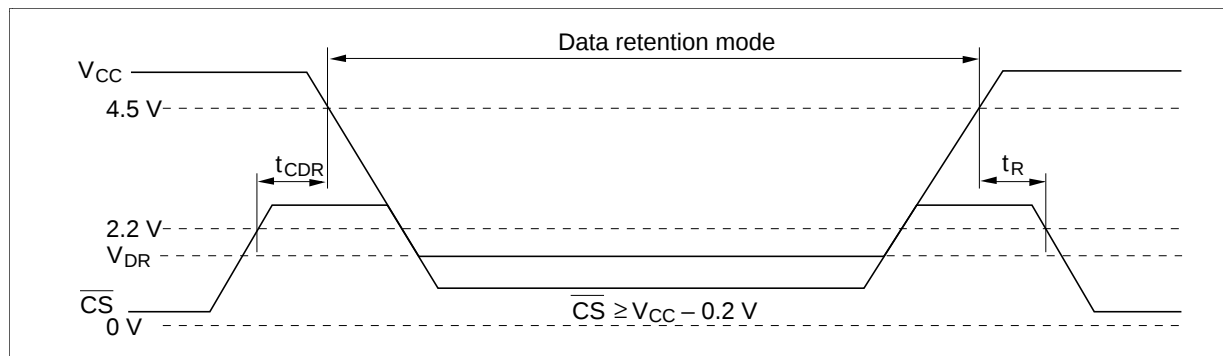
Low V_{CC} Data Retention Characteristics ($T_a = 0$ to $+70^\circ\text{C}$)

This characteristics is guaranteed only for L-version.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2\text{V}$, $V_{in} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} < V_{in} \leq 0.2\text{V}$
Data retention current	I_{CCDR}	—	2	50^{*1}	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	
Operation recovery time	t_R	5	—	—	ms	

Note: 1. $V_{CC} = 3.0\text{V}$

Low V_{CC} Data Retention Timing Waveform

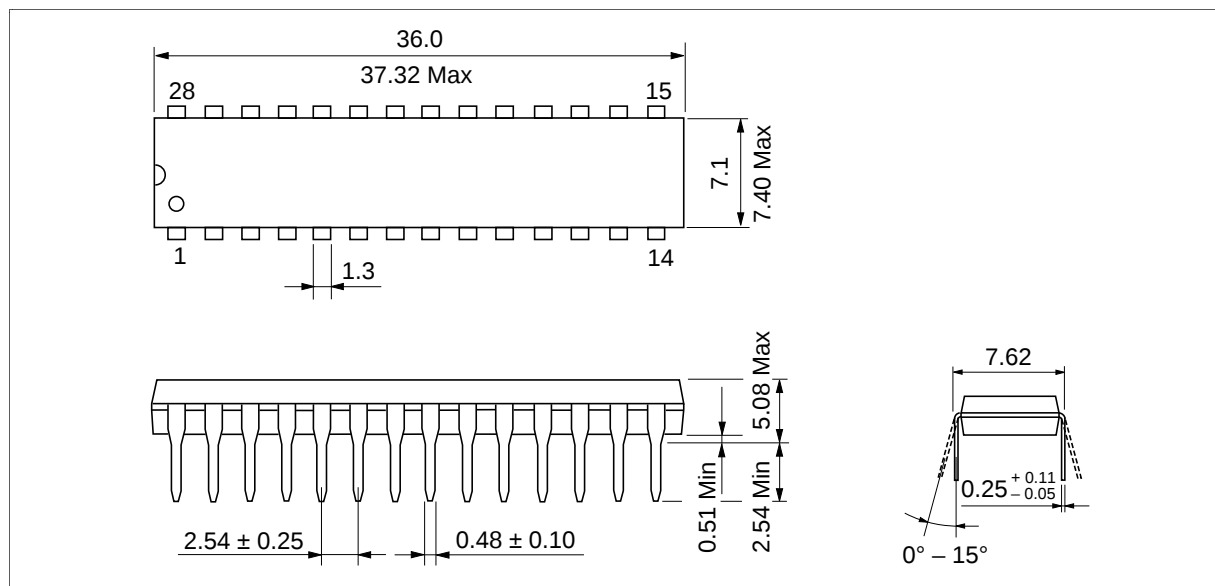


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Package Dimensions

HM62832UHP/UHLP Series (DP-28NA)

Unit: mm



HM62832UHJP/UHLJP Series (CP-28DN)

Unit: mm

