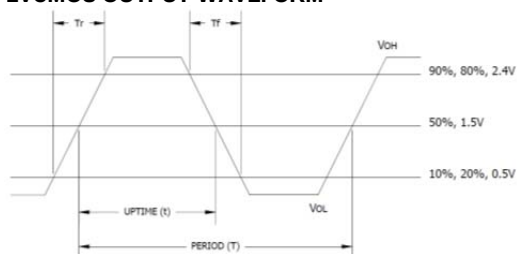
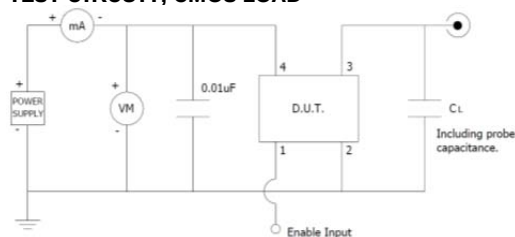


ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	V_{CC}	-	-0.5	-	4.0	V
Storage Temperature	T_{STG}	-	-40	-	+100	°C
Frequency Range	f_O	-	1.0	-	125	MHz
Frequency Stability [See Note 1 and Ordering Information]	$\Delta f/f_O$	-	-	-	20, 25, 50	± ppm
Aging	$\Delta f/f_O$	-	-	-	3	± ppm/yr
Operating Temperature	T_A	-	-20 -40	+25	+70 +85	°C
Supply Voltage	V_{CC}	± 10 %	1.62 2.25 2.52 2.97 4.50	1.8 2.5 2.8 3.3 5.0	1.98 2.75 3.08 3.63 5.50	V
Supply Current	I_{CC}	$C_L = 15pF$ 1.0 MHz to 100 MHz 100.1 MHz to 125 MHz	- - -	- - -	7 12	mA
Model 632M [+18V]						
Model 632N, 632T [+2.5V, +2.8V]					10 20	
Model 632L, 632S [+3.3V, +5.0V]					15 25	
Output Load	C_L		-	-	15	pF
Output Voltage Levels						
Logic '1' Level	V_{OH}	CMOS Load	90% V_{CC}	-	-	V
Logic '0' Level	V_{OL}	CMOS Load	-	-	10% V_{CC}	
Output Current						
Logic '1' Level [M,N,T,L,S]	I_{OH}	$V_{OH} = 90\%V_{CC}$ [1.8V, 2.5/2.8V, 3.3V, 5.0V]	-	-	-2, -4, -8, -16	mA
Logic '0' Level [M,N,T,L,S]	I_{OL}	$V_{OL} = 10\%V_{CC}$ [1.8V, 2.5/2.8V, 3.3V, 5.0V]	-	-	+2, +4, +8, +16	
Output Duty Cycle	SYM	@ 50% Level	45	-	55	%
Rise and Fall Time		@ 10% - 90% Levels, $C_L = 15pF$				
Model 632M [+18V]	T_R, T_F	1.0 MHz to 20 MHz 20.1 MHz to 125 MHz	- -	- -	5 4	ns
Model 632N, 632T [+2.5V, +2.8V]		1.0 MHz to 20 MHz 20.1 MHz to 125 MHz	- -	- -	4 3	
Model 632L, 632S [+3.3V, +5.0V]		1.0 MHz to 20 MHz 20.1 MHz to 125 MHz	- -	- -	3 2	
Start Up Time	T_S	Application of V_{CC}	-	-	2	ms
Enable Function						
Enable Input Voltage	V_{IH}	Pin 1 Logic '1', Output Enabled	0.7* V_{CC}	-	-	V
Disable Input Voltage	V_{IL}	Pin 1 Logic '0', Output Disabled	-	-	0.3* V_{CC}	
Enable Time [M,N,T,L,S]	T_{PLZ}	Pin 1 Logic '1'	-	-	2	ms
Standby Current	I_{ST}	Pin 1 Logic '0', Output Disabled	-	-	15	µA
Period Jitter, pk-pk	pjpk-pk	-	-	-	40	ps
Phase Jitter, RMS	tjrms	Bandwidth 12 kHz - 20 MHz	-	-	1	

Notes:

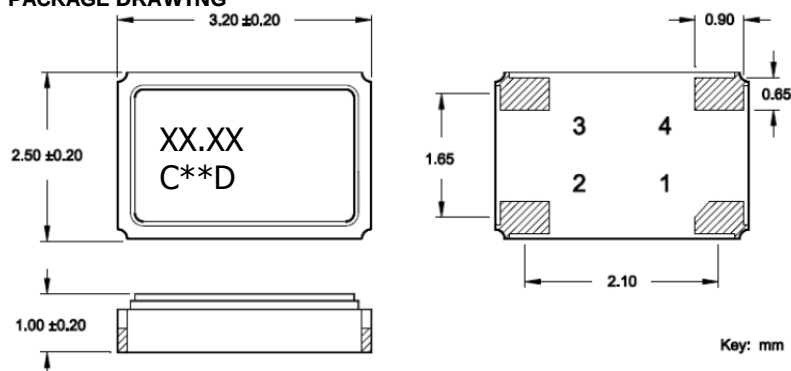
- Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and aging.

LVC MOS OUTPUT WAVEFORM

TEST CIRCUIT, CMOS LOAD

ENABLE TRUTH TABLE

PIN 1	PIN 3
Logic '1'	Output
Open	Output
Logic '0'	High Imp.

MECHANICAL SPECIFICATIONS

PACKAGE DRAWING



MARKING INFORMATION

1. XX.XX – Frequency in MHz.
2. C – CTS and Pin 1 identifier.
3. ** – Manufacturing Site Code.
4. D – Manufacturing Date Code.
[See Table 1 for codes.]
5. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.

NOTES

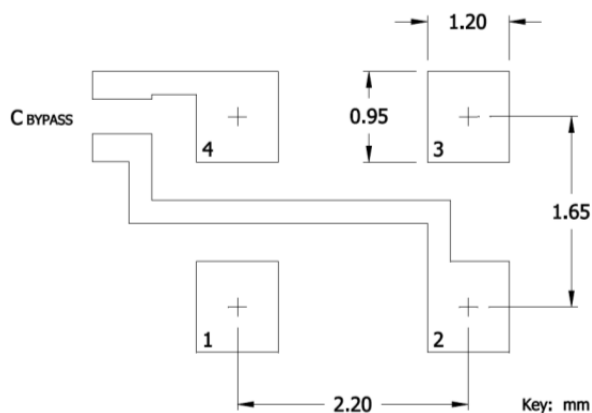
1. Termination pads (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
2. Reflow conditions per JEDEC J-STD-020; 260°C maximum, 20 seconds.
3. MSL = 1.

TABLE I

YEAR \ MONTH					JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z

SUGGESTED SOLDER PAD GEOMETRY

C_{BYPASS} should be ≥ 0.01 uF.



D.U.T. PIN ASSIGNMENTS

PIN	SYMBOL	DESCRIPTION
1	EOH	Enable
2	GND	Circuit & Package Ground
3	Output	RF Output
4	V _{CC}	Supply Voltage