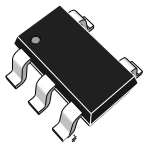
TS391, TS391A

Datasheet

Low-power single voltage comparator



SOT23-5

DFN8 2x2

Maturity status link
TS391, TS391A

Features

- Wide single supply voltage range or dual supplies 2 V to 36 V or ± 1 V to ± 18 V
- Very low supply current (0.2 mA) independent of supply voltage (1 mW / comparator at 5 V)
- Low input bias current: 25 nA typ.
- Low input offset current: ± 5 nA typ.
- Low input offset voltage: ± 2 mV max. for TS391A
- Input common-mode voltage range includes ground
- Low output saturation voltage: 250 mV typ. (I_o = 4 mA)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, CMOS compatible outputs

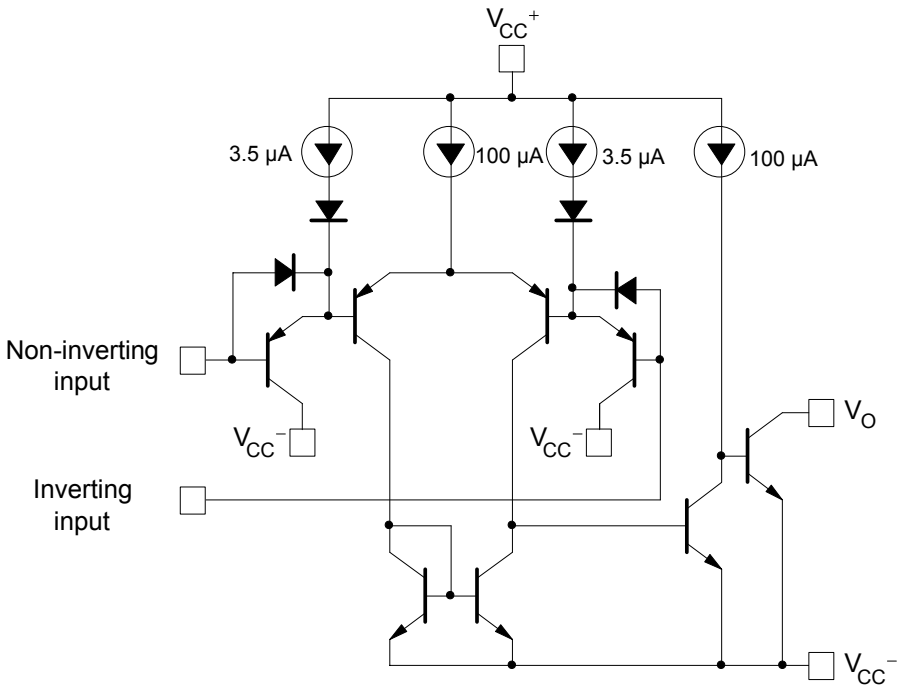
Description

These devices consist of a low-power voltage comparator designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic where the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

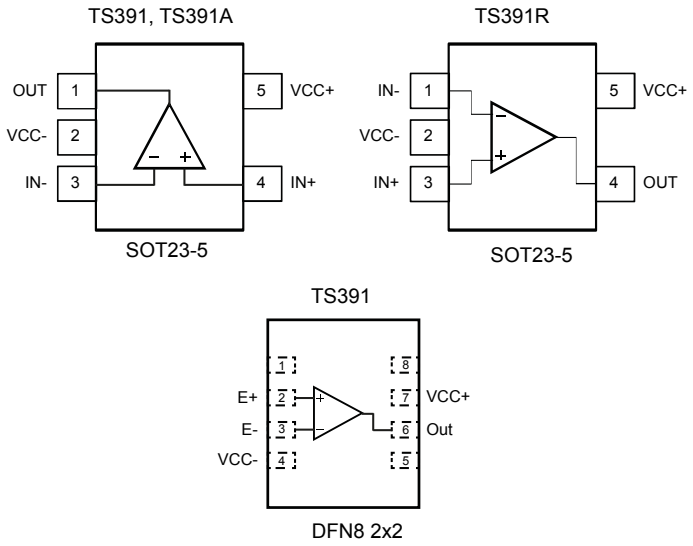
1 Schematic diagram

Figure 1. **Schematic diagram**



2 Package pin connections

Figure 2. Pin connections (top view)



3 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings (AMR)

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		±18 or 36	V
V_{id}	Differential input voltage		±36	
V_i	Input voltage		-0.3 to 36	
V_o	Output voltage (1)		36	
	Output short-circuit to ground (2)		Infinite	
T_j	Maximum junction temperature		150	°C
T_{stg}	Storage temperature range		-65 to 150	
R_{thja}	Thermal resistance junction to ambient (3)	SOT23-5	250	°C/W
		DFN8 2x2	57	
ESD	Human body model (HBM) (4)		1500	V
	Machine model (MM) (5)		100	
	Charged device model (CDM) (6)		1000	

1. *Output voltage can be set up to 36 V even if the V_{CC} is lower.*
2. *Short-circuits from the output to V_{CC}^+ can cause excessive heating and potential destruction. The maximum output current is approximately 20 mA independent of the magnitude of V_{CC}^+.*
3. *Short-circuits can cause excessive heating. These values are typical.*
4. *Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.*
5. *Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.*
6. *Charged device model: all pins and package are charged together to the specified voltage and then discharged directly to ground through only one pin. This is done for all pins.*

Table 2. Operating conditions

Symbol	Parameter		Value	Unit
V_{CC}	Supply voltage		2 to 36 or ±1 to ±18	V
V_{icm}	Input common mode voltage range (1)	T_{amb} = 25 °C	0 to (V_{CC}^+) - 1.5	
		$T_{min} \leq T_{amb} \leq T_{max}$	0 to (V_{CC}^+) - 2	
T_{oper}	Operating free-air temperature range		-40 to 125	°C

1. *The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3 V. The upper end of the common-mode voltage range is (V_{CC}^+) – 1.5 V, but either or both inputs can go to 30 V without damage. As long as one input stays within the Vicm operating range, the comparator will provide a proper output state. Even if the second pin is within 0 V to 30 V.*

4 Electrical characteristics

Table 3. V_{CC}^+ = 5 V, V_{CC}^- = 0 V, T_{amb} = 25 °C (unless otherwise specified)

Symbol	Parameter and test conditions		Min.	Typ.	Max.	Unit
V_{io}	TS391	Input offset voltage		1	5	mV
		Input offset voltage, $T_{min} \le T_{amb} \le T_{max}$			9	
	TS391A	Input offset voltage (1)		1	1.5	
		Input offset voltage, $T_{min} \le T_{amb} \le T_{max}$			2	
I_{ib}	TS391	Input bias current		25	250	nA
		Input bias current, $T_{min} \le T_{amb} \le T_{max}$			400	
	TS391A	Input bias current (2)		25	150	
		Input bias current, $T_{min} \le T_{amb} \le T_{max}$			250	
I_{io}	Input offset current			5	50	
	Input offset current, $T_{min} \le T_{amb} \le T_{max}$				150	
A_{VD}	Large signal voltage gain, (V_{CC+}) = 15 V, R_L=15 kΩ, V_o = 1 to 11 V		50	200		V/mV
I_{CC}	Supply current (V_{CC}^+) = 5 V, no load			0.2	0.5	mA
	Supply current (V_{CC}^+) = 30 V, no load			0.5	1.25	
V_{id}	Differential input voltage (3)				V_{CC+}	V
I_{sink}	Output sink current, V_{id} = - 1 V, V_o = 1.5 V		6	16		mA
V_{OL}	Low level output voltage, V_{id} = 1 V, V_{CC}^+ = 30 V, T = T_{amb}			250	400	mV
	Low level output voltage, V_{id} = 1 V, V_{CC}^+ = 30 V, $T_{min} \le T_{amb} \le T_{max}$				700	
I_{OH}	High level output current, V_{id} = 1 V, V_{CC}^+ = V_o = 30 V, T = T_{amb}			0.1		nA
	High level output current, V_{id} = 1 V, V_{CC}^+ = V_o = 30 V, $T_{min} \le T_{amb} \le T_{max}$				1	µA
t_{re}	Small signal response time, R_L = 5.1 kΩ to (V_{CC+}) (4)			1.3		µs
t_{rel}	Large signal response time, V_i = TTL, V_{ref} = 1.4 V, R_L = 5.1 kΩ to V_{CC}^+			300		ns

1. *At the output switch point, $V_o \approx$ 1.4 V, R_S = 0 Ω with (V_{CC}^+) from 5 V to 30 V, and over the full input common-mode range (0 V to (V_{CC}^+) – 1.5 V).*
2. *The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output, so there is no load charge on the reference of input lines.*
3. *Positive excursions of the input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than –0.3 V (or 0.3 V below the negative power supply, if used)*
4. *The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals, 300 ns can be obtained.*

5 Electrical characteristic curves

Figure 3. Supply current vs. supply voltage

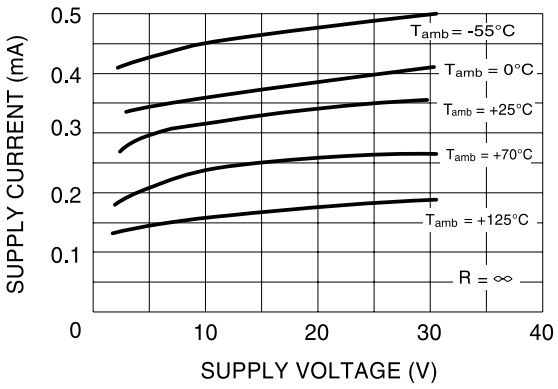


Figure 4. Response time for various input overdrives - negative transition

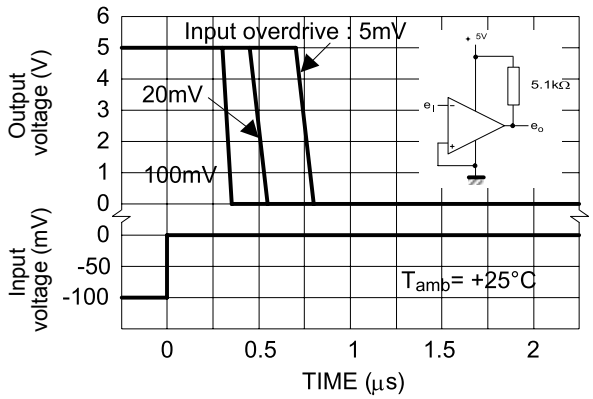


Figure 5. Input current vs. supply voltage

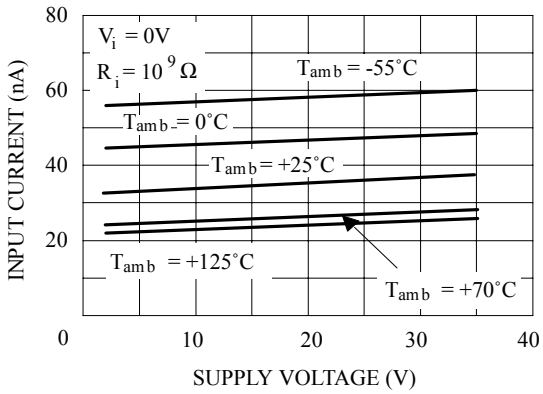


Figure 6. Response time for various input overdrives - positive transition

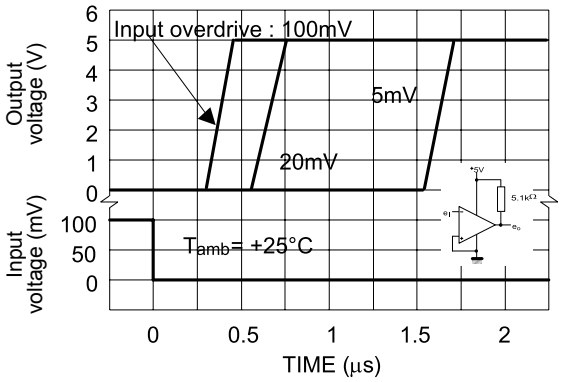
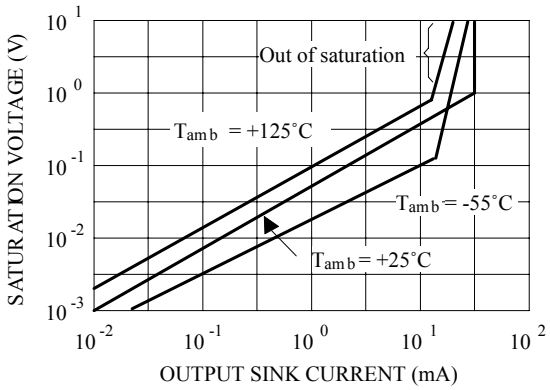


Figure 7. Output saturation voltage vs. output current



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 SOT23-5 package information

Figure 8. **SOT23-5 package outline**

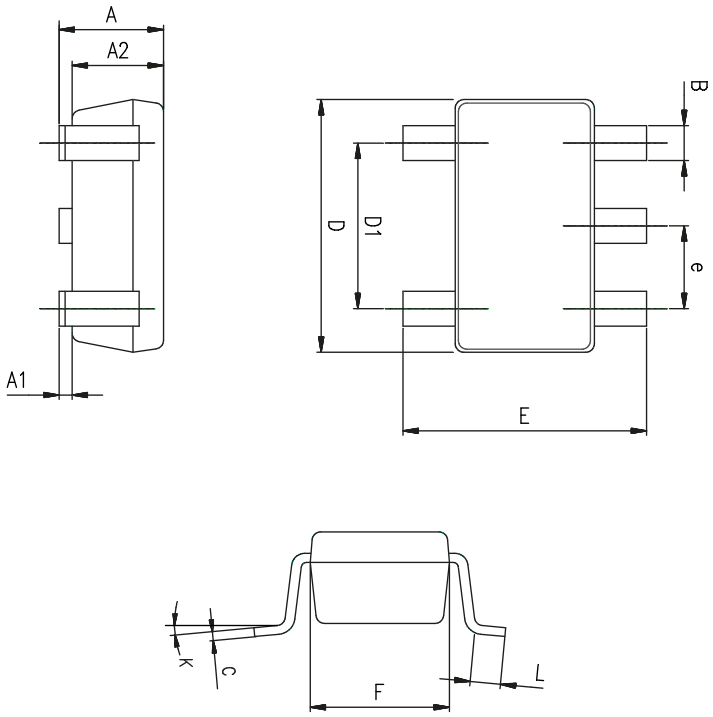


Table 4. **SOT23-5 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.014	0.016	0.020
C	0.09	0.15	0.20	0.004	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.014	0.024
K	0 degrees		10 degrees	0 degrees		10 degrees

6.2 DFN8 2 x 2 package information

Figure 9. **DFN8 2 x 2 package outline**

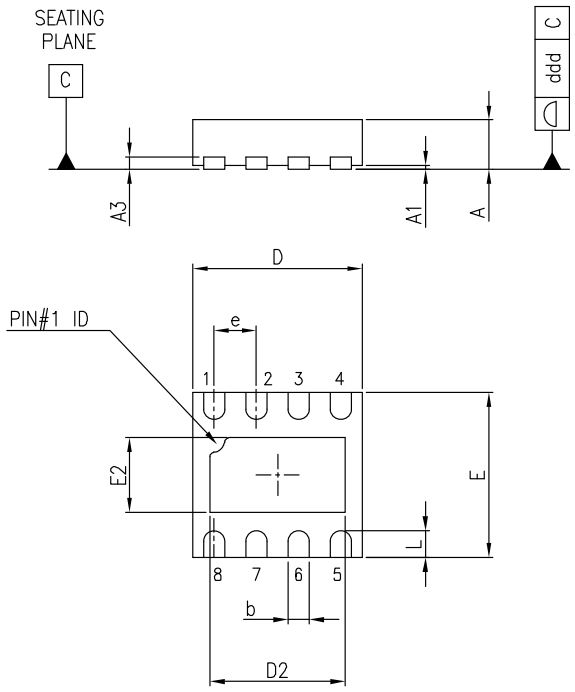
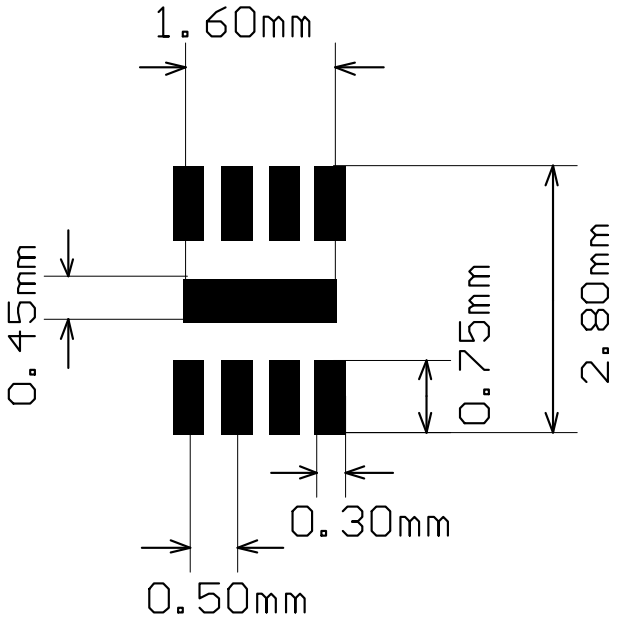


Table 5. **DFN8 2 x 2 mechanical data**

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.51	0.55	0.60	0.020	0.022	0.024
A1			0.05			0.002
A3		0.15			0.006	
b	0.18	0.25	0.30	0.007	0.010	0.012
D	1.85	2.00	2.15	0.073	0.079	0.085
D2	1.45	1.60	1.70	0.057	0.063	0.067
E	1.85	2.00	2.15	0.073	0.079	0.085
E2	0.75	0.90	1.00	0.030	0.035	0.039
e		0.50			0.020	
L	0.225	0.325	0.425	0.009	0.013	0.017
ddd			0.08			0.003

Figure 10. **DFN8 2 x 2 recommended footprint**



7 Ordering information

Table 6. Order codes

Part number	Temperature range	Package	Packaging	Marking
TS391ILT	-40 °C to 125 °C	SOT23-5	Tape and reel	K511
TS391AILT				K512
TS391IYLT (1)		SOT23-5 (automotive grade)		K510
TS391RILT		SOT23-5		K509
TS391RIYLT (1)		SOT23-5 (automotive grade)		K535
TS391IQ2T		DFN8 2x2		K5D

1. *Qualification and characterization according to AEC Q100 and Q003 or equivalent, advanced screening according to AEC Q001 & Q002 or equivalent.*

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
22-Sep-2004	1	Initial release.
06-Jan-2006	2	PPAP reference inserted in the document.
21-Nov-2007	3	Added values for R_{thja}, R_{thjc} and ESD in Table 1: Absolute maximum ratings (AMR). Added footnote for automotive grade order code in order codes table. Updated format.
21-Jan-2010	4	Corrected ESD tolerance values for human body model and machine model in Table 1: Absolute maximum ratings (AMR) and added ESD tolerance value for charged device model. Updated note 1 in Table 6: Order codes.
23-May-2011	5	Added TS391R pinout on page 1. Modified V_{CC} range in Table 2: Operating conditions. Added TS391RILT order code in Table 6: Order codes.
02-Mar-2012	6	Added DFN8 package information and changed SOT23-5L package drawing in Chapter 4.
06-Nov-2015	7	Removed letter "L" and "plastic package" from SOT23-5 silhouette and letters "Q2" and "plastic micropackage" from DFN8 2x2 silhouette. Standardized name of the DFN8 package to: "DFN8 2x2" throughout datasheet. Table 1: "Absolute maximum ratings (AMR)": added parameter V_o. Table 4: "SOT23-5 mechanical data": updated “K” parameter. Table 5: "DFN8 2 x 2 mechanical data": updated “L” parameter.
20-Mar-2017	8	Added new part number TS391A. Features: updated low input offset voltage for TS391A. Table 3: added Vio and Iib information for TS391A. Table 6: "Order codes": added new order code TS391AILT.
06-Mar-2020	9	Table 6 added new order code TS391RIYLT.
14-Jan-2021	10	Updated Figure 3. Pin connections (top view).
04-Sep-2023	11	Updated V_{OL} and I_{OH} relation of parameters in Table 3.

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