P4C1024
HIGH SPEED 128K x 8
DUAL CHIP ENABLE
CMOS STATIC RAM

FEATURES

- **High Speed (Equal Access and Cycle Times)**
  - **— 15/20/25/35 ns (Commercial/Industrial)**
  - **— 20/25/35/45/55/70/85/100/120 ns (Military)**
- **Single 5 Volts ±10% Power Supply**
- **Easy Memory Expansion Using $\overline{CE}_1$, CE_2 and $\overline{OE}$ Inputs**
- **Common Data I/O**
- **Three-State Outputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Advanced CMOS Technology**
- **Fast t_{OE}**
- **Automatic Power Down**
- **Packages**
  - **—32-Pin 300 mil DIP and SOJ**
  - **—32-Pin 400 mil SOJ**
  - **—32-Pin 600 mil Ceramic DIP**
  - **—32-Pin 400 mil Ceramic DIP**
  - **—32-Pin Solder Seal Flatpack**
  - **—32-Pin LCC (450 x 550 mil)**
  - **—32-Pin LCC (400 x 820 mil) [Two-Sided]**
  - **—32-Pin Ceramic SOJ**

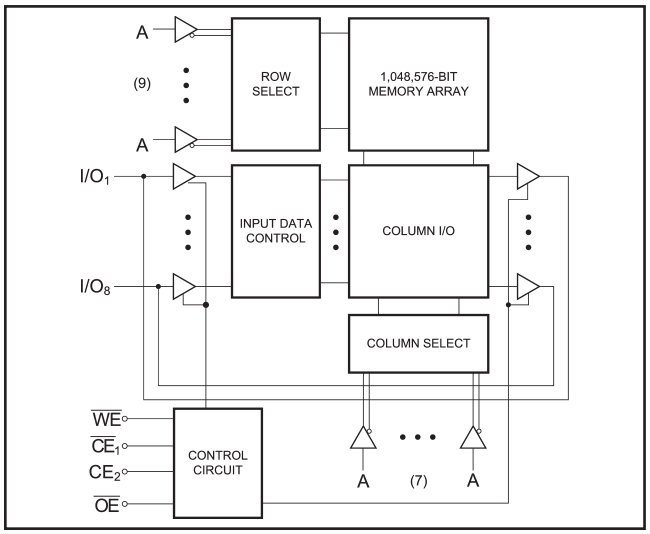
DESCRIPTION

The P4C1024 is a 1,048,576-bit high-speed CMOS static RAM organized as 128Kx8. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5V±10% tolerance power supply.

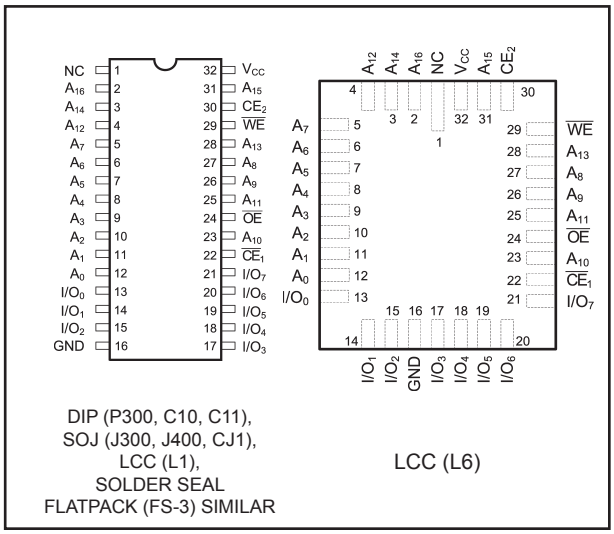
Access times of 15 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level. The P4C1024 is a member of a family of PACE RAM™ products offering fast access times.

The P4C1024 device provides asynchronous operations with matching access and cycle times. Memory locations are specified on address pins A_0 to A_{16}. Reading is accomplished by device selection ($\overline{CE}_1$ low and CE_2 high) and output enabling ($\overline{OE}$) while write enable ($\overline{WE}$) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{CE}_1$ or $\overline{OE}$ is HIGH or $\overline{WE}$ or CE_2 is LOW.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



DIP (P300, C10, C11),
SOJ (J300, J400, CJ1),
LCC (L1),
SOLDER SEAL
FLATPACK (FS-3) SIMILAR

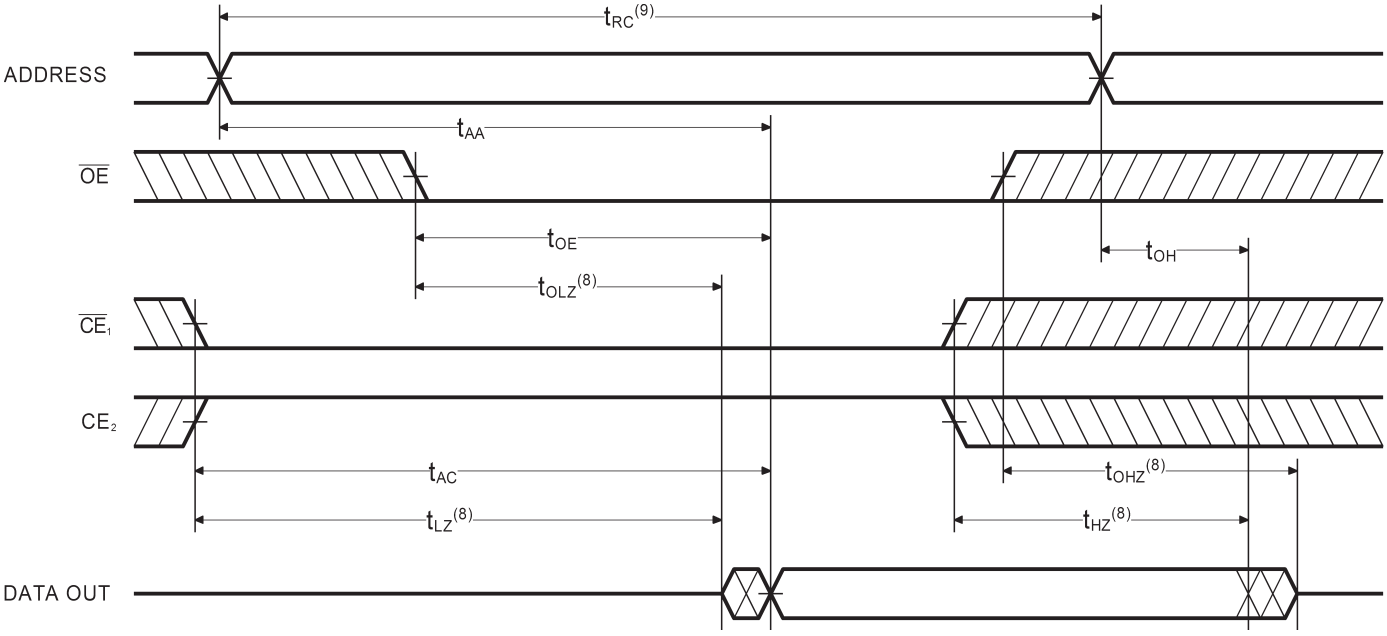
LCC (L6)

AC ELECTRICAL CHARACTERISTICS—READ CYCLE

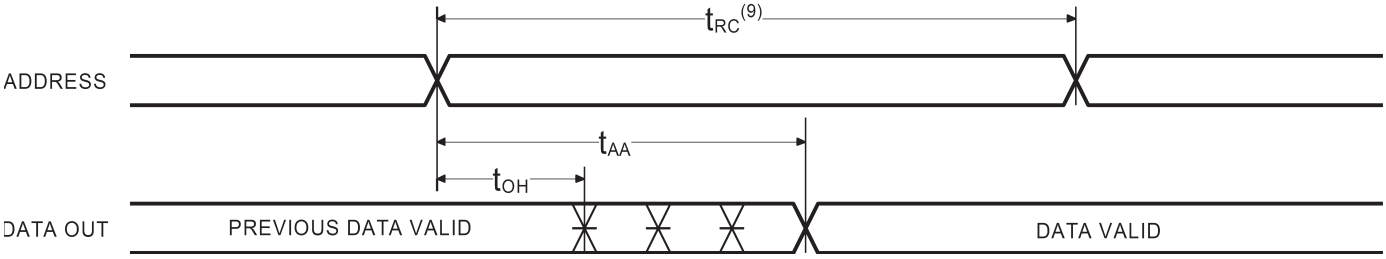
(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Sym	Parameter	-15		-20		-25		-35		-45		-55		-70		-85		-100		-120		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{RC}	Read Cycle Time	15		20		25		35		45		55		70		85		100		120		ns
t_{AA}	Address Access Time		15		20		25		35		45		55		70		85		100		120	ns
t_{AC}	Chip Enable Access Time		15		20		25		35		45		55		70		85		100		120	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		3		3		3		3		3		3		ns
t_{LZ}	Chip Enable to Output in Low Z	3		3		3		3		3		3		3		3		3		3		ns
t_{HZ}	Chip Disable to Output in High Z		8		9		11		15		20		25		30		35		40		50	ns
t_{OE}	Output Enable Low to Data Valid		7		9		11		15		20		25		30		35		40		50	ns
t_{OLZ}	Output Enable Low to Low Z	0		0		0		0		0		0		0		0		0		0		ns
t_{OHZ}	Output Enable High to High Z		7		9		11		15		20		25		30		35		40		50	ns
t_{PU}	Chip Enable to Power Up Time	0		0		0		0		0		0		0		0		0		0		ns
t_{PD}	Chip Disable to Power Down Time		12		20		20		20		25		30		35		40		45		50	ns

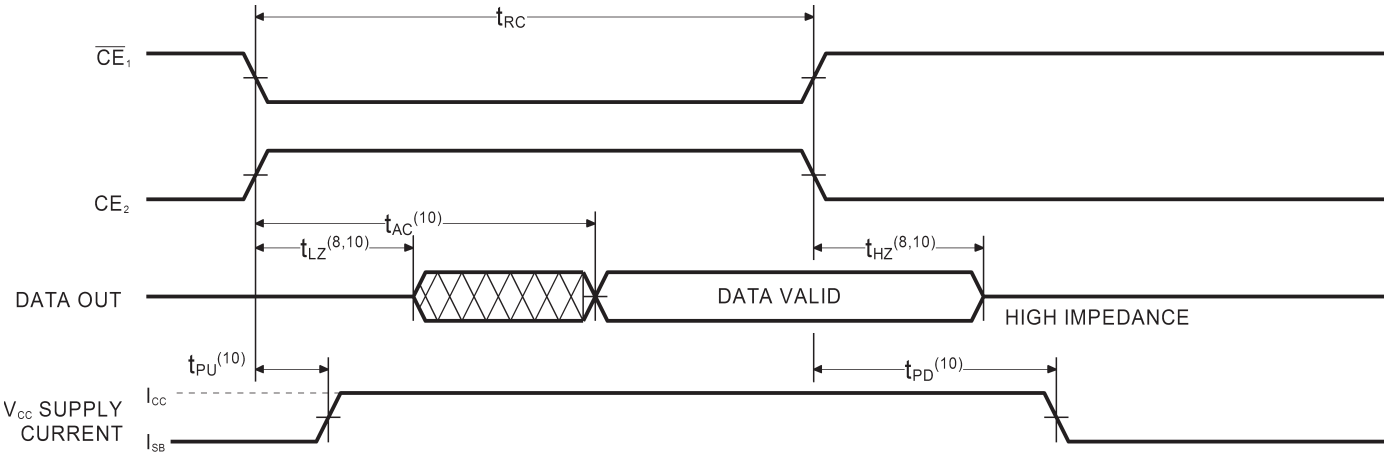
TIMING WAVEFORM OF READ CYCLE NO. 1 ($\overline{OE}$ CONTROLLED)[5]



TIMING WAVEFORM OF READ CYCLE NO. 2 (ADDRESS CONTROLLED)[5,6]



TIMING WAVEFORM OF READ CYCLE NO. 3 ($\overline{CE_1}$, CE_2 CONTROLLED)[5,7,10]



Notes:

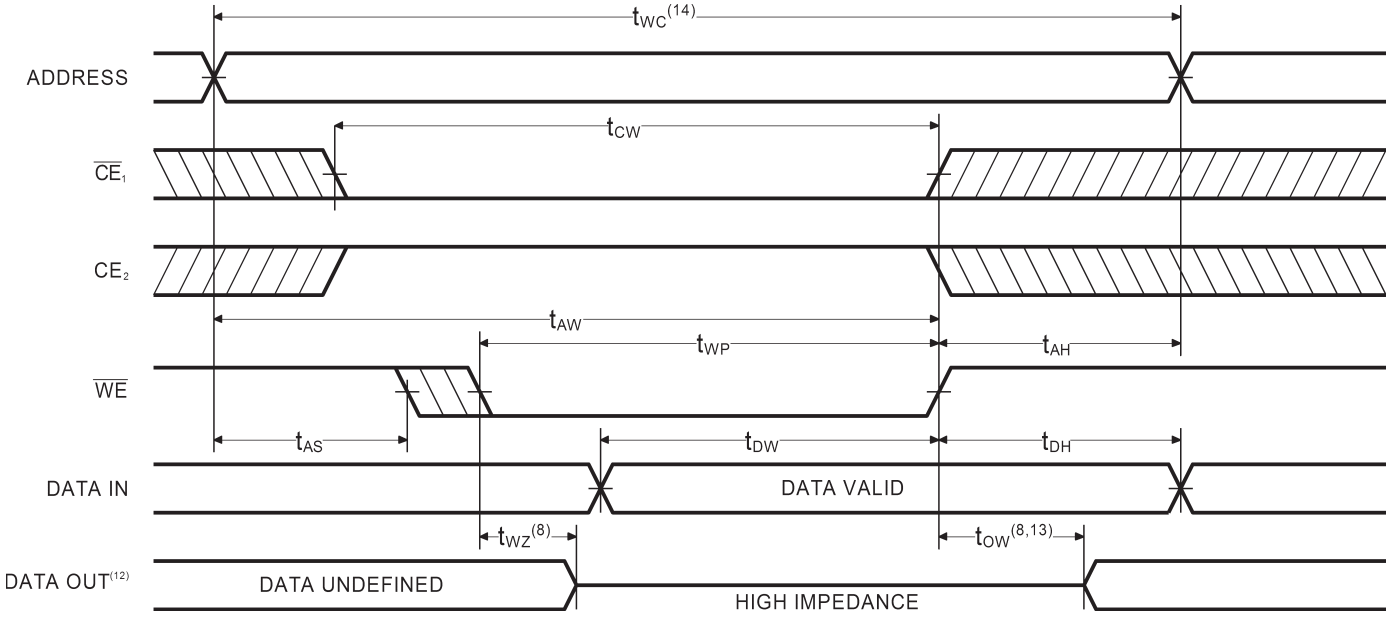
5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE_1}$ is LOW, CE_2 is HIGH and $\overline{OE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
9. READ Cycle Time is measured from the last valid address to the first transitioning address.
10. Transitions caused by a chip enable control have similar delays irrespective of whether $\overline{CE_1}$ or CE_2 causes them.

AC CHARACTERISTICS—WRITE CYCLE

(V_{CC} = 5V ± 10%, All Temperature Ranges)[2]

Symbol	Parameter	-15		-20		-25		-35		-45		-55		-70		-85		-100		-120		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{WC}	Write Cycle Time	15		20		25		35		45		55		70		85		100		120		ns
t_{CW}	Chip Enable Time to End of Write	12		15		18		22		30		35		45		50		60		75		ns
t_{AW}	Address Valid to End of Write	12		15		20		25		35		45		60		70		85		100		ns
t_{AS}	Address Set-up Time	0		0		0		0		0		0		0		0		0		0		ns
t_{WP}	Write Pulse Width	12		15		18		22		25		30		40		45		55		70		ns
t_{AH}	Address Hold Time	0		0		0		0		0		0		0		0		0		0		ns
t_{DW}	Data Valid to End of Write	7		8		10		15		20		25		30		35		45		60		ns
t_{DH}	Date Hold Time	0		0		0		0		0		0		0		0		0		0		ns
t_{WZ}	Write Enable to Output in High Z		8		10		11		15		18		20		25		30		40		50	ns
t_{OW}	Output Active from End of Write	3		3		3		3		3		3		3		3		3		3		ns

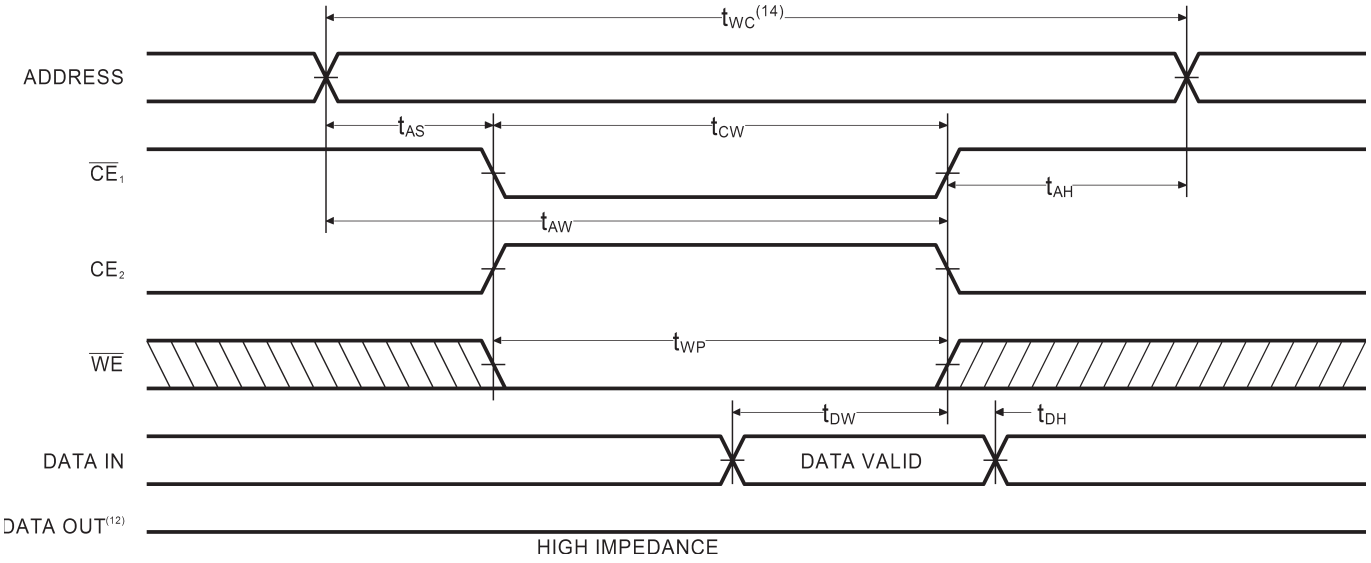
TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED)[11]



Notes:

11. $\overline{CE_1}$ and $\overline{WE}$ must be LOW, and CE_2 HIGH for WRITE cycle.
12. $\overline{OE}$ is LOW for this WRITE cycle to show t_{WZ} and t_{OW}.
13. If $\overline{CE_1}$ goes HIGH, or CE_2 goes LOW, simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedance state.
14. Write Cycle Time is measured from the last valid address to the first transitioning address.

TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CE}$ CONTROLLED)[11]



AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise and Fall Times	3ns
Input Timing Reference Level	1.5V
Output Timing Reference Level	1.5V
Output Load	See Fig. 1 and 2

TRUTH TABLE

Mode	$\overline{CE}_1$	CE_2	$\overline{OE}$	$\overline{WE}$	$\overline{I/O}$	Power
Standby	H	X	X	X	High Z	Standby
Standby	X	L	X	X	High Z	Standby
D_{OUT} Disabled	L	H	H	H	High Z	Active
Read	L	H	L	H	D_{OUT}	Active
Write	L	H	X	L	High Z	Active

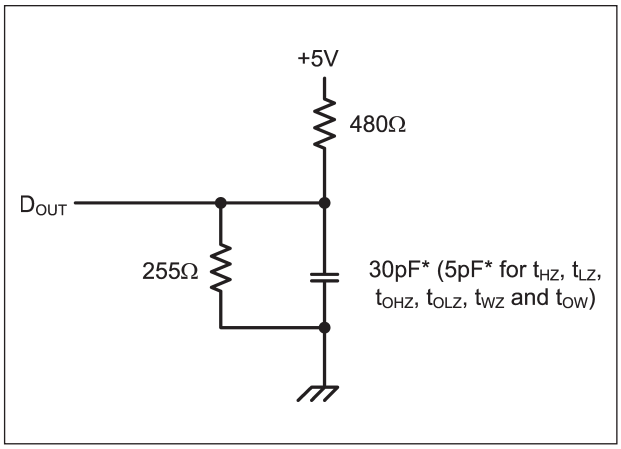


Figure 1. Output Load

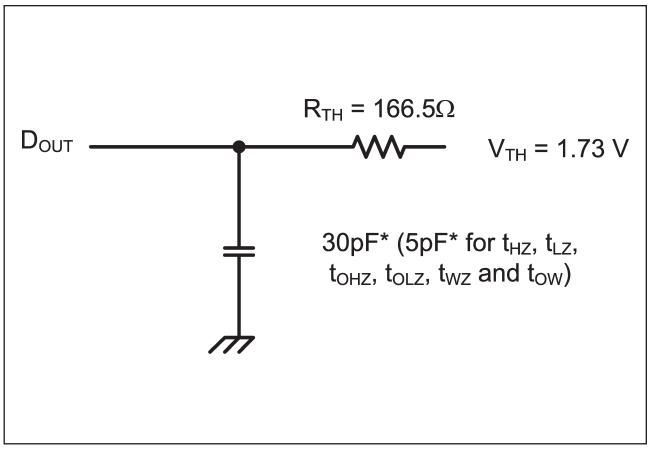


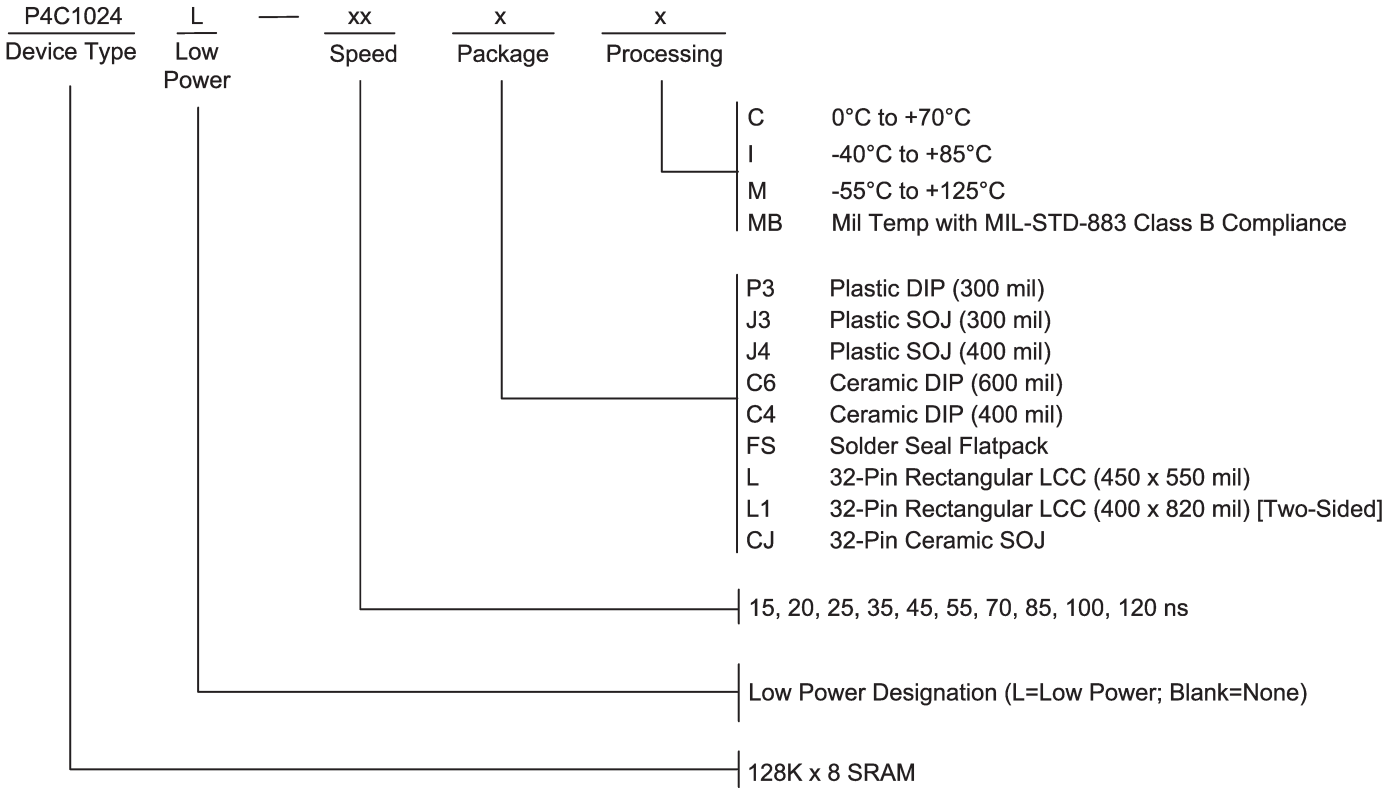
Figure 2. Thevenin Equivalent

* including scope and test fixture.

Note:
Because of the ultra-high speed of the P4C1024, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the V_{CC} and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between V_{CC} and ground.

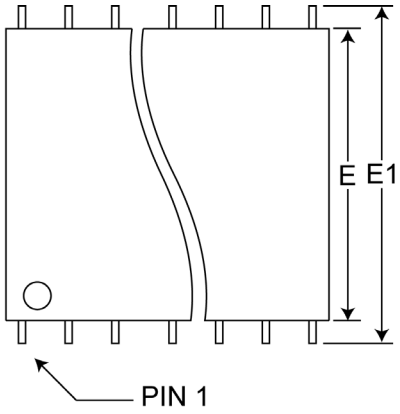
To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.73V (Thevenin Voltage) at the comparator input, and a 116Ω resistor must be used in series with D_{OUT} to match 166Ω (Thevenin Resistance).

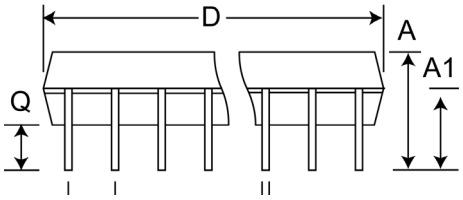
ORDERING INFORMATION

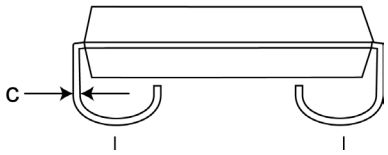


SOJ SMALL OUTLINE IC PACKAGE (300 mil)

Pkg #	J300	
# Pins	32 (300 mil)	
Symbol	**Min**	**Max**
A	0.128	0.148
A1	0.082	-
b	0.016	0.020
C	0.007	0.010
D	0.820	0.830
e	0.050 BSC	
E	0.335 BSC	
E1	0.295	0.305
E2	0.267 BSC	
Q	0.025	-

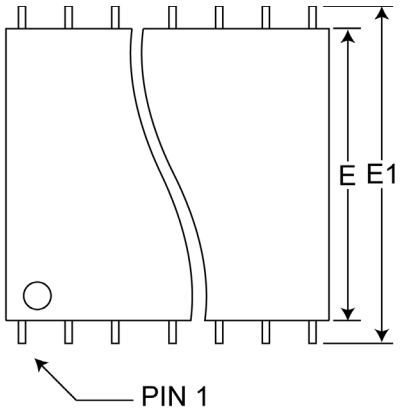


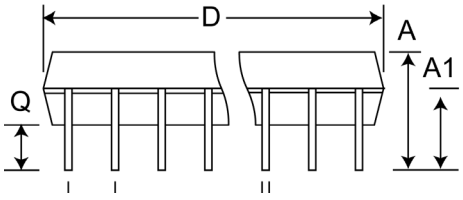


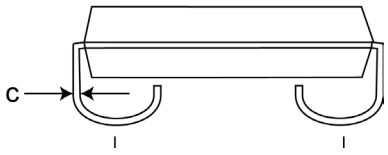


SOJ SMALL OUTLINE IC PACKAGE (400 mil)

Pkg #	J400	
# Pins	32 (400 mil)	
Symbol	**Min**	**Max**
A	0.128	0.148
A1	0.082	-
b	0.015	0.020
C	0.007	0.013
D	0.820	0.830
e	0.050 BSC	
E	0.435	0.445
E1	0.395	0.405
E2	0.370 BSC	
Q	0.025	-

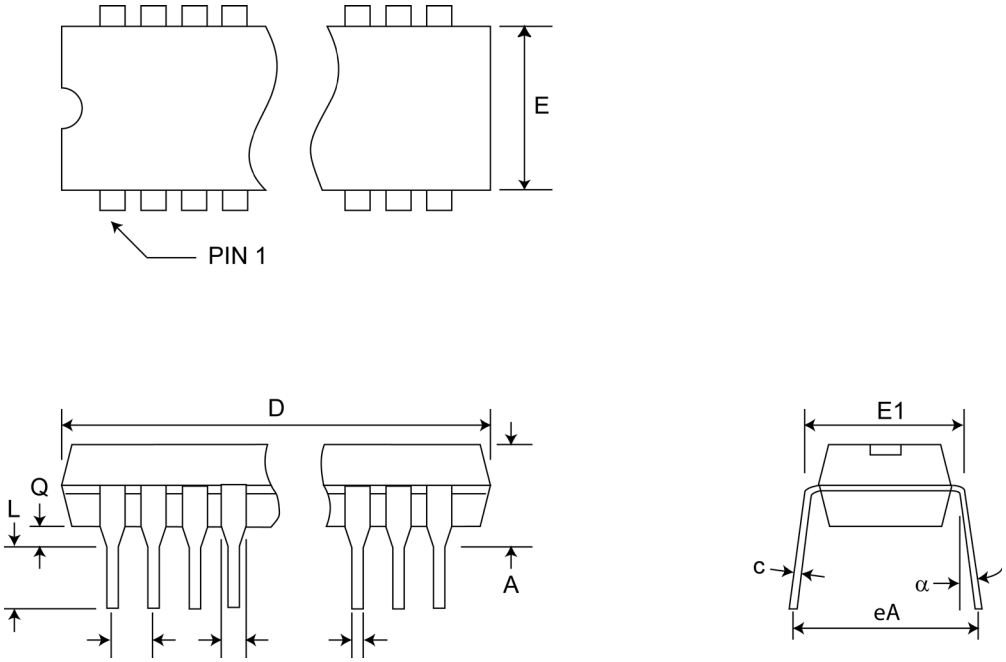






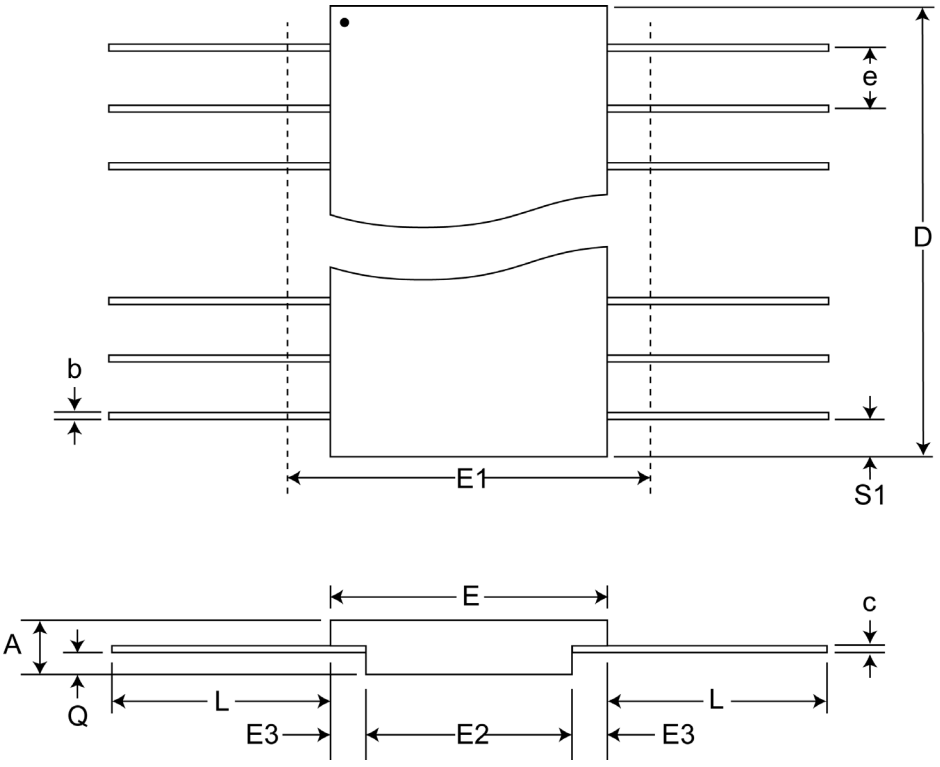
Pkg #	P300	
# Pins	32 (300 mil)	
Symbol	**Min**	**Max**
A	-	0.200
A1	0.015	-
b	0.014	0.022
b2	0.048	0.054
C	0.008	0.014
D	1.580	1.620
E1	0.270	0.300
E	0.300	0.310
e	0.100 BSC	
eB	0.320	0.390
L	0.120	0.140
α	0°	15°

PLASTIC DUAL IN-LINE PACKAGE



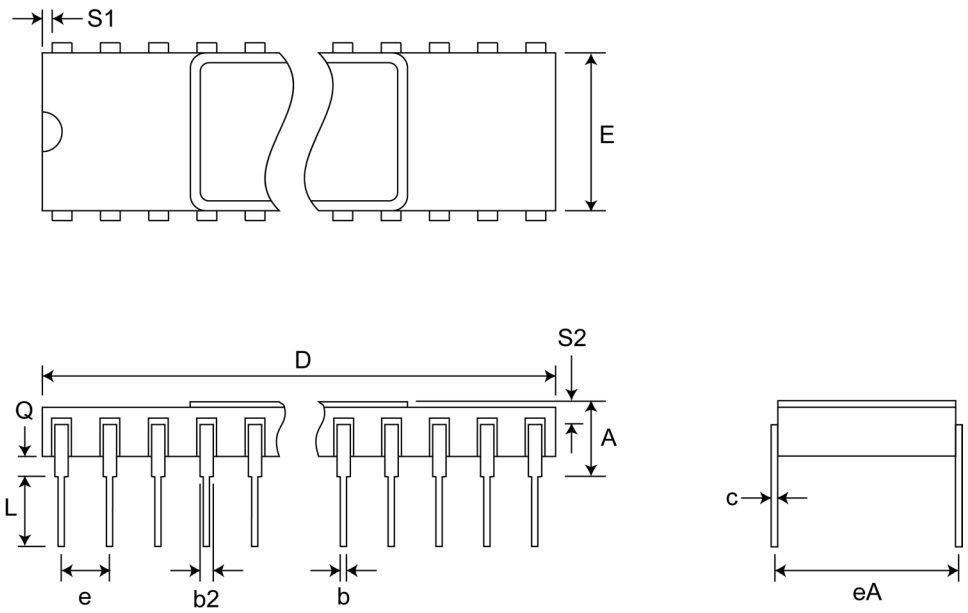
Pkg #	FS-3	
# Pins	32	
Symbol	**Min**	**Max**
A	0.097	0.125
b	0.015	0.019
c	0.003	0.009
D	-	0.830
E	0.400	0.420
E1	-	0.450
E2	0.180	-
E3	0.030	-
e	0.050 BSC	
L	0.250	0.370
Q	0.020	0.045
S	-	0.045
S1	0.000	-
M	-	0.002
N	32	

SOLDER SEAL FLAT PACKAGE



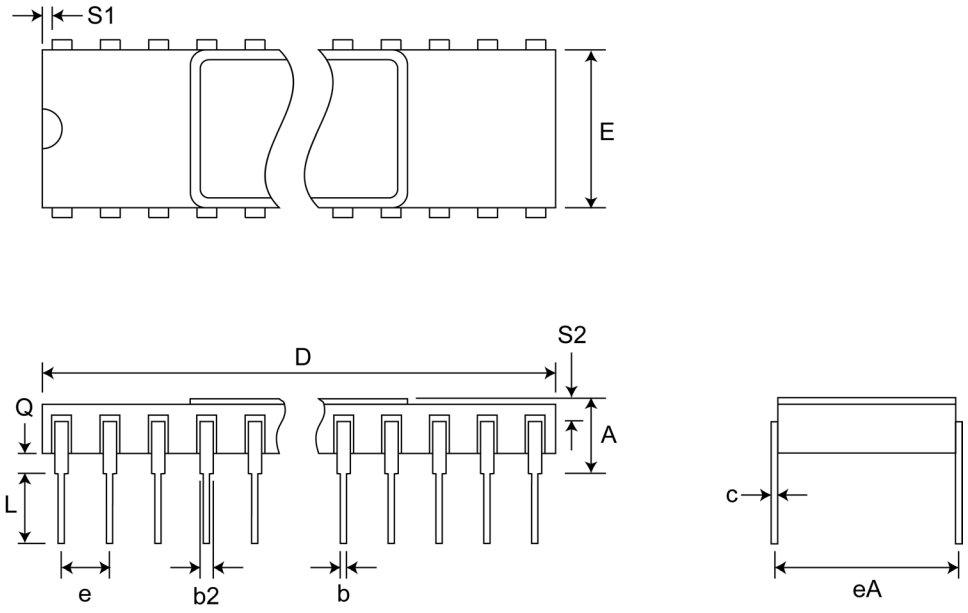
SIDEBRAZED DUAL IN-LINE PACKAGE (600 mil)

Pkg #	C10	
# Pins	32 (600 mil)	
Symbol	**Min**	**Max**
A	-	0.225
b	0.014	0.026
b2	0.045	0.065
C	0.008	0.018
D	-	1.680
E	0.510	0.620
eA	0.600 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.070
S1	0.005	-
S2	0.005	-



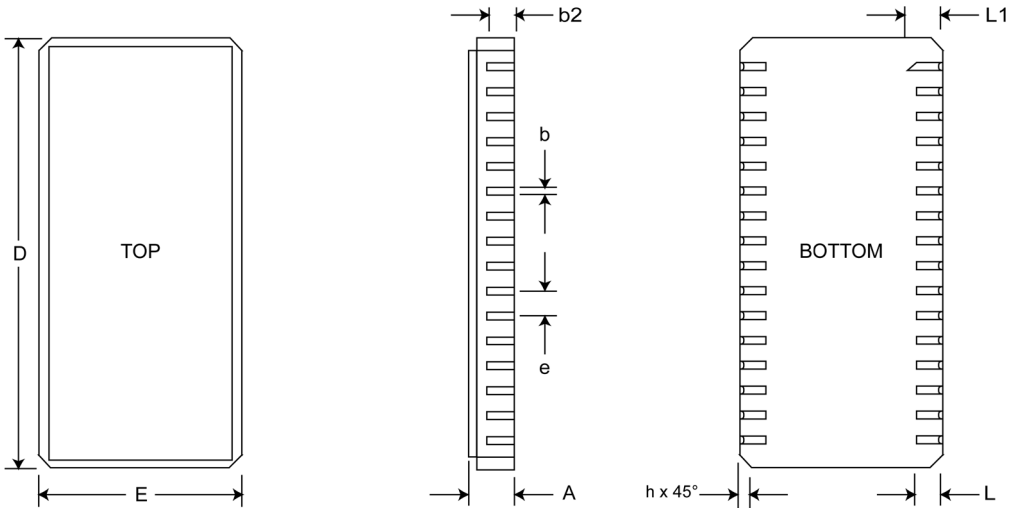
SIDEBRAZED DUAL IN-LINE PACKAGE (400 mil)

Pkg #	C11	
# Pins	32 (400 mil)	
Symbol	**Min**	**Max**
A	-	0.232
b	0.014	0.023
b2	0.038	0.065
C	0.008	0.018
D	-	1.700
E	0.350	0.410
eA	0.400 BSC	
e	0.100 BSC	
L	0.125	0.200
Q	0.015	0.060
S1	0.005	-
S2	0.005	-



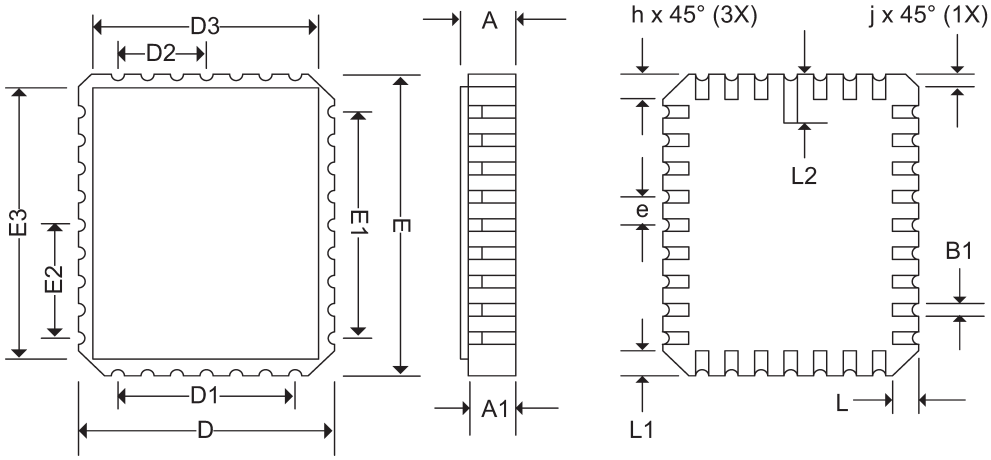
Pkg #	L1	
# Pins	32	
Symbol	**Min**	**Max**
A	0.080	0.100
b	0.022	0.028
b1	0.006	0.022
b2	0.040	-
D	0.820	0.840
E	0.392	0.400
e	0.050 BSC	
h	0.012 REF	
L	0.070	0.080
L1	0.090	0.110
L2	0.003	0.015
N	32	

2-SIDED LEADLESS CHIP CARRIER



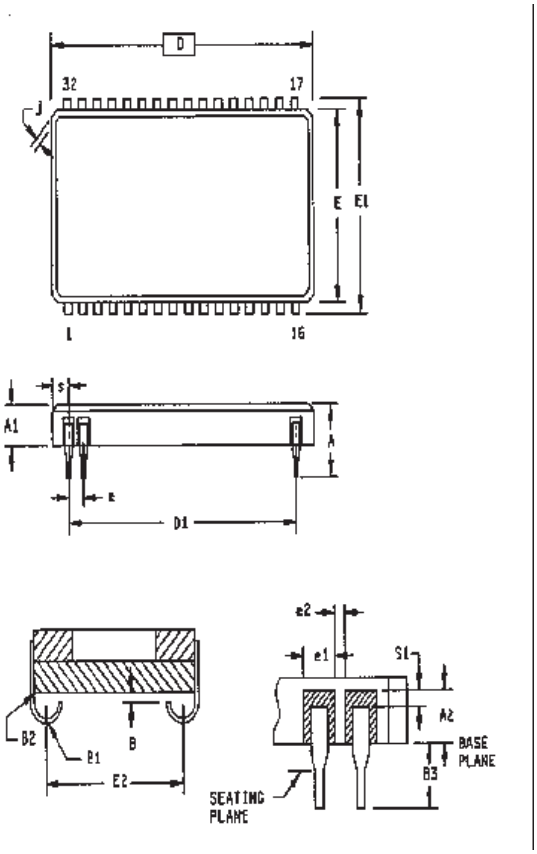
Pkg #	L6	
# Pins	32	
Symbol	**Min**	**Max**
A	0.060	0.075
A1	0.050	0.065
B1	0.022	0.028
D	0.442	0.458
D1	0.300 BSC	
D2	0.150 BSC	
D3	-	0.458
E	0.540	0.560
E1	0.400 BSC	
E2	0.200 BSC	
E3	-	0.558
e	0.050 BSC	
h	0.040 REF	
j	0.020 REF	
L	0.045	0.055
L1	0.045	0.055
L2	0.075	0.095
ND	7	
NE	9	

RECTANGULAR LEADLESS CHIP CARRIER



Pkg #	CJ1	
# Pins	32	
Symbol	**Min**	**Max**
A	0.120	0.165
A1	0.088	0.120
A2	0.070	REF
B	0.010	REF
B1	0.030R	TYP
B2	0.020	REF
B3	0.025	0.045
D	0.816	0.838
D1	0.750	REF
E	0.419	0.431
E1	0.430	0.445
E2	0.360	0.380
e	0.050 BSC	
e1	0.038	TYP
e2	0.005	
j	0.005	TYP
S	0.030	0.040
S1	0.020	TYP

CERAMIC SOJ SMALL OUTLINE IC PACKAGE



REVISIONS

DOCUMENT NUMBER:	SRAM124
DOCUMENT TITLE:	P4C1024 HIGH SPEED 128K x 8 DUAL CHIP ENABLE CMOS STATIC RAM

REV.	ISSUE DATE	ORIG. OF CHANGE	DESCRIPTION OF CHANGE
OR	1997	DAB	New Data Sheet
A	Oct-05	JDB	Change logo to Pyramid
B	Jan-11	JDB	Added L1 package, corrected data retention table
C	Dec-11	JDB	Removed Selection Guide, combined commercial and industrial temps in features section