

HEXFET® Power MOSFET

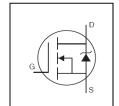


Features

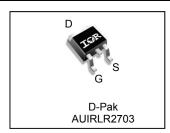
- Advanced Planar Technology
- · Logic Level Gate Drive
- Low On-Resistance
- Dynamic dV/dT Rating
- 175°C Operating Temperature
- Fast Switching
- · Fully Avalanche Rated
- · Repetitive Avalanche Allowed up to Timax
- · Lead-Free, RoHS Compliant
- Automotive Qualified *

Description

Specifically designed for Automotive applications, this cellular design of HEXFET® Power MOSFETs utilizes the latest processing techniques to achieve low on-resistance per silicon area. This benefit combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in Automotive and a wide variety of other applications.



V _{DSS}	30V
R _{DS(on)} max.	45mΩ
D (Silicon Limited)	23A
D (Package Limited)	20A



G	D	S
Gate	Drain	Source

Page part number Dockers Type		Standard Pack		Orderable Part Number	
Base part number	Package Type	Form	Quantity	Orderable Part Number	
ALUDI DOZOS	D. Dok	Tube	75	AUIRLR2703	
AUIRLR2703	D-Pak	Tape and Reel Left	3000	AUIRLR2703TRL	

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	23		
I _D @ T _C = 100°C	Continuous Drain Current, V _{GS} @ 10V (Silicon Limited)	16	A	
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ 10V (Package Limited) 20			
I _{DM}	Pulsed Drain Current ①	96		
P _D @T _C = 25°C	Maximum Power Dissipation	45	W	
	Linear Derating Factor	0.30	W/°C	
V_{GS}	Gate-to-Source Voltage	± 16	V	
E _{AS}	Single Pulse Avalanche Energy (Thermally Limited) ②	77	m l	
E _{AS (tested)}	Single Pulse Avalanche Energy (tested Value) ®	200	mJ	
I _{AR}	Avalanche Current ①	14	А	
E _{AR}	Repetitive Avalanche Energy ①	4.5	mJ	
dv/dt	Peak Diode Recovery®	5.0	V/ns	
T_J	Operating Junction and	-55 to + 175		
T _{STG}	Storage Temperature Range		°C	
	Soldering Temperature, for 10 seconds (1.6mm from case)	300		

Thermal Resistance

Symbol	nbol Parameter		Max.	Units
$R_{\theta JC}$	Junction-to-Case ®		3.3	
$R_{ heta JA}$	Junction-to-Ambient (PCB Mount) ∅		50	°C/W
$R_{ heta JA}$	Junction-to-Ambient		110	

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^{*}Qualification standards can be found at www.infineon.com



Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	30			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		0.030		V/°C	Reference to 25 $^{\circ}$ C, I_{D} = 1mA
				0.045		V _{GS} = 10V, I _D = 14A ④
$R_{DS(on)}$	Static Drain-to-Source On-Resistance			0.065	Ω	V _{GS} = 4.5V, I _D = 12A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0			V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
gfs	Forward Trans conductance	6.4			S	V _{DS} = 25V, I _D = 14A ⑦
1	Drain-to-Source Leakage Current			25	μA	$V_{DS} = 30V, V_{GS} = 0V$
IDSS	Diam-to-Source Leakage Current			250	μΑ	$V_{DS} = 24V, V_{GS} = 0V, T_{J} = 150^{\circ}C$
I _{GSS}	Gate-to-Source Forward Leakage			100	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage			-100	ПА	V _{GS} = - 16V

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

Q_g	Total Gate Charge	 	15		I _D = 14A
Q_{gs}	Gate-to-Source Charge	 	4.6	nC	$V_{DS} = 24V$
Q_{gd}	Gate-to-Drain Charge	 	9.3		V _{GS} = 4.5V ④⑦
$t_{d(on)}$	Turn-On Delay Time	 8.5			V _{DD} = 15V
t _r	Rise Time	 140		no	I _D = 14A
$t_{d(off)}$	Turn-Off Delay Time	 12		ns	$R_G = 12\Omega, V_{GS} = 4.5V$
t _f	Fall Time	 20			$R_D = 1.1\Omega $
L _D	Internal Drain Inductance	 4.5			Between lead, 6mm (0.25in.)
L _S	Internal Source Inductance	 7.5			from package and center of die contact
C _{iss}	Input Capacitance	 450			$V_{GS} = 0V$
Coss	Output Capacitance	210		pF	V _{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	 110			<i>f</i> = 1.0MHz⑦

Diode Characteristics

	Parameter	Min.	Тур.	Max.	Units	Conditions
	Continuous Source Current			226		MOSFET symbol
I _S	(Body Diode)			23 ⑤	^	showing the
	Pulsed Source Current			06	A	integral reverse
I _{SM}	(Body Diode) ①			- 96		p-n junction diode.
V_{SD}	Diode Forward Voltage			1.3	V	$T_J = 25^{\circ}C, I_S = 14A, V_{GS} = 0V $
t _{rr}	Reverse Recovery Time		65	97	ns	$T_J = 25^{\circ}C$, $I_F = 14A$
Q_{rr}	Reverse Recovery Charge		140	210	nC	di/dt = 100A/µs④⑦
t _{on}	Forward Turn-On Time	Intrinsi	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)			

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- $^{\circ}$ V_{DD} =15V,Starting T_J = 25°C, L = 570 μ H, R_G = 25 Ω , I_{AS} = 14A (See fig. 12)
- $\label{eq:local_local_local} \begin{tabular}{ll} \begin{tabular$
- 4 Pulse width $\leq 300 \mu s$; duty cycle $\leq 2\%$.
- © Calculated continuous current based on maximum allowable junction temperature. Package limitation current = 20A.
- © This is applied for I-PAK, LS of D-PAK is measured between lead and center of die contact.
- ② Uses IRL2703 data and test conditions.



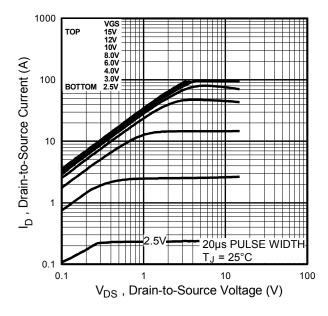


Fig. 1 Typical Output Characteristics

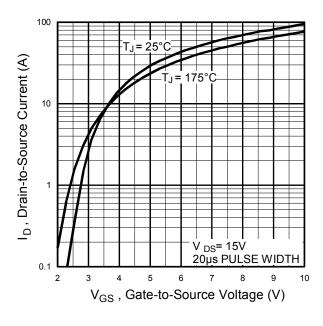


Fig. 3 Typical Transfer Characteristics

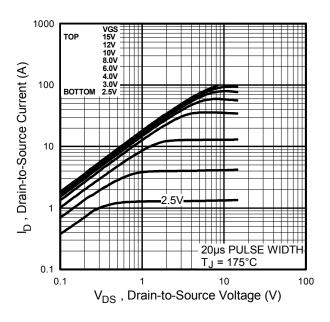


Fig. 2 Typical Output Characteristics

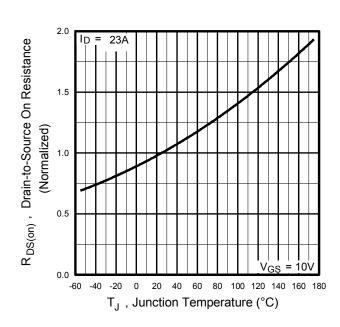


Fig. 4 Normalized On-Resistance Vs. Temperature



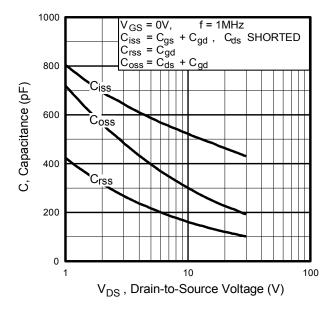


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

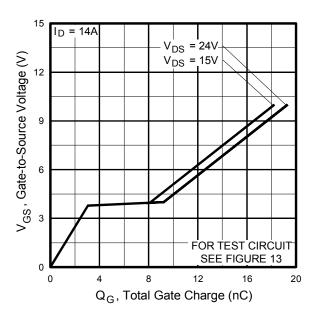


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

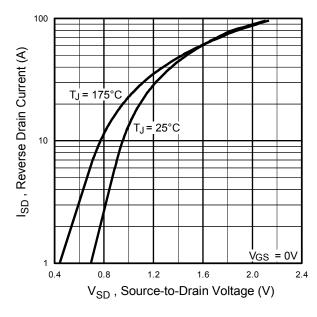


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

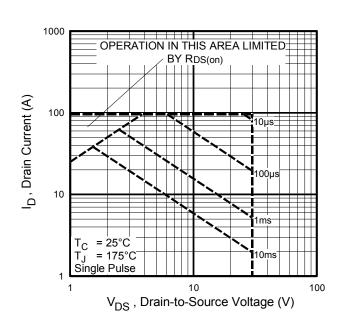


Fig 8. Maximum Safe Operating Area



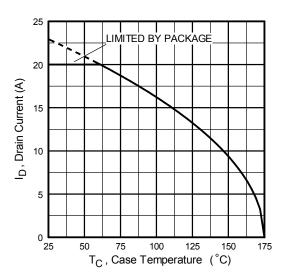


Fig 9. Maximum Drain Current Vs. Case Temperature

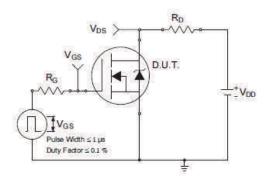


Fig 10a. Switching Time Test Circuit

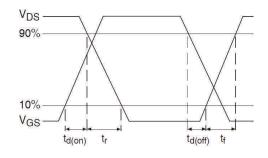


Fig 10b. Switching Time Waveforms

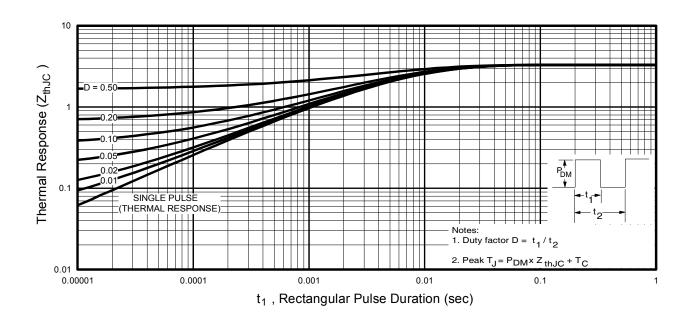


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case



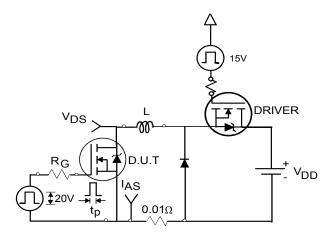


Fig 12a. Unclamped Inductive Test Circuit

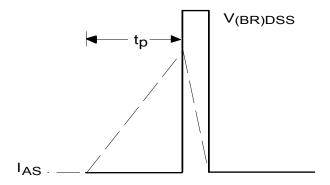


Fig 12b. Unclamped Inductive Waveforms

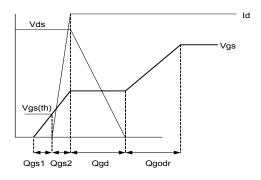


Fig 13a. Gate Charge Waveform

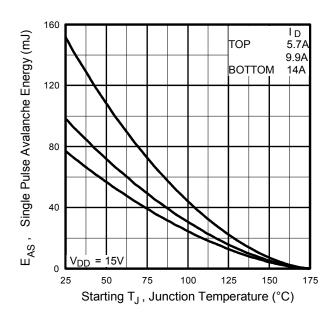


Fig 12c. Maximum Avalanche Energy vs. Drain Current

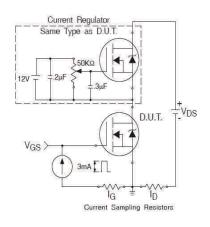
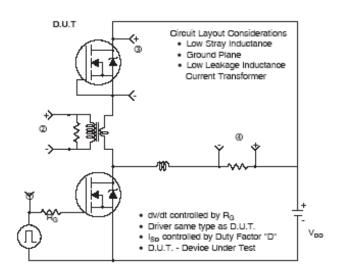
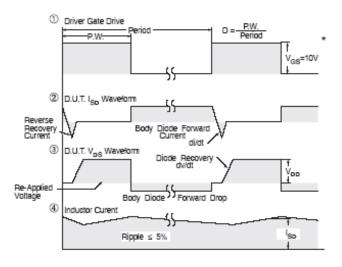


Fig 13b. Gate Charge Test Circuit



Peak Diode Recovery dv/dt Test Circuit



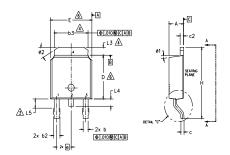


^{*} V_{GS} = 5V for Logic Level Devices

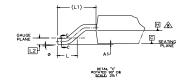
Fig 14. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

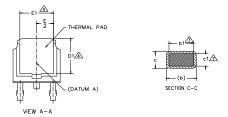


D-Pak (TO-252AA) Package Outline (Dimensions are shown in millimeters (inches))









NOTES:

- 1.- DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
- 2.- DIMENSION ARE SHOWN IN INCHES [MILLIMETERS].
- 1 LEAD DIMENSION UNCONTROLLED IN L5.
- A- DIMENSION D1, E1, L3 & b3 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
- 5.— SECTION C-C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 AND 0.10 [0.13 AND 0.25] FROM THE LEAD TIP.
- bildension D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005 [0.13] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
- A- DIMENSION b1 & c1 APPLIED TO BASE METAL ONLY.
- ♠ DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
- 9.- OUTLINE CONFORMS TO JEDEC OUTLINE TO-252AA.

S Y M	DIMENSIONS				
В	MILLIM	MILLIMETERS INCHES			
0 L	MIN.	MAX.	MIN.	MAX.	E S
Α	2.18	2.39	.086	.094	
A1	-	0.13	_	.005	
b	0.64	0.89	.025	.035	
ь1	0.65	0.79	.025	.031	7
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	4
С	0.46	0.61	.018	.024	
c1	0.41	0.56	.016	.022	7
c2	0.46	0.89	.018	.035	
D	5.97	6.22	.235	.245	6
D1	5.21	-	.205	-	4
Ε	6.35	6.73	.250	.265	6
E1	4.32	-	.170	-	4
е	2.29	BSC	.090	BSC	
Н	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74	BSC	.108	REF.	
L2	0.51	BSC	.020	BSC	
L3	0.89	1.27	.035	.050	4
L4	-	1.02	-	.040	
L5	1.14	1.52	.045	.060	3
ø	0,	10*	0,	10°	
ø1	0.	15*	0.	15*	
ø2	25°	35°	25*	35°	

LEAD ASSIGNMENTS

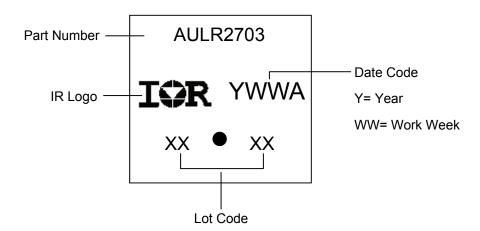
HEXFET

- 1.- GATE
- 2.- DRAIN
- 3.- SOURCE
- 4.- DRAIN

IGBT & CoPAK

- 1.- GATE
- 2.- COLLECTOR
- 3.- EMITTER
- 4.- COLLECTOR

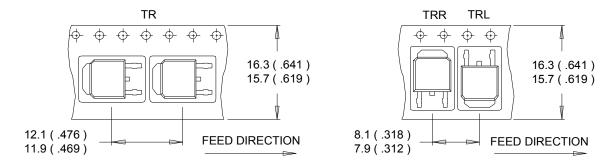
D-Pak (TO-252AA) Part Marking Information



Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

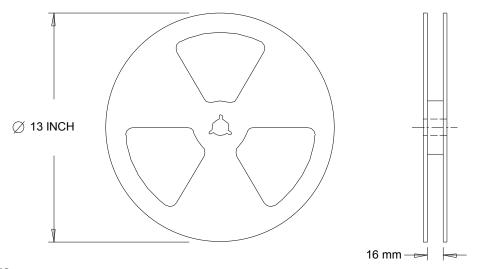


D-Pak (TO-252AA) Tape & Reel Information (Dimensions are shown in millimeters (inches))



NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES:

1. OUTLINE CONFORMS TO EIA-481.

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/



Qualification Information

		1					
		Automotive					
		(per AEC-Q101)					
Qualificat	tion Level	Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.					
Moisture	Sensitivity Level	D-Pak	MSL1				
			Class M2 (+/- 150V) [†]				
	Machine Model	AEC-Q101-002					
FOR	Liverage Dady Madal	Class H1A (+/- 500V) †					
ESD	Human Body Model	AEC-Q101-001					
Charged Device Model		Class C5 (+/- 2000V) [†]					
		AEC-Q101-005					
RoHS Co	mpliant	Yes					

[†] Highest passing voltage.

Revision History

Date	Comments		
12/11/2015	Updated datasheet with corporate template		
12/11/2015	Corrected ordering table on page 1.		

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