MN74HC240/MN74HC240S

Inverting Octal TRI-STATE Buffers

■ Description

MN74HC240/MN74HC240S are high-speed inverting buffers constructed with octal tri-state outputs. High-speed operation can be obtained for driving a large capacity bus line, because these ICs have large current output. When the output is "L", inputs 1G and 2G are available, where output becomes enable and each of the four buffers is independently controlled. Adoption of the silicon gate CMOS process makes possible low power consumption and a high noise allowance; LS TTl 15-inputs can be directly driven. Resistors and diodes are used in the V_{DD} and V_{SS} in order to protect the input/output from damage by static electricity. Same pin configuration and function as standard 54LS/74LS Logic Family.

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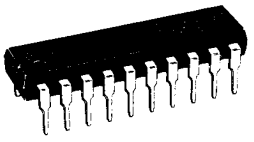

20-pin plastic DIL package

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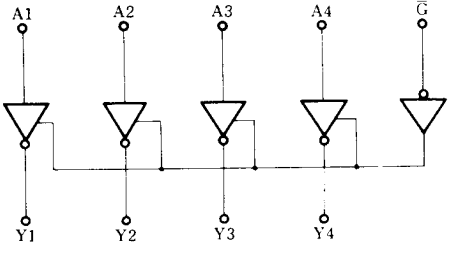
20-pin Panaflat package (SO-20D)

■ Truth table

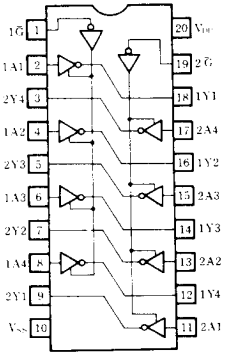
$1\bar{G}$	1A	1Y	$2\bar{G}$	2A	2Y
L	L	H	L	L	H
L	H	L	L	H	L
H	L	Hi-Z	H	L	Hi-Z
H	H	Hi-Z	H	H	Hi-Z

Note:
1. Hi-Z: High impedance

■ Logic diagram (1 gate)



Pin configuration (top view)



■ Absolute maximum ratings

Item			Sym.	Rating	Unit
Supply voltage			V_{DD}	−0.5～7.0	V
Input/output voltage			V_I, V_O	−0.5～V_{DD}+0.5	V
Input current			I_I	±20	mA
Output current			I_O	±35	mA
Power dissipation	MN74HC240	Ta=−40～+60℃	P_D	400	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 8mW/℃	
	MN74HC240S	Ta=−40～+60℃	P_D	275	mW
		Ta=+60～+85℃		Decrease to 200mW at the rate of 3.8mW/℃	
Storage temperature range			T_{stg}	−65～+150	℃
Supply current			I_{DD}, I_{SS}	±50	mA

■ Recommended operating conditions

Item	Sym.	Rating	Unit
Operating supply voltage	V_{DD}	1.4～6.0	V
Input voltage	V_I	0～V_{DD}	V
Operating temperature range	T_{opr}	−40～+85	℃
Input rise and fall time	t_r, t_f	0～500	ns

■ DC characteristics (V_{DD}=5V±10%, V_{SS}=0V)

Item	Sym.	Test conditions		Ta=−40℃		Ta=+25℃		Ta=+85℃		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
Quiescent supply current	I_{DD}	V_I=V_{DD} or V_{SS}			4		4		40	μA
High level input voltage	V_{IH}	V_O=V_{DD}−1.0V or 0.5V, $\|I_O\|$≦1μA	V_{DD}=4.5V	3.15		3.15		3.15		V
			V_{DD}=5.0V	3.50		3.50		3.50		
			V_{DD}=5.5V	3.85		3.85		3.85		
Low level input voltage	V_{IL}	V_O=V_{DD}−1.0V or 0.5V, $\|I_O\|$≦1μA	V_{DD}=4.5V		0.9		0.9		0.9	V
			V_{DD}=5.0V		1.0		1.0		1.0	
			V_{DD}=5.5V		1.1		1.1		1.1	
Input current	±I_I	V_I=V_{DD} or V_{SS}			0.3		0.3		1	μA
High level output voltage	V_{OH}	V_I=V_{SS}, $\|I_O\|$≦1μA		V_{DD}−0.05		V_{DD}−0.05		V_{DD}−0.05		V
Low level output voltage	V_{OL}	V_I=V_{DD} or V_{SS}, $\|I_O\|$≦1μA			0.05		0.05		0.05	V
High level output current	I_{OH}	V_I=V_{SS}, V_O=V_{DD}−0.8V		−9		−7.5		−6		mA
Low level output current	I_{OL}	V_I=V_{DD} or V_{SS}, V_O=0.4V		9		7.5		6		mA
Output leakage current	±I_{OZ}	V_I=V_{DD} or V_{SS}, V_O=V_{DD} or V_{SS}			0.4		0.4		1	μA

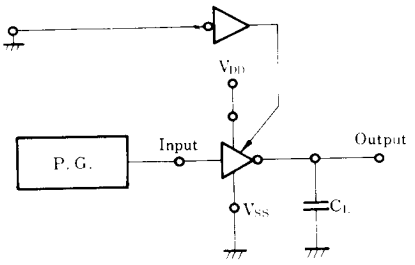
■ AC characteristics (V_{DD}=5V, V_{SS}=0V, Ta=25℃ Input transition time ≦6ns, C_L=50pF)

Item	Sym.	Test conditions	Min.	Typ.	Max.	Unit
Output rise time	t_{TLH}			7	15	ns
Output fall time	t_{THL}			6	15	ns
Propagation time (L→H)	t_{PLH}			8	15	ns
Propagation time (H→L)	t_{PHL}			7	15	ns
3-stage propagation time (H→Z)	t_{PHZ}	R_L=1kΩ		12	20	ns
3-stage propagation time (L→Z)	t_{PLZ}	R_L=1kΩ		15	25	ns
3-stage propagation time (Z→H)	t_{PZH}	R_L=1kΩ		11	20	ns
3-stage propagation time (Z→L)	t_{PZL}	R_L=1kΩ		12	20	ns

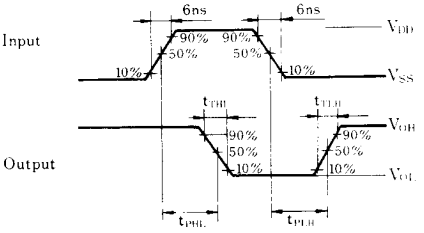
※ Switching time measurement circuit and waveform

〔1〕 t_{TLH}, t_{THL}, t_{PLH}, t_{PHL}

1. Measurement circuit

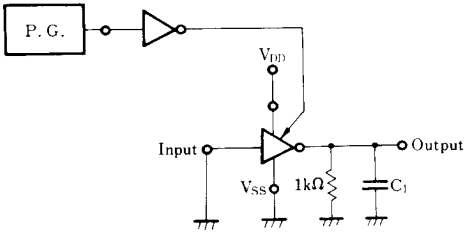


2. Waveforms

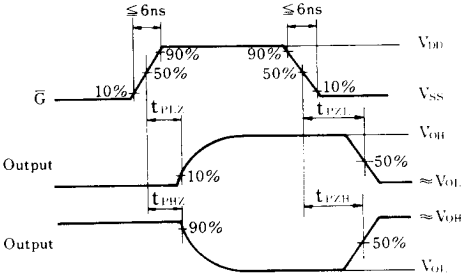


〔2〕 t_{PHZ}, t_{PZH}

1. Measurement circuit



2. Waveforms (t_{PHZ}, t_{PZH}, t_{PLZ}, t_{PZL})



〔3〕 t_{PLZ}, t_{PZL}

1. Measurement circuit