

SNx4AHC16244 16-Bit Buffers/Drivers With 3-State Outputs

1 Features

- Members of the Texas Instruments *Widebus™* Family
- EPIC™* (Enhanced-Performance Implanted CMOS) Process
- Operating Range 2-V to 5.5-V V_{CC}
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)

2 Applications

- Motor Drives
- Wireless Infrastructures
- Health and Fitness Wearables
- Telecom Infrastructures
- Electronic Points of Sale

3 Description

The SNx4AHC16244 devices are 16-bit buffers and line drivers designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4AHC16244	SSOP (48)	15.80 mm × 7.50 mm
	TSSOP (48)	12.50 mm 6.10 mm
	TVSOP (48)	9.70 mm 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

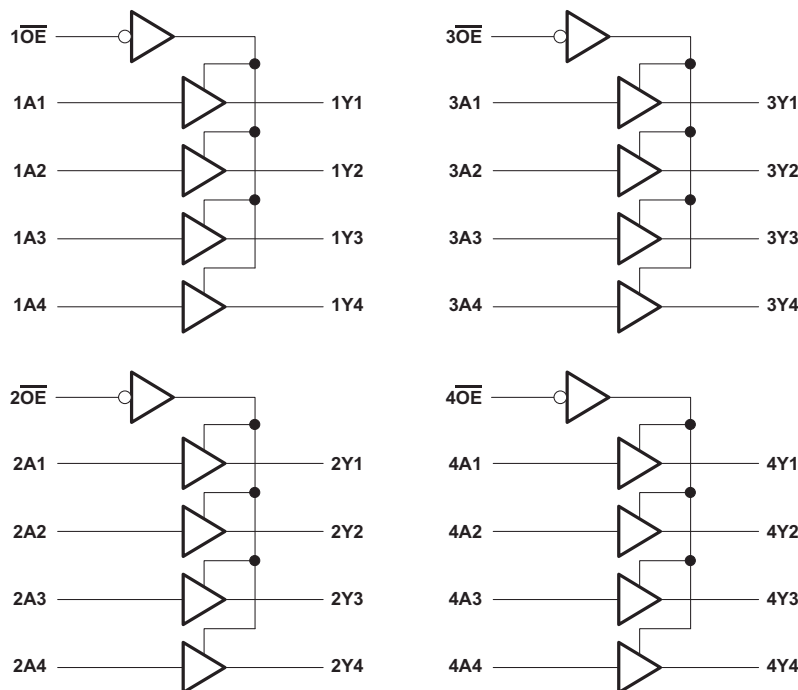


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5 Revision History

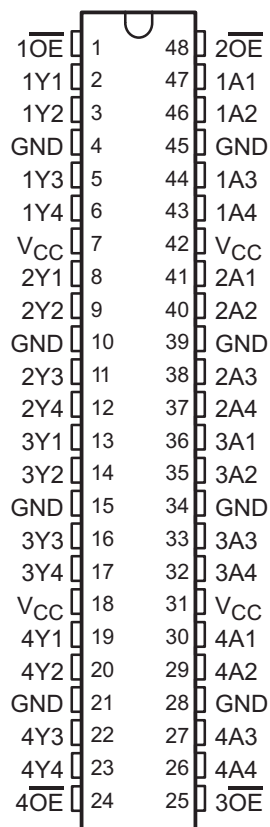
Changes from Revision G (January 2000) to Revision H

Page

• Updated document to new TI data sheet format.	1
• Deleted Ordering Information table.	1
• Added Applications.	1
• Added Pin Functions table.	3
• Added Pin Functions table.	4
• Added Handling Ratings table.	5
• Changed MAX operating temperature to 125°C in Recommended Operating Conditions table.	5
• Added Thermal Information table.	6
• Added –40°C to 125°C range for SN74AHC16244 in Electrical Characteristics table.	6
• Added $T_A = -40^\circ\text{C}$ to 125°C for SN74AHC16244 in both Switching Characteristics tables.	7
• Added Typical Characteristics.	8
• Added Detailed Description section.	10
• Added Application and Implementation section.	12
• Added Power Supply Recommendations and Layout sections.	13

6 Pin Configuration and Functions

SN54AHC16244 . . . WD PACKAGE
SN74AHC16244 . . . DGG, DGV, OR DL PACKAGE
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1OE	I	Output Enable 1
2	1Y1	O	1Y1 Output
3	1Y2	O	1Y2 Output
4	GND	—	Ground Pin
5	1Y3	O	1Y3 Output
6	1Y4	O	1Y4 Output
7	V _{CC}	—	Power Pin
8	2Y1	O	2Y1 Output
9	2Y2	O	2Y2 Output
10	GND	—	Ground Pin
11	2Y3	O	2Y3 Output
12	2Y4	O	2Y4 Output
13	3Y1	O	3Y1 Output
14	3Y2	O	3Y2 Output
15	GND	—	Ground Pin
16	3Y3	O	3Y3 Output
17	3Y4	O	3Y4 Output
18	V _{CC}	—	Power Pin

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
19	4Y1	O	4Y1 Output
20	4Y2	O	4Y2 Output
21	GND	—	Ground Pin
22	4Y3	O	4Y3 Output
23	4Y4	O	4Y4 Output
24	$\overline{4OE}$	I	Output Enable 4
25	$\overline{3OE}$	I	Output Enable 3
26	4A4	I	4A4 Input
27	4A3	I	4A3 Input
28	GND	—	Ground Pin
29	4A2	I	4A2 Input
30	4A1	I	4A1 Input
31	V _{CC}	—	Power Pin
32	3A4	I	3A4 Input
33	3A3	I	3A3 Input
34	GND	—	Ground Pin
35	3A2	I	3A2 Input
36	3A1	I	3A1 Input
37	2A4	I	2A4 Input
38	2A3	I	2A3 Input
39	GND	—	Ground Pin
40	2A2	I	2A2 Input
41	2A1	I	2A1 Input
42	V _{CC}	—	Power Pin
43	1A4	I	1A4 Input
44	1A3	I	1A3 Input
45	GND	—	Ground Pin
46	1A2	I	1A2 Input
47	1A1	I	1A1 Input
48	$\overline{2OE}$	I	Output Enable 2

7 Specifications

7.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	–0.5	7	V
V _I	Input voltage range ⁽²⁾	–0.5	7	V
V _O	Output voltage range ⁽²⁾	–0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0		–20 mA
I _{OK}	Output clamp current	V _O < 0 or V _O > V _{CC}		±20 mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±25 mA
Continuous current through V _{CC} or GND				±75 mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

7.2 Handling Ratings

		MIN	MAX	UNIT
T _{stg}	Storage temperature range	–65	150	°C
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾		0 2000 V

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN54AHC16244 ⁽²⁾		SN74AHC16244		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5		1.5		V
		V _{CC} = 3 V	2.1		2.1		
		V _{CC} = 5.5 V	3.85		3.85		
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5		0.5		V
		V _{CC} = 3 V	0.9		0.9		
		V _{CC} = 5.5 V	1.65		1.65		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	−50		−50		μA
		V _{CC} = 3.3 V ± 0.3 V	−4		−4		mA
		V _{CC} = 5 V ± 0.5 V	−8		−8		
I _{OL}	Low-level output current	V _{CC} = 2 V	50		50		μA
		V _{CC} = 3.3 V ± 0.3 V	4		4		mA
		V _{CC} = 5 V ± 0.5 V	8		8		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100		100		ns/V
		V _{CC} = 5 V ± 0.5 V	20		20		
T _A	Operating free-air temperature		−55	125	−40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs* (SCBA004).
- (2) Product Preview

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHC16244			UNIT
		DGV	DL	DGG	
		48 PINS	48 PINS	48 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	83.5	64.6	72.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	35.7	34.5	26.8	
R _{θJB}	Junction-to-board thermal resistance	46.6	36.4	39.4	
ψ _{JT}	Junction-to-top characterization parameter	4.3	11.1	2.6	
ψ _{JB}	Junction-to-board characterization parameter	46.0	36.1	39.1	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report ([SPRA953](#)).

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC16244 ⁽¹⁾		SN74AHC16244		–40°C to 125°C SN74AHC16244		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = –50 μA	2 V	1.9	2		1.9		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		4.4		
	I _{OH} = –4 mA	3 V	2.58			2.48		2.48		2.48		
	I _{OH} = –8 mA	4.5 V	3.94			3.8		3.8		3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.5		0.44		0.44	
	I _{OL} = 8 mA	4.5 V			0.36		0.5		0.44		0.44	
I _I	V _I = V _{CC} or GND	0 V to 5.5 V			±0.1		±1 ⁽²⁾		±1		±1	μA
I _{OZ}	V _O = V _{CC} or GND	5.5 V			±0.25		±2.5		±2.5		±2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40		40	μA
C _i	V _I = V _{CC} or GND	5 V		2	10		10		10		10	pF
C _o	V _O = V _{CC} or GND	5 V		3.5								pF

(1) Product Preview

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

7.6 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC16244 ⁽¹⁾		SN74AHC16244		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$ SN74AHC16244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	5.8 ⁽²⁾	8.4 ⁽²⁾		1 ⁽²⁾	10 ⁽²⁾	1	10	1	11	ns
t_{PHL}				5.8 ⁽²⁾	8.4 ⁽²⁾		1 ⁽²⁾	10 ⁽²⁾	1	10	1	11	
t_{PZH}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	6.6 ⁽²⁾	10.6 ⁽²⁾		1 ⁽²⁾	12.5 ⁽²⁾	1	12.5	1	13.5	ns
t_{PZL}				6.6 ⁽²⁾	10.6 ⁽²⁾		1 ⁽²⁾	12.5 ⁽²⁾	1	12.5	1	13.5	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	5 ⁽²⁾	11.5 ⁽²⁾		1 ⁽²⁾	12.5 ⁽²⁾	1	12.5	1	13.5	ns
t_{PLZ}				5 ⁽²⁾	11.5 ⁽²⁾		1 ⁽²⁾	12.5 ⁽²⁾	1	12.5	1	13.5	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	8.3	11.9		1	13.5	1	13.5	1	14.5	ns
t_{PHL}				8.3	11.9		1	13.5	1	13.5	1	14.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	9.1	14.1		1	16	1	16	1	17	ns
t_{PZL}				9.1	14.1		1	16	1	16	1	17	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	10.3	14		1	16	1	16	1	17	ns
t_{PLZ}				10.3	14		1	16	1	16	1	17	
$t_{sk(0)}$			$C_L = 50\text{ pF}$			1.5 ⁽³⁾				1.5		1.5	ns

(1) Product Preview

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) On products compliant to MIL-PRF-38535, this parameter does not apply.

7.7 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC16244 ⁽¹⁾		SN74AHC16244		$T_A = -40^\circ\text{C to } 125^\circ\text{C}$ SN74AHC16244		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.9 ⁽²⁾	6 ⁽²⁾		1 ⁽²⁾	7 ⁽²⁾	1	6.5	1	7	ns
t_{PHL}				3.9 ⁽²⁾	6 ⁽²⁾		1 ⁽²⁾	7 ⁽²⁾	1	6.5	1	7	
t_{PZH}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	4.7 ⁽²⁾	7.3 ⁽²⁾		1 ⁽²⁾	8.5 ⁽²⁾	1	8.5	1	9.5	ns
t_{PZL}				4.7 ⁽²⁾	7.3 ⁽²⁾		1 ⁽²⁾	8.5 ⁽²⁾	1	8.5	1	9.5	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	5 ⁽²⁾	7.2 ⁽²⁾		1 ⁽²⁾	8.5 ⁽²⁾	1	8.5	1	9	ns
t_{PLZ}				5 ⁽²⁾	7.2 ⁽²⁾		1 ⁽²⁾	8.5 ⁽²⁾	1	8.5	1	9	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.4	8		1	9	1	8.5	1	9	ns
t_{PHL}				5.4	8		1	9	1	8.5	1	9	
t_{PZH}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	6.2	9.3		1	10.5	1	10.5	1	11.5	ns
t_{PZL}				6.2	9.3		1	10.5	1	10.5	1	11.5	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	6.7	9.2		1	10.5	1	10.5	1	11	ns
t_{PLZ}				6.7	9.2		1	10.5	1	10.5	1	11	
$t_{sk(0)}$			$C_L = 50\text{ pF}$			1 ⁽³⁾				1		1	ns

(1) Product Preview

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(3) On products compliant to MIL-PRF-38535, this parameter does not apply.

7.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		SN74AHC16244			UNIT
		MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		–0.2	–0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

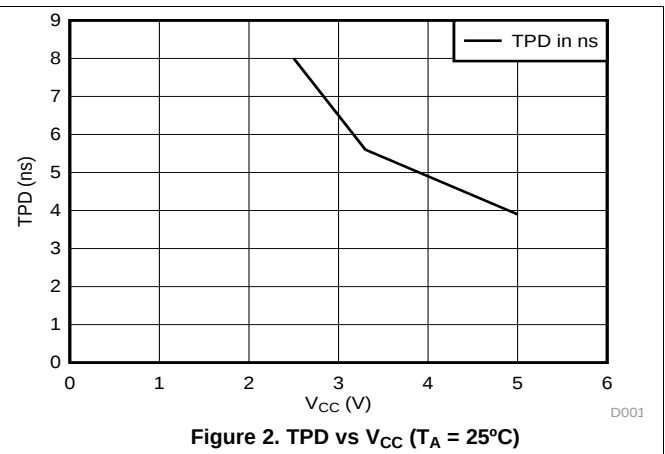
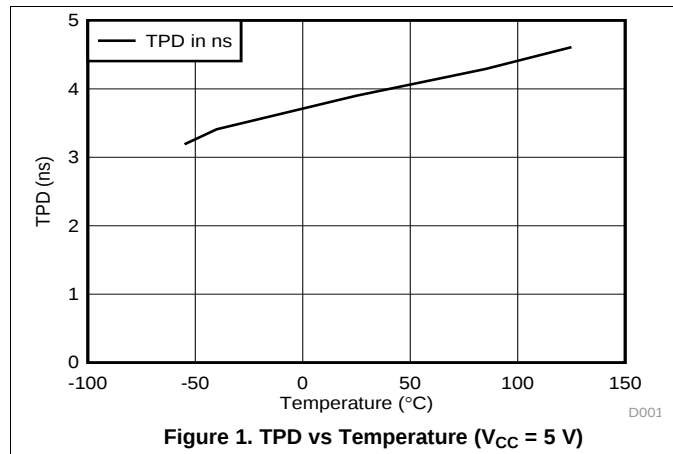
(1) Characteristics are for surface-mount packages only.

7.9 Operating Characteristics

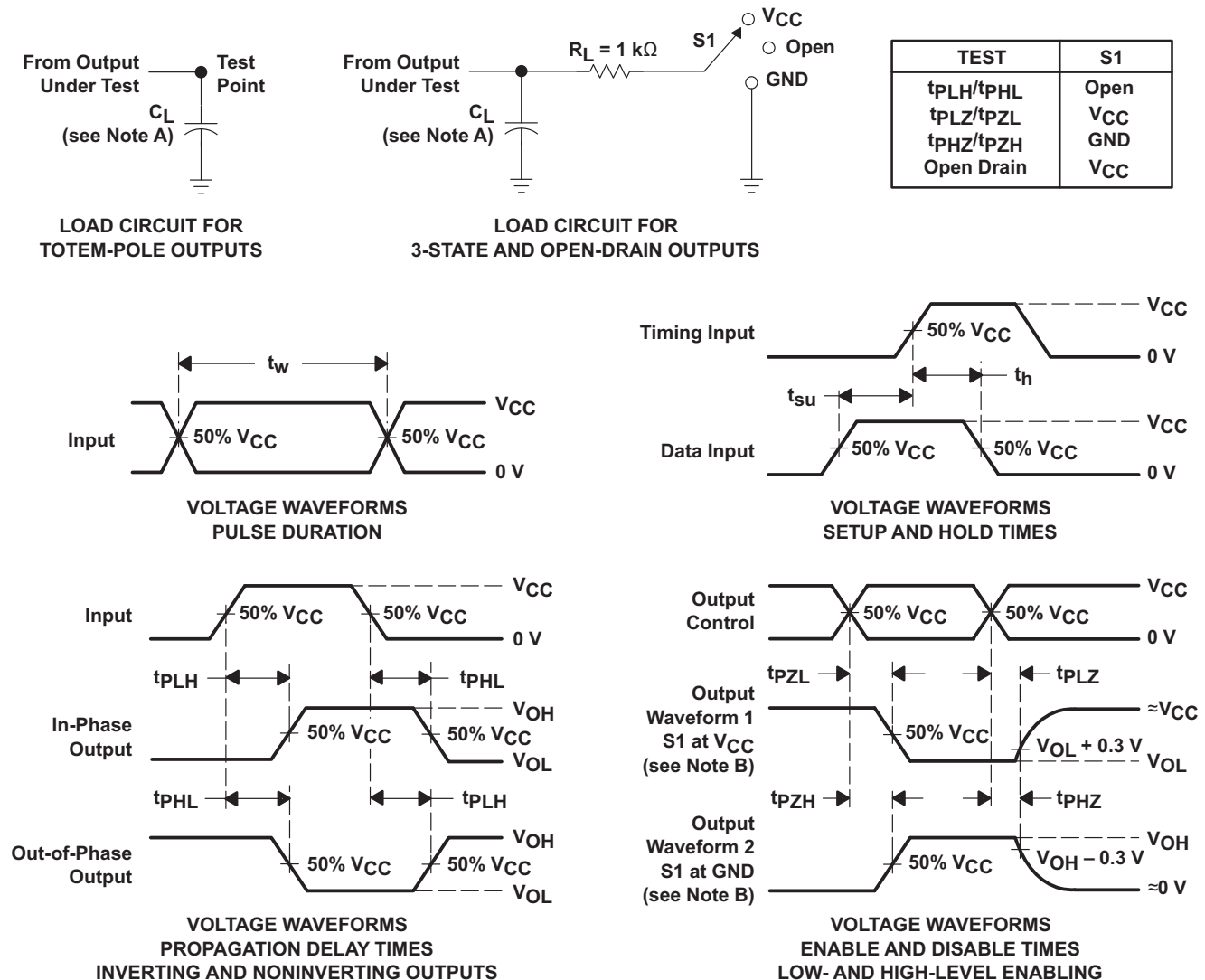
$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	10.5	pF

7.10 Typical Characteristics



8 Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.

D. The outputs are measured one at a time with one input transition per measurement.

Figure 3. Load Circuit and Voltage Waveforms

9 Detailed Description

9.1 Overview

The SNx4AHC16244 devices are 16-bit buffers and line drivers designed specifically to improve the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented receivers and transmitters.

These devices can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer. They provide true outputs and symmetrical active-low output-enable ($\overline{OE}$) inputs.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. The SN54AHC16244 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN74AHC16244 is characterized for operation from -40°C to 85°C .

9.2 Functional Block Diagram

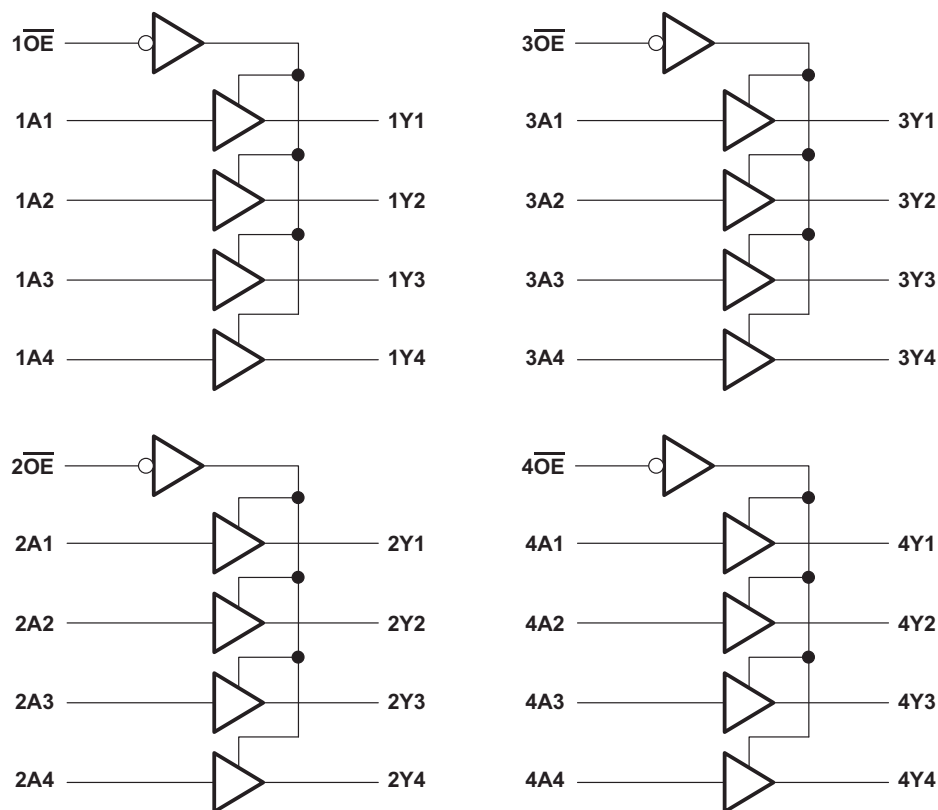
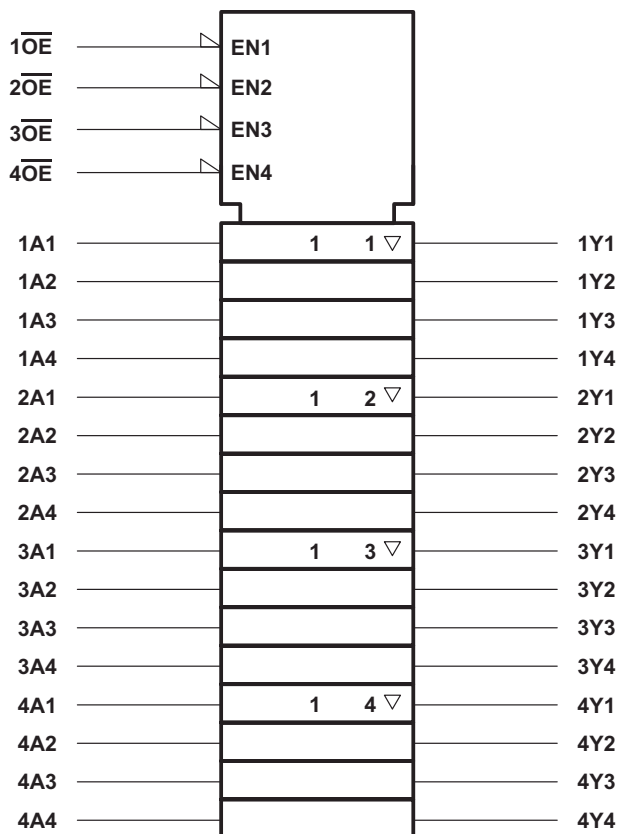


Figure 4. Logic Diagram (Positive Logic)

Functional Block Diagram (continued)



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Figure 5. Logic Symbol

9.3 Feature Description

- Wide operating voltage range
 - Operates from 2 V to 5.5 V
- Allows down voltage translation
 - Inputs accept voltages up to 5.5 V
- Slows edges rates, minimizing output ringing

9.4 Device Functional Modes

**Table 1. Function Table
(Each 4-bit Buffer/Driver)**

INPUTS		OUTPUT Y
$\overline{\text{OE}}$	A	
L	H	H
L	L	L
H	X	High-Z

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN74AHC16244 is a low-drive CMOS device that can be used for a multitude of applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs are tolerant to 5.5 V at any valid V_{CC} . This feature makes it ideal for translating down to the V_{CC} level. Figure 6 shows the reduction in ringing compared to higher-drive parts, such as AC.

10.2 Typical Application

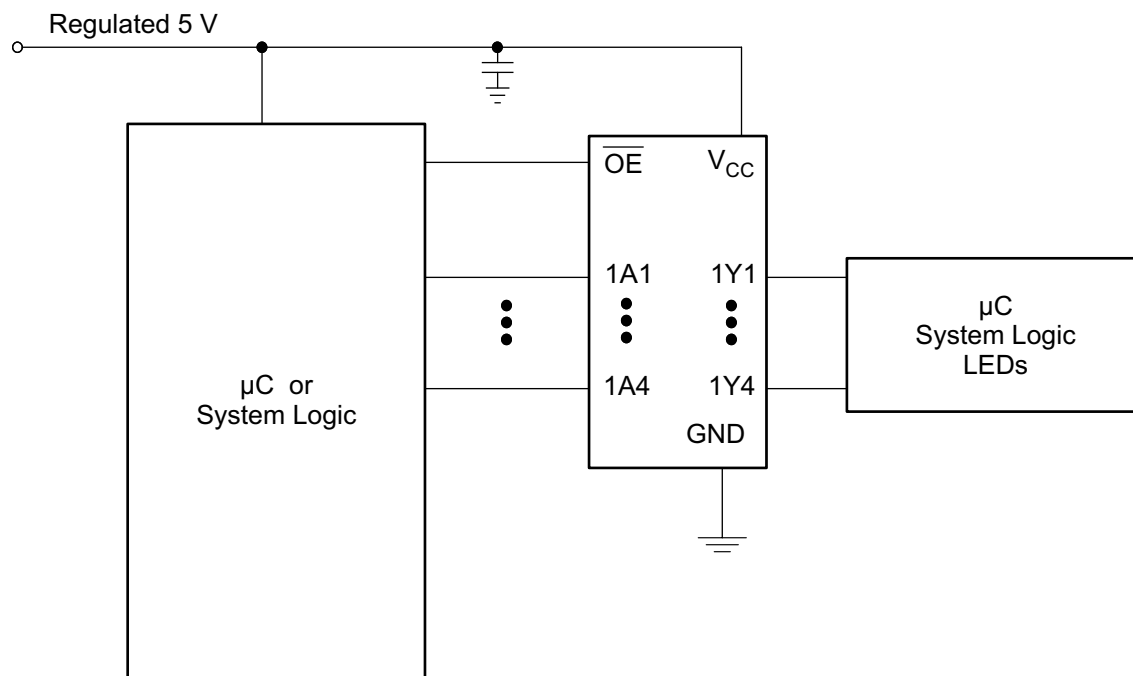


Figure 6. Application Diagram

10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

10.2.2 Detailed Design Procedure

- Recommended input conditions:
 - For rise time and fall time specifications, see $(\Delta t/\Delta V)$ in the [Recommended Operating Conditions](#) table.
 - For specified high and low levels, see $(V_{IH}$ and $V_{IL})$ in the [Recommended Operating Conditions](#) table.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommend output conditions:
 - Load currents should not exceed 25 mA per output and 75 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

Typical Application (continued)

10.2.3 Application Curves

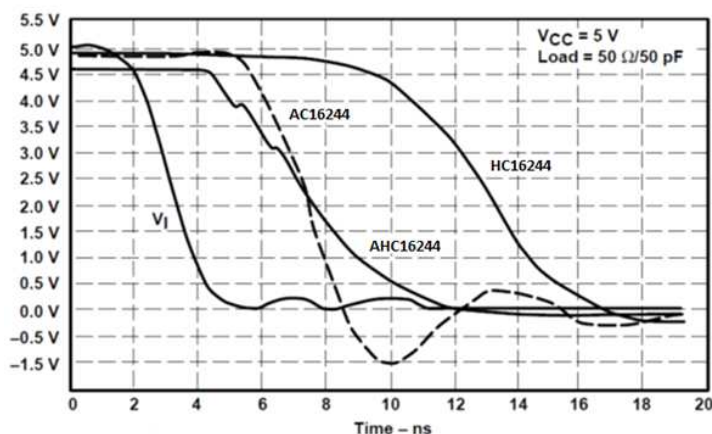


Figure 7. Switching Characteristics Comparison

11 Power Supply Recommendations

The power supply can be any voltage between the Min and Max supply voltage rating located in the [Recommended Operating Conditions](#).

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1 μF capacitor is recommended. If there are multiple V_{CC} terminals then 0.01 μF or 0.022 μF capacitors are recommended for each power terminal. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1 μF and 1.0 μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

12 Layout

12.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in [Figure 8](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} , whichever makes more sense or is more convenient. It is generally acceptable to float outputs unless the part is a transceiver.

12.2 Layout Example

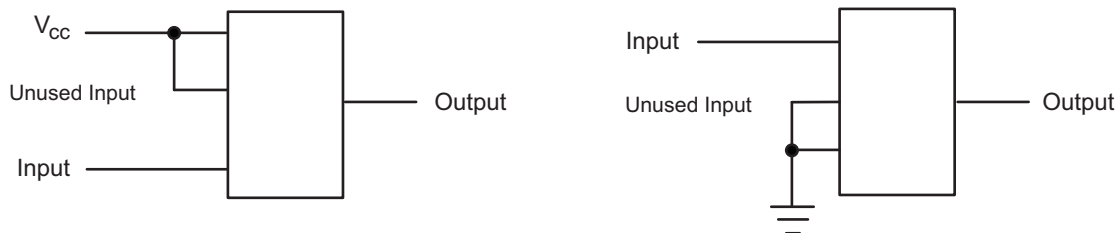


Figure 8. Layout Diagram

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 2. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHC16244	Click here	Click here	Click here	Click here	Click here
SN74AHC16244	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

Widebus is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
74AHC16244DGGRG4	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC16244
SN74AHC16244DGGR	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC16244
SN74AHC16244DGGR.A	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC16244
SN74AHC16244DGGR.B	Active	Production	TSSOP (DGG) 48	2000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC16244
SN74AHC16244DGVR	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HE244
SN74AHC16244DGVR.A	Active	Production	TVSOP (DGV) 48	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HE244
SN74AHC16244DL	Obsolete	Production	SSOP (DL) 48	-	-	Call TI	Call TI	-40 to 125	AHC16244
SN74AHC16244DLR	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC16244
SN74AHC16244DLR.A	Active	Production	SSOP (DL) 48	1000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC16244
SN74AHC16244DLR.B	Active	Production	SSOP (DL) 48	1000 LARGE T&R	-	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC16244

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC16244DGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74AHC16244DGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74AHC16244DLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

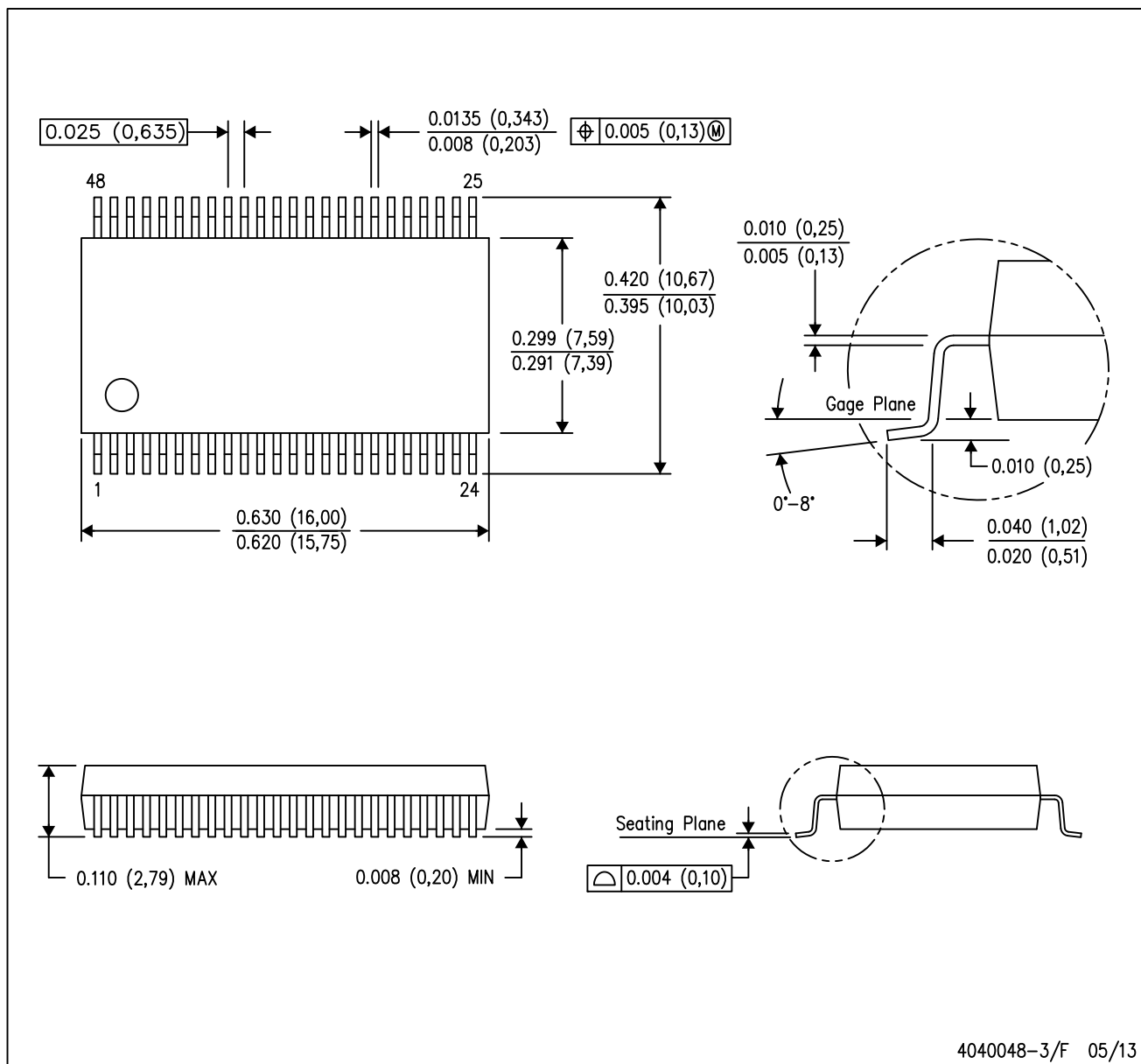


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC16244DGGR	TSSOP	DGG	48	2000	356.0	356.0	45.0
SN74AHC16244DGVR	TVSOP	DGV	48	2000	353.0	353.0	32.0
SN74AHC16244DLR	SSOP	DL	48	1000	356.0	356.0	53.0

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MO-118

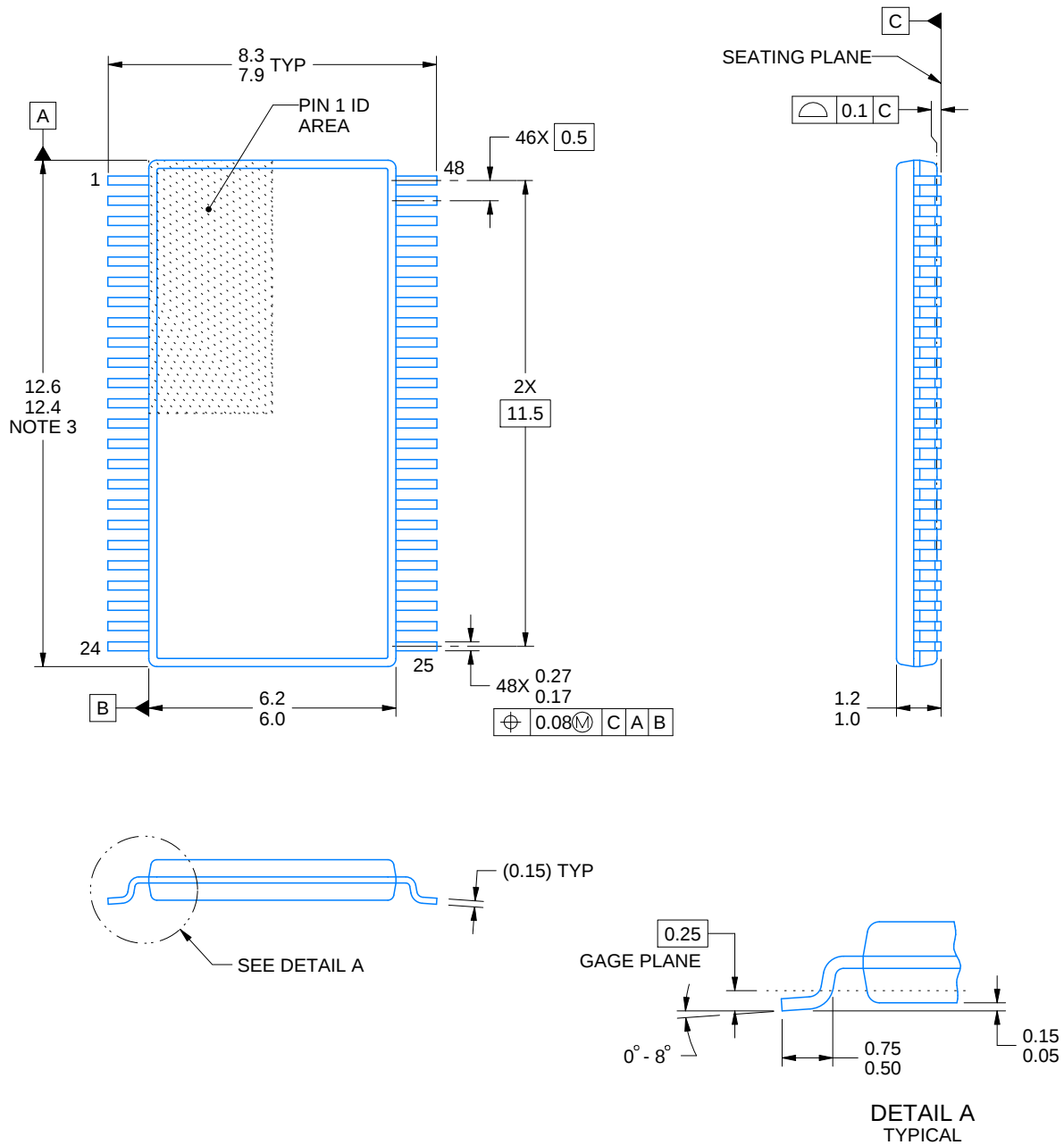
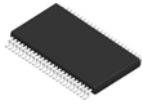
DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194



4214859/B 11/2020

NOTES:

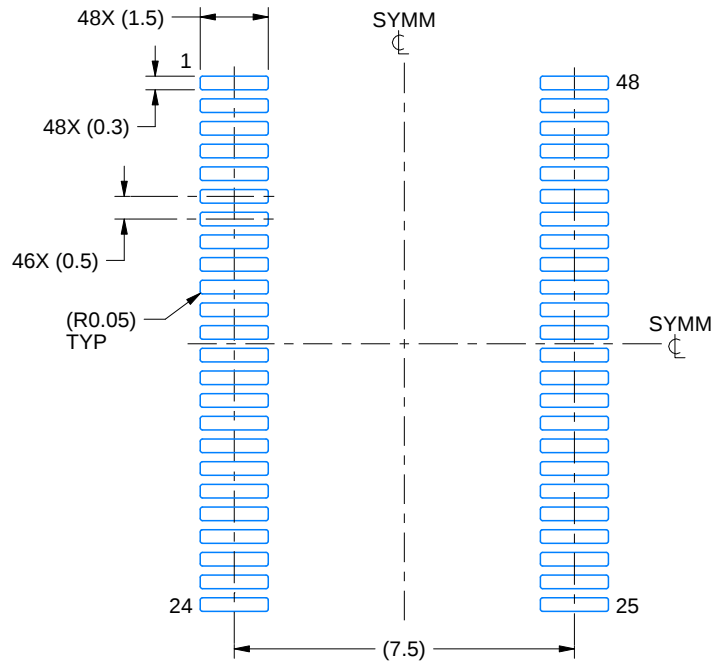
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

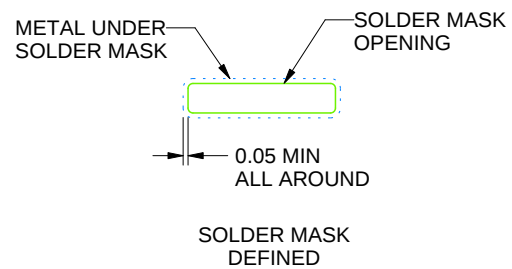
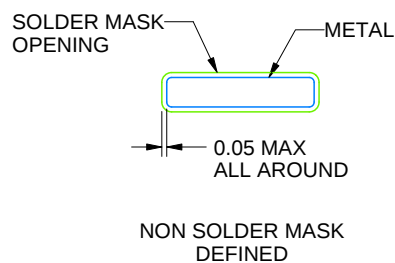
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

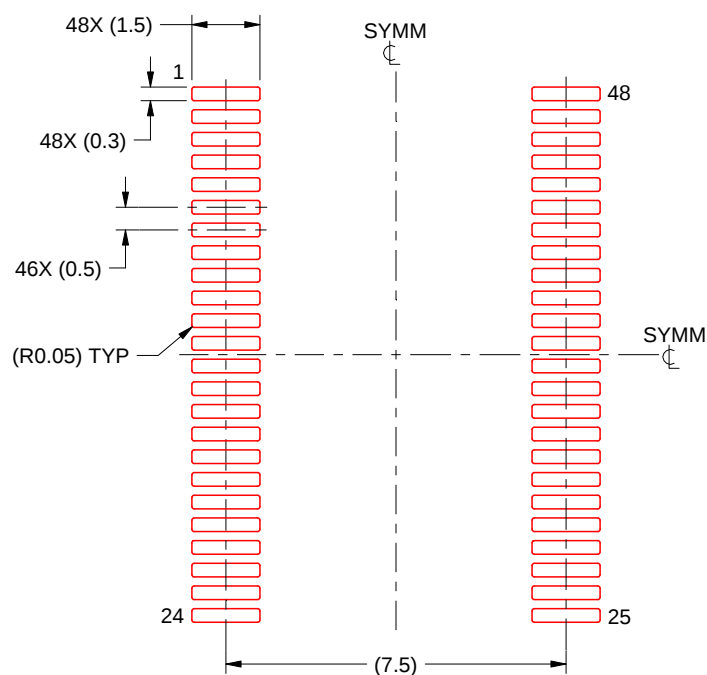
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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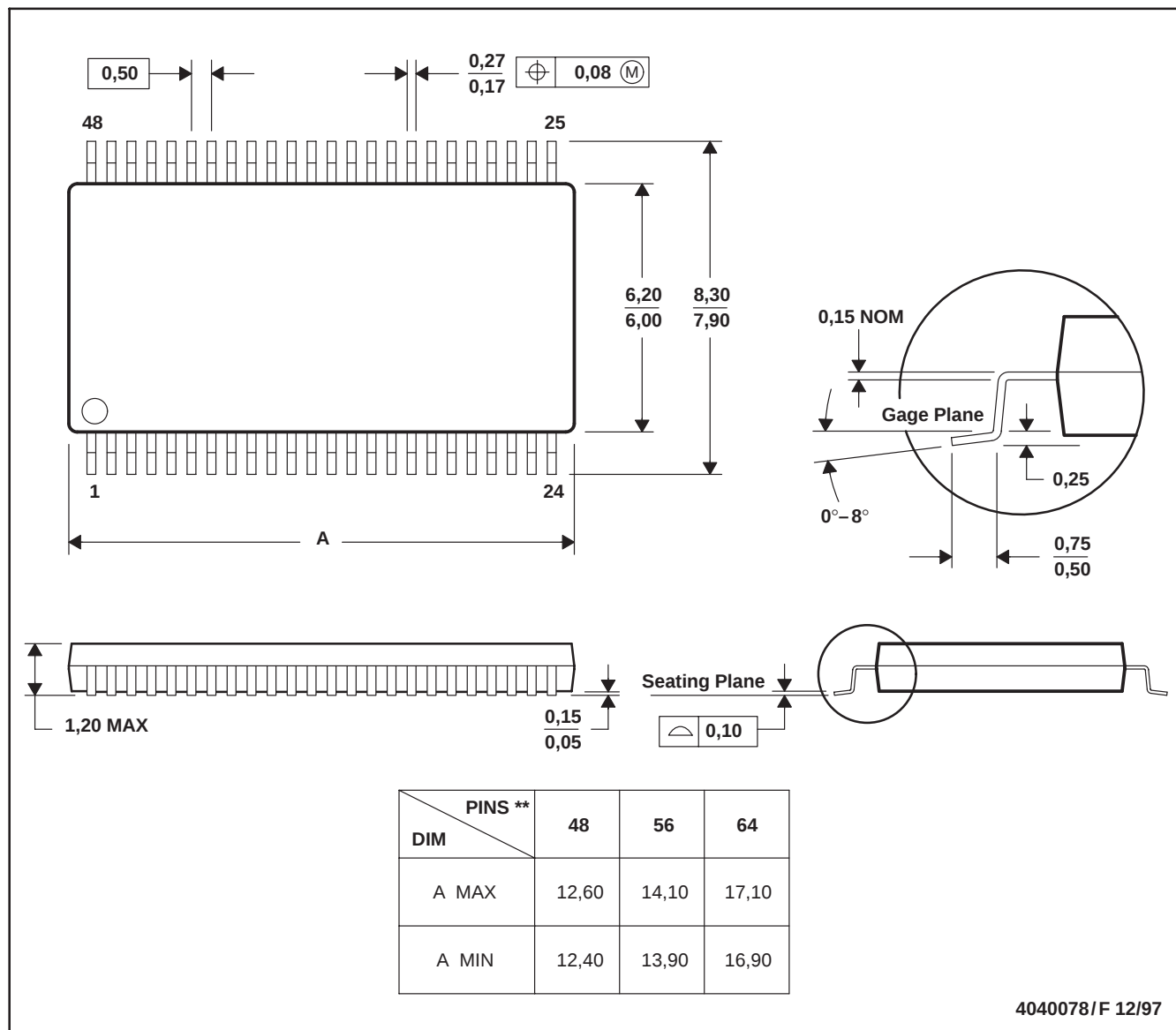
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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