

R1WV3216R Series

32Mb superSRAM (2M wordx16bit)

REJ03C0215-0100Z

Rev.1.00

2004.4.13

Description

The R1WV3216R Series is a family of low voltage 32-Mbit static RAMs organized as 2097152-words by 16-bit, fabricated by Renesas's high-performance 0.15um CMOS and TFT technologies.

The R1WV3216R Series is suitable for memory applications where a simple interfacing , battery operating and battery backup are the important design objectives.

The R1WV3216R Series is made by stacked-micro-package technology and two chips of 16Mbit superSRAMs are assembled in one package.

The R1WV3216R Series is packaged in a 52pin micro thin small outline mount device[μTSOP / 10.79mm x 10.49mm with the pin-pitch of 0.4mm] or a 48balls fine pitch ball grid array [f-BGA / 7.5mmx8.5mm with the ball-pitch of 0.75mm and 6x8 array] . It gives the best solution for a compaction of mounting area as well as flexibility of wiring pattern of printed circuit boards.

Features

- Single 2.7-3.6V power supply
- Small stand-by current:4μA (3.0V, typ.)
- Data retention supply voltage =2.0V
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion by CS1#, CS2, LB# and UB#
- Common Data I/O
- Three-state outputs: OR-tie capability
- OE# prevents data contention on the I/O bus
- Process technology: 0.15um CMOS

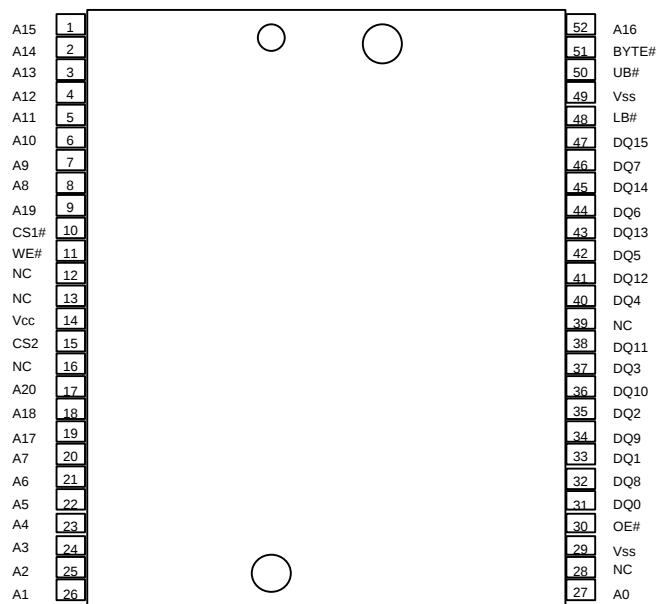
Ordering Information

Type No.	Access time	Package
R1WV3216RSD-7S%	70 ns	350-mil 52-pin plastic μ - TSOP(II) (normal-bend type) (52PTG)
R1WV3216RSD-8S%	85 ns	
R1WV3216RBG-7S%	70 ns	7.5mmx8.5mm f-BGA 0.75mm pitch 48ball
R1WV3216RBG-8S%	85 ns	

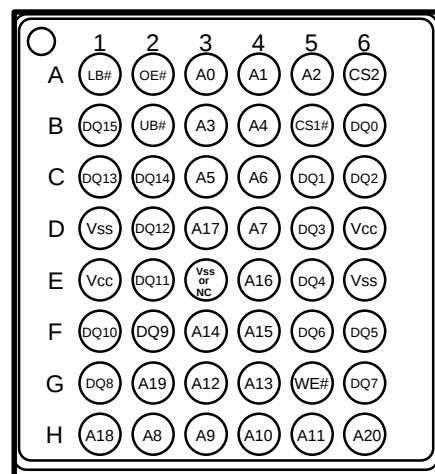
% - Temperature version; see table below

%	Temperature Range
R	0 ~ +70 °C
W	-20 ~ +85 °C
I	-40 ~ +85 °C

Pin Arrangement

52-pin μ TSOP

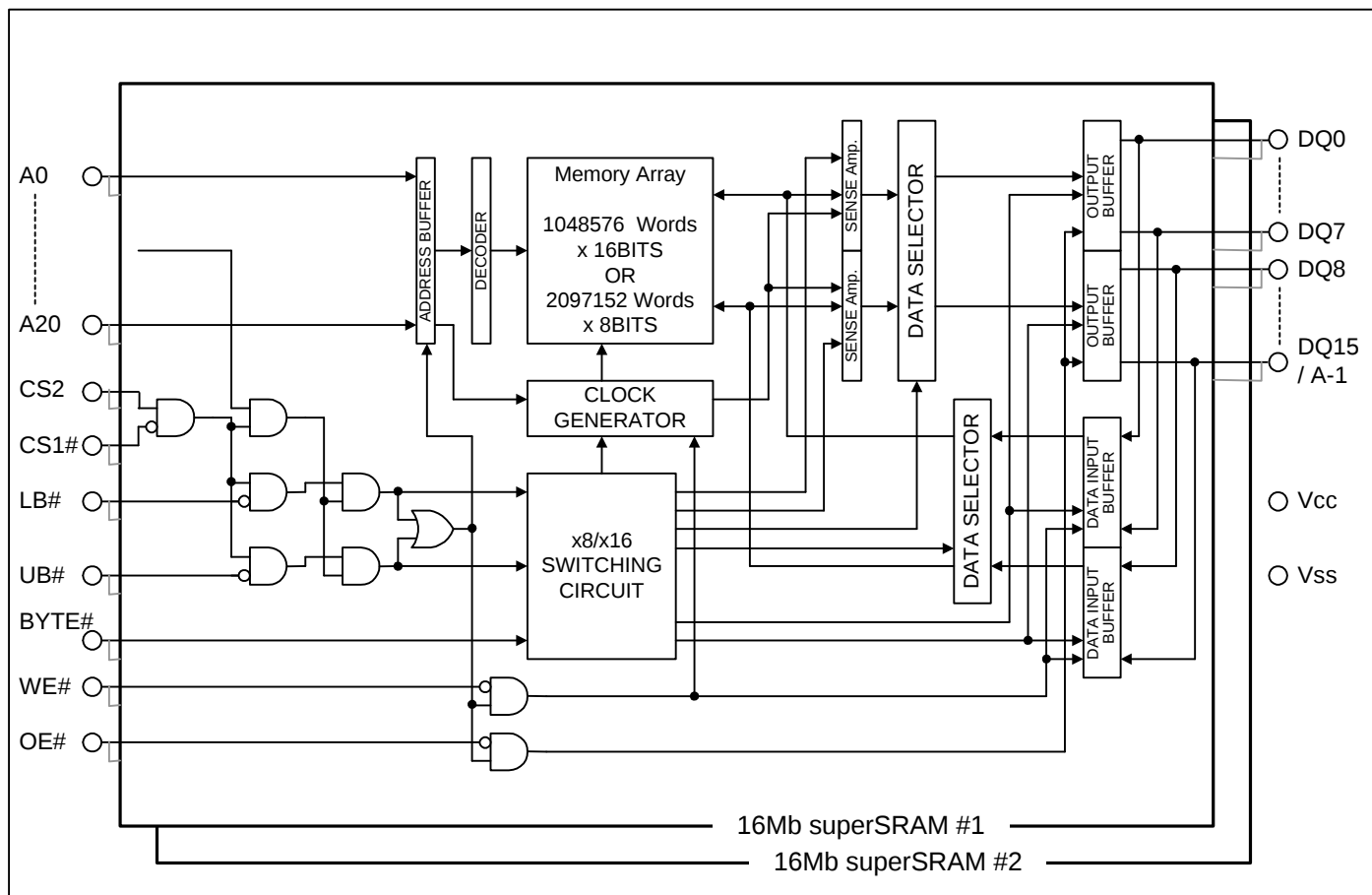
48-pin fBGA



Pin Description

Pin name	Function
A0 to A20	Address input
DQ 0 to DQ15	Data input/output
CS1# & CS2	Chip select
WE#	Write enable
OE#	Output enable
LB#	Lower byte select
UB#	Upper byte select
Vcc	Power supply
Vss	Ground
BYTE#	Byte (x8 mode) enable input
NC	Non connection

Block Diagram



Note: BYTE# pin supported by only TSOP type.

Operating Table

CS1#	CS2	BYTE#	LB#	UB#	WE#	OE#	DQ0-7	DQ8-14	DQ15	Operation
H	X	X	X	X	X	X	High-Z	High-Z	High-Z	Stand by
X	L	X	X	X	X	X	High-Z	High-Z	High-Z	Stand by
X	X	H	H	H	X	X	High-Z	High-Z	High-Z	Stand by
L	H	H	L	H	L	X	Din	High-Z	High-Z	Write in lower byte
L	H	H	L	H	H	L	Dout	High-Z	High-Z	Read from lower byte
L	H	X	X	X	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	H	L	L	X	High-Z	Din	Din	Write in upper byte
L	H	H	H	L	H	L	High-Z	Dout	Dout	Read from upper byte
L	H	H	L	L	L	X	Din	Din	Din	Write
L	H	H	L	L	H	L	Dout	Dout	Dout	Read
L	H	L	L	L	L	X	Din	High-Z	A-1	Write
L	H	L	L	L	H	L	Dout	High-Z	A-1	Read

Note 1. H: VIH L: VIL X: VIH or VIL

2. BYTE# pin supported by only TSOP type. When apply BYTE# = "L", please assign LB#=UB#="L".

Absolute Maximum Ratings

Parameter	Symbol	Value		Unit
Power supply voltage relative to Vss	Vcc	-0.5 to +4.6		V
Terminal voltage on any pin relation to Vss	V _T	-0.5* ¹ to Vcc+0.3* ²		V
Power dissipation	P _T	0.7		W
Operation temperature	T _{opr}	R ver.	0 to +70	°C
		W ver.	-20 to +85	°C
		I ver.	-40 to +85	°C
Storage temperature	T _{stg}	-65 to +150		°C
Storage temperature range under bias	T _{bias}	R ver.	0 to +70	°C
		W ver.	-20 to +85	°C
		I ver.	-40 to +85	°C

Note 1: -2.0V in case of AC (Pulse width ≤ 30ns)

2: Maximum voltage is +4.6V

Recommended Operating Conditions

Parameter		Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage		V _{CC}	2.7	3.0	3.6	V	
		V _{SS}	0	0	0	V	
Input high voltage		V _{IH}	2.4	-	V _{CC} +0.2	V	
Input low voltage		V _{IL}	-0.2	-	0.4	V	1
Ambient temperature range	R ver.	T _a	0	-	+70	°C	2
	W ver.		-20	-	+85	°C	2
	I ver.		-40	-	+85	°C	2

Note 1. -2.0V in case of AC (Pulse width ≤ 30ns)

2. Ambient temperature range depends on R/W/I-version. Please see table on page 2.

DC Characteristics

Parameter	Symbol	Min.	Typ.* ¹	Max.	Unit	Test conditions* ²	
Input leakage current	I _{LI}	-	-	1	μA	V _{in} =V _{SS} to V _{CC}	
Output leakage current	I _{LO}	-	-	1	μA	CS1# =V _{IH} or CS2=V _{IL} or OE# = V _{IH} or WE# =V _{IL} or LB# =UB# =V _{IH} , V _{I/O} =V _{SS} to V _{CC}	
Average operating current	I _{CC1}	-	60	70	mA	Min. cycle, duty =100% I _{I/O} = 0 mA, CS1# =V _{IL} , CS2=V _{IH} Others = V _{IH} / V _{IL}	
	I _{CC2} Write	-	20	25	mA	Cycle time = 1 μs, I _{I/O} = 0 mA, CS1#≤ 0.2V, CS2 ≥ V _{CC} -0.2V V _{IH} ≥ V _{CC} -0.2V , V _{IL} ≤ 0.2V, Write & Read duty=100% respectively	
	I _{CC2} Read	-	15	20	mA		
Standby current	I _{SB}	-	0.1	0.3	mA	CS2=V _{IL}	
Standby current	I _{SB1}	-	4	12	μA	~+25°C	V _{in} ≥ 0V (1) 0V≤CS2≤0.2V or (2) CS2≥V _{CC} -0.2V, CS1# ≥V _{CC} -0.2V or (3) LB# =UB# ≥V _{CC} -0.2V, CS2≥V _{CC} -0.2V, CS1# ≤0.2V Average value
		-	7	24	μA	~+40°C	
		-	-	50	μA	~+70°C	
		-	-	80	μA	~+85°C	
Output hige voltage	V _{OH}	2.4	-	-	V	I _{OH} = -1mA	
Output Low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA	

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (T_a = 25°C), and not 100% tested.

2. BYTE# pin supported by only TSOP type.

BYTE# ≥ V_{CC}-0.2V or BYTE# ≤ 0.2V

Capacitance

(Ta = +25°C, f = 1MHz)

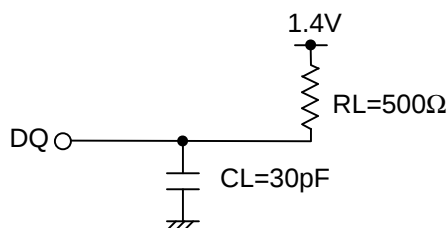
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	-	-	20	pF	V in = 0V	1
Input / output capacitance	C I/O	-	-	20	pF	V I/O = 0V	1

Note 1. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc=2.7~3.6V, Ta = 0~+70°C / -20~+85°C / -40~+85°C *)

- Input pulse levels: VIL= 0.4V, VIH=2.4V
- Input rise and fall time : 5ns
- Input and output timing reference levels : 1.4V
- Output load : See figures (Including scope and jig)



Note: Temperature range depends on R/W/I-version. Please see table on page 2.

Read Cycle

Parameter	Symbol	R1WV3216R**-7S		R1WV3216R**-8S		Unit	Notes
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	70	-	85	-	ns	
Address access time	t_{AA}	-	70	-	85	ns	
Chip select access time	t_{ACS1}	-	70	-	85	ns	
	t_{ACS2}	-	70	-	85	ns	
Output enable to output valid	t_{OE}	-	35	-	45	ns	
Output hold from address change	t_{OH}	10	-	10	-	ns	
LB#,UB# access time	t_{BA}	-	70	-	85	ns	
Chip select to output in low-Z	t_{CLZ}	10	-	10	-	ns	2,3
LB#,UB# enable to low-Z	t_{BLZ}	5	-	5	-	ns	2,3
Output enable to output in low-Z	t_{OLZ}	5	-	5	-	ns	2,3
Chip deselect to output in high-Z	t_{CHZ1}	0	25	0	30	ns	1,2,3
	t_{CHZ2}	0	25	0	30	ns	1,2,3
LB#,UB# disable to high-Z	t_{BHZ}	0	25	0	30	ns	1,2,3
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	ns	1,2,3

Write Cycle

Parameter	Symbol	R1WV3216R**-7S		R1WV3216R**-8S		Unit	Notes
		Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	70	-	85	-	ns	
Address valid to end of write	t_{AW}	65	-	70	-	ns	
Chip selection to end of write	t_{CW}	65	-	70	-	ns	5
Write pulse width	t_{WP}	55	-	60	-	ns	4
LB#,UB# valid to end of write	t_{BW}	65	-	70	-	ns	
Address setup time	t_{AS}	0	-	0	-	ns	6
Write recovery time	t_{WR}	0	-	0	-	ns	7
Data to write time overlap	t_{DW}	35	-	40	-	ns	
Data hold from write time	t_{DH}	0	-	0	-	ns	
Output active from end of write	t_{OW}	5	-	5	-	ns	2
Output disable to output in high-Z	t_{OHZ}	0	25	0	30	ns	1,2
Write to output in high-Z	t_{WHZ}	0	25	0	30	ns	1,2

Note 1. t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. AT any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

4. A write occurs during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
A write begins at the latest transition among CS1# going low, CS2 going high, WE# going low and LB# going low or UB# going low.

A write ends at the earliest transition among CS1# going high, CS2 going low, WE# going high and LB# going high or UB# going high. t_{WP} is measured from the beginning of write to the end of write.

5. t_{CW} is measured from the later of CS1# going low or CS2 going high to end of write.

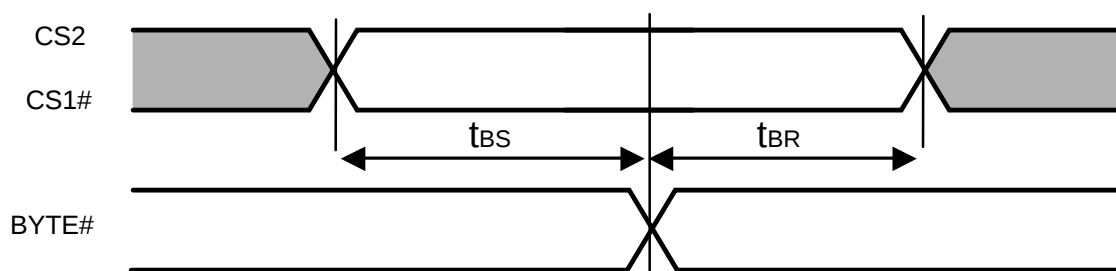
6. t_{AS} is measured the address valid to the beginning of write.

7. t_{WR} is measured from the earliest of CS1# or WE# going high or CS2 going low to the end of write cycle.

Byte enable (supported by only 52-pin μ TSOP)

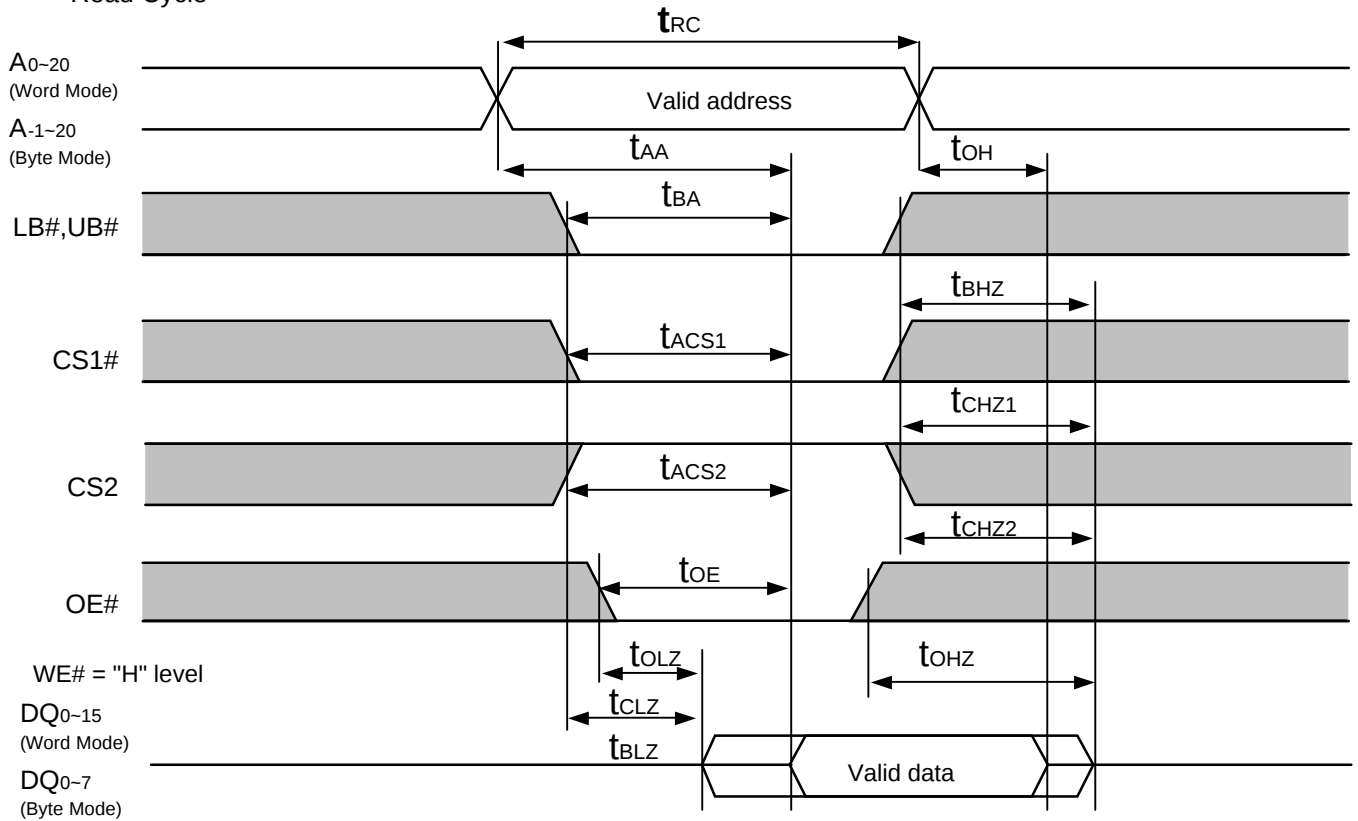
Parameter	Symbol	R1WV3216R**-7S		R1WV3216R**-8S		Unit	Notes
		Min.	Max.	Min.	Max.		
Byte setup time	t_{BS}	5	-	5	-	ms	
Byte recovery time	t_{BR}	5	-	5	-	ms	

BYTE# Timing Waveform

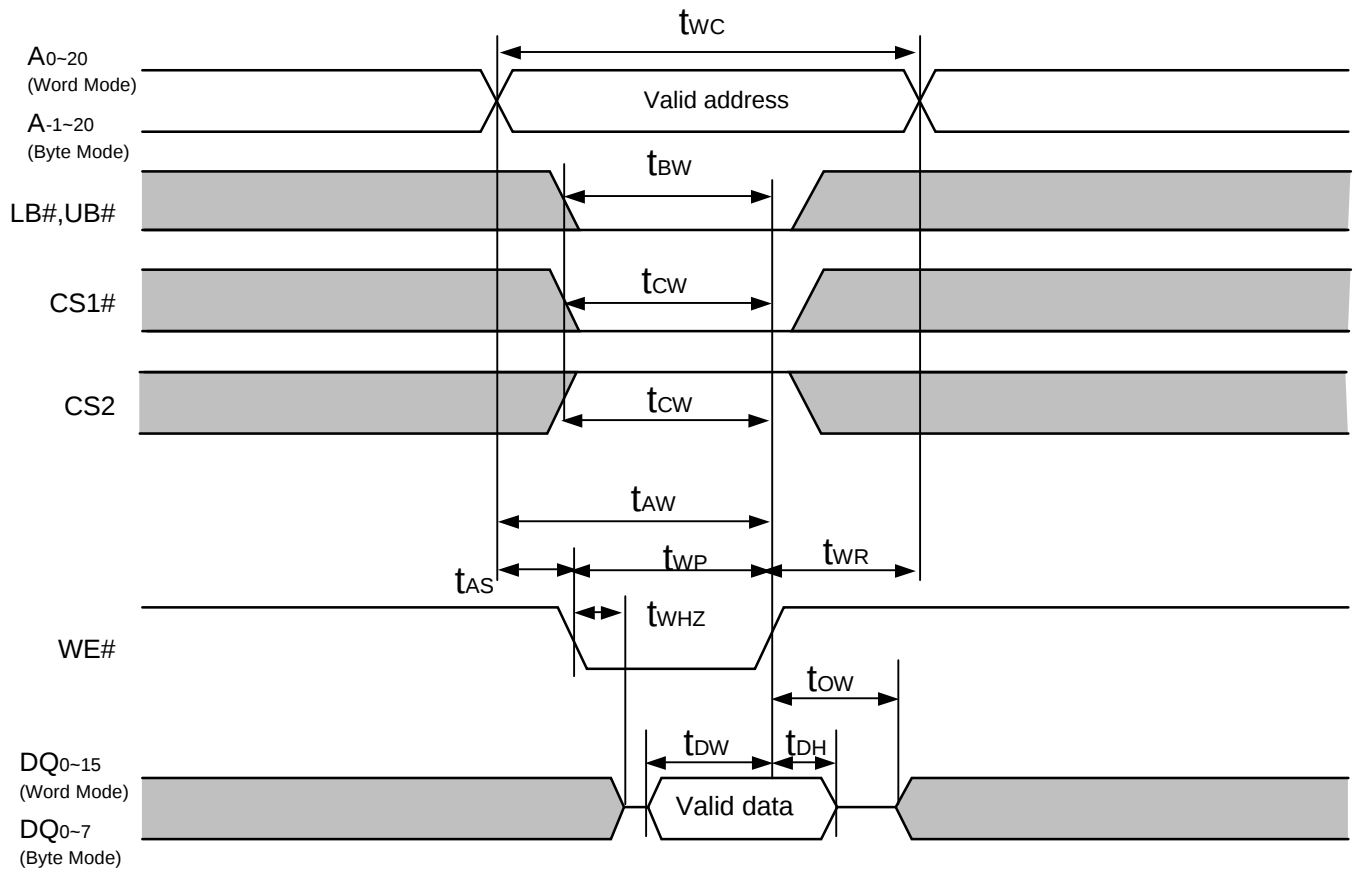


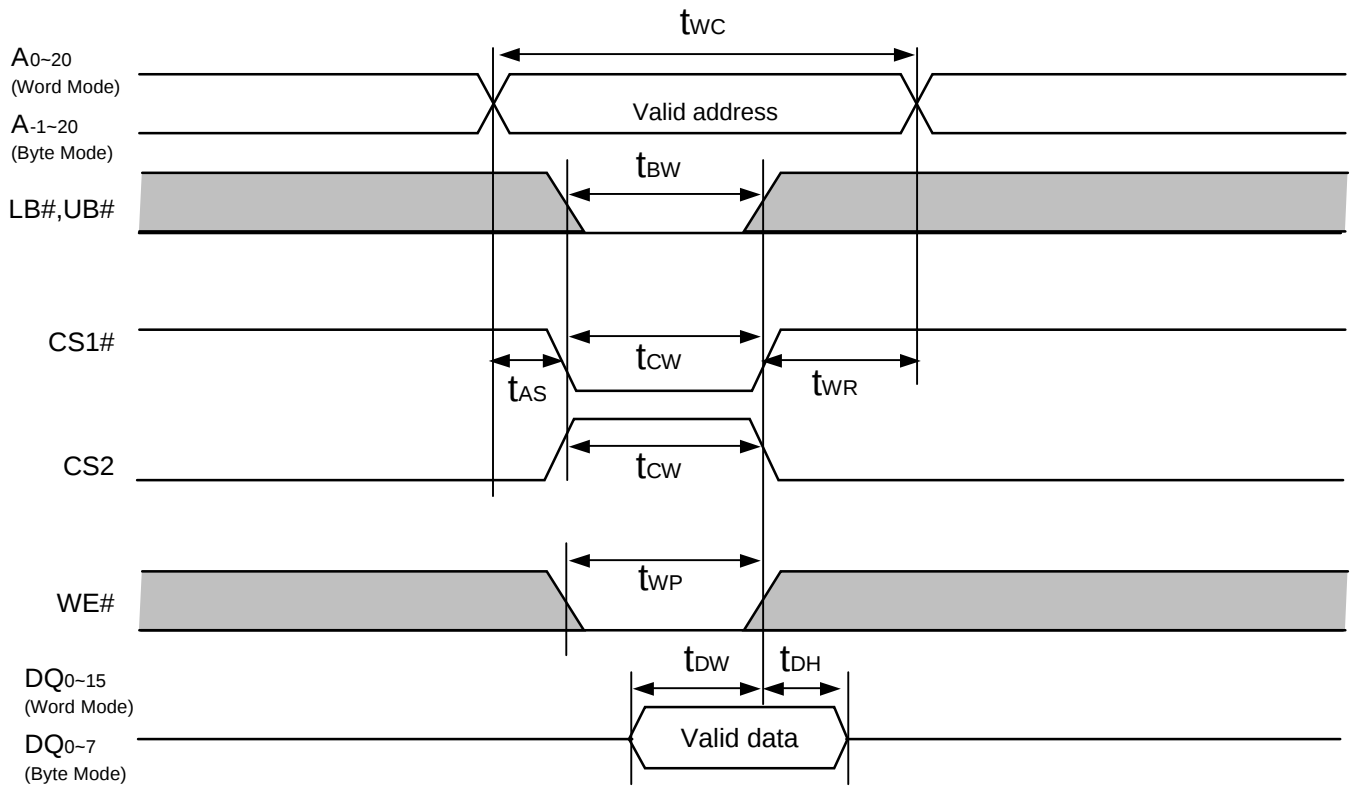
Timing Waveform

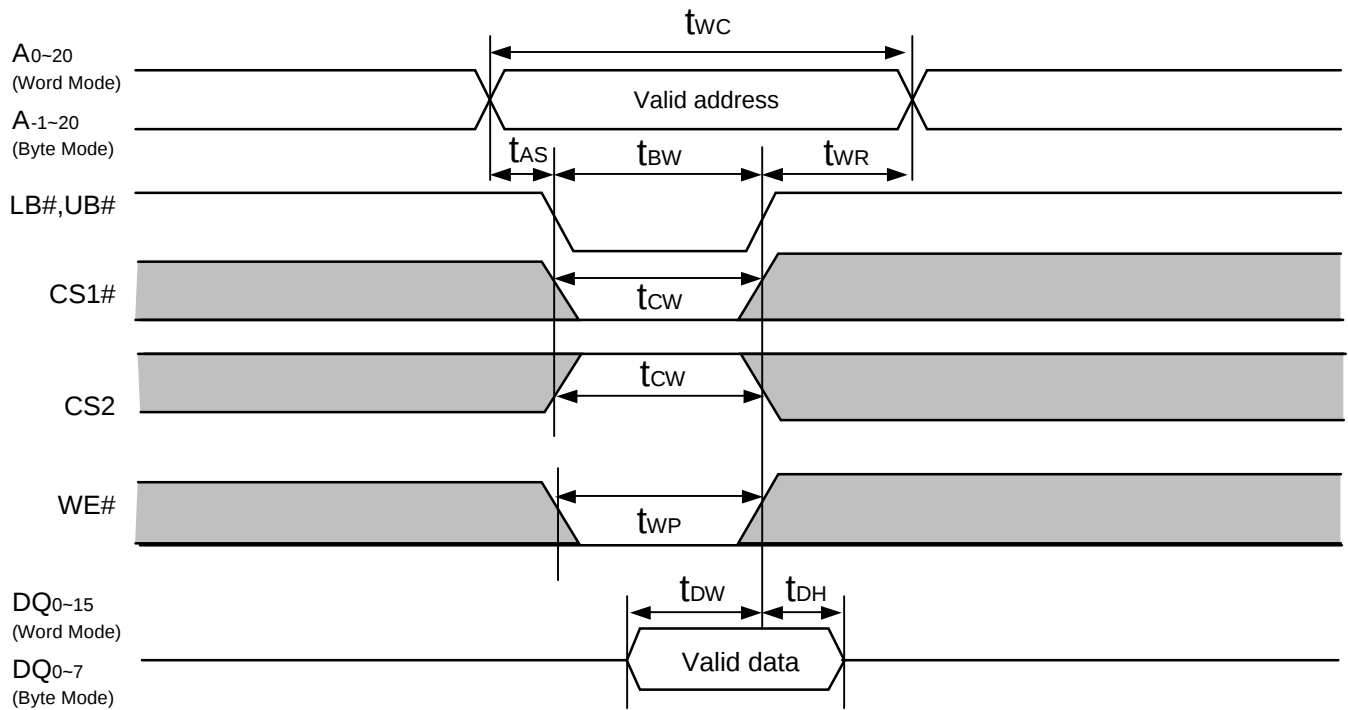
Read Cycle



Write Cycle (1) (WE# Clock)



Write Cycle (2) (CS1# ,CS2 Clock, OE#=V_{IH})

Write Cycle (3) (LB#,UB#Clock, OE#=V_{IH})

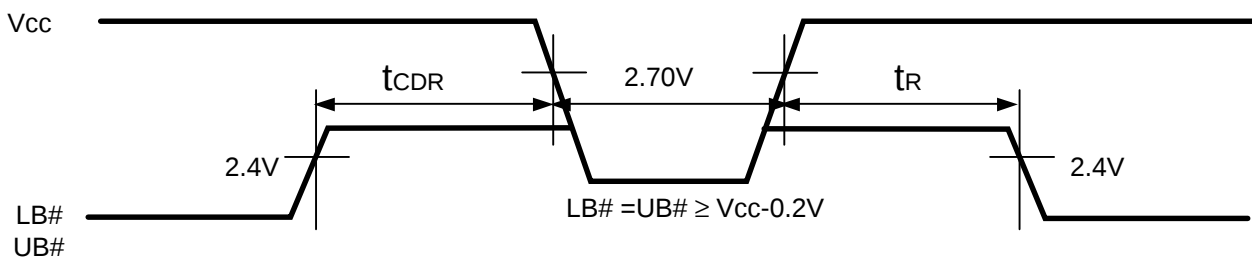
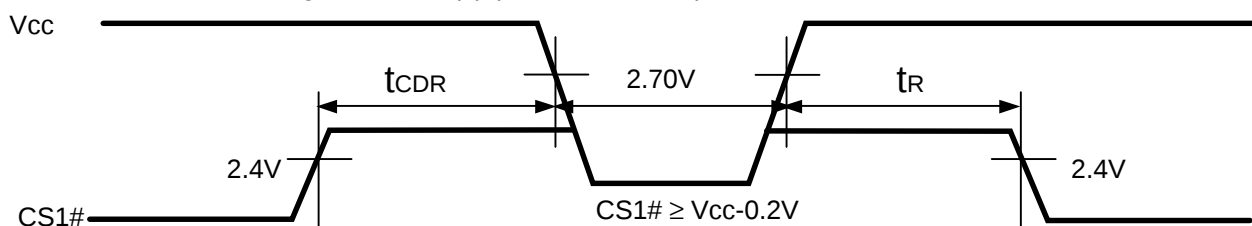
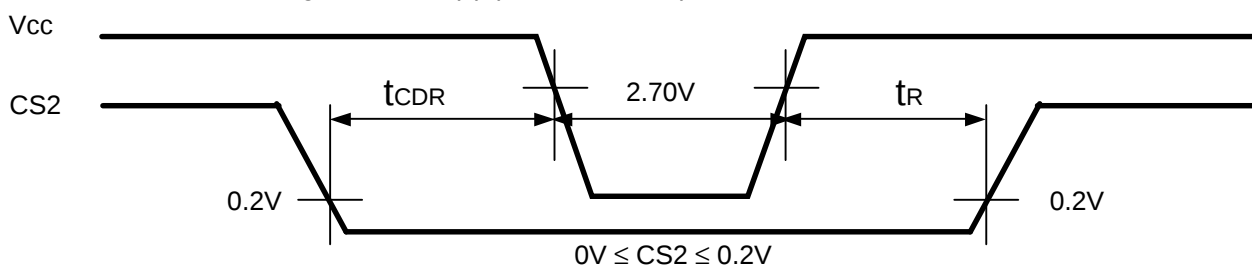
Data Retention Characteristics

Parameter	Symbol	Min.	Typ.*1	Max.	Unit	Test conditions*2,3
Vcc for data retention	V_{DR}	2.0	-	3.6	V	$V_{in} \geq 0V$ (1) $0V \leq CS2 \leq 0.2V$ or (2) $CS2 \geq V_{cc}-0.2V$, $CS1\# \geq V_{cc}-0.2V$ or (3) $LB\# = UB\# \geq V_{cc}-0.2V$, $CS2 \geq V_{cc}-0.2V$, $CS1\# \leq 0.2V$
Data retention current	I_{CCDR}	-	4	12	μA	$\sim +25^{\circ}C$ $V_{cc}=3.0V, V_{in} \geq 0V$
		-	7	24	μA	$\sim +40^{\circ}C$ (1) $0V \leq CS2 \leq 0.2V$ or (2) $CS2 \geq V_{cc}-0.2V$, $CS1\# \geq V_{cc}-0.2V$ or
		-	-	50	μA	$\sim +70^{\circ}C$ (3) $LB\# = UB\# \geq V_{cc}-0.2V$, $CS2 \geq V_{cc}-0.2V$, $CS1\# \leq 0.2V$
		-	-	80	μA	$\sim +85^{\circ}C$ Average value
Chip deselect to data retention time	t_{CDR}	0	-	-	ns	See retention waveform
Operation recovery time	t_R	5	-	-	ms	

Note 1. Typical parameter of I_{CCDR} indicates the value for the center of distribution at $V_{cc}=3.0V$ and not 100% tested.

2. $BYTE\#$ pin supported by TSOP type. $BYTE\# \geq V_{cc}-0.2V$ or $BYTE\# \leq 0.2V$

3. Also $CS2$ controls address buffer, $WE\#$ buffer, $CS1\#$ buffer, $OE\#$ buffer, $LB\#$, $UB\#$ buffer and Din buffer. If $CS2$ controls data retention mode, V_{in} levels (address, $WE\#$, $OE\#$, $CS1\#$, $LB\#$, $UB\#$, I/O) can be in the high impedance state. If $CS1\#$ controls data retention mode, $CS2$ must be $CS2 \geq V_{cc}-0.2V$ or $0V \leq CS2 \leq 0.2V$. The other input levels (address, $WE\#$, $OE\#$, $CS1\#$, $LB\#$, $UB\#$, I/O) can be in the high impedance state.

Data Retention timing Waveform (1) ($LB\#, UB\#$ Controlled)Data Retention timing Waveform (2) ($CS1\#$ Controlled)Data Retention timing Waveform (3) ($CS2$ Controlled)

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